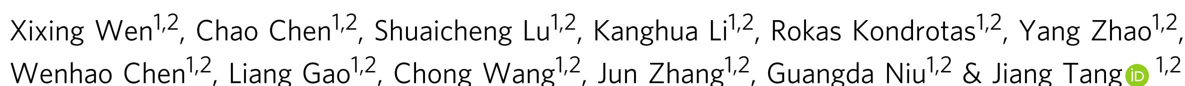
nature COMMUNICATIONS

ARTICLE

DOI: 10.1038/s41467-018-04634-6 OPEN

Vapor transport deposition of antimony selenide thin film solar cells with 7.6% efficiency



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Antimony selenide is an emerging promising thin film photovoltaic material thanks to its binary composition, suitable bandgap, high absorption coefficient, inert grain boundaries and earth-abundant constituents. However, current devices produced from rapid thermal evaporation strategy suffer from low-quality film and unsatisfactory performance. Herein, we develop a vapor transport deposition technique to fabricate antimony selenide films, a technique that enables continuous and low-cost manufacturing of cadmium telluride solar cells. We improve the crystallinity of antimony selenide films and then successfully produce superstrate cadmium sulfide/antimony selenide solar cells with a certified power conversion efficiency of 7.6%, a net 2% improvement over previous 5.6% record of the same device configuration. We analyze the deep defects in antimony selenide solar cells, and find that the density of the dominant deep defects is reduced by one order of magnitude using vapor transport deposition process.

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Antimony selenide (Sb_2Se_3) has recently emerged as a promising green alternative to CdTe solar cells because it possesses very attractive optoelectronic properties such as proper bandgap (about 1.03 eV indirect and 1.17 eV direct) for the absorption of a significant portion of the solar spectrum, high optical absorption coefficient (greater than 10^5 cm^{-1}) and decent carrier mobility (about 10 $cm^2 V^{-1} s^{-1}$)[1–3]. Besides, because it is a binary compound with high vapor pressure, a fast, low temperature vacuum-based deposition technique can be employed like the ones established in CdTe photovoltaics. It also possesses a one-dimensional crystal structure with loose van der Waals interaction between ribbons[1], thereby enabling grain boundaries free of dangling bonds in *c*-axis-oriented films and minimizing recombination losses therein. Furthermore, the earth-abundant elemental compositions of Sb_2Se_3 as well as its easy fabrication promise low-cost manufacturing. All these attributes suggest the great potential of Sb_2Se_3 for high-efficiency thin film solar cell and commercial application.

However, the highest power conversion efficiency (PCE) of Sb_2Se_3 thin film solar cells with a CdS/Sb_2Se_3 superstrate configuration is so far 5.6%[2, 4–11], and with a ZnO/Sb_2Se_3 superstrate configuration 5.93%[1]. Employing PbS colloidal quantum dots (QDs) as the hole transport layer, as-fabricated device CdS/Sb_2Se_3/PbS QDs demonstrated an efficiency of 6.5%[12]. Rapid thermal evaporation (RTE) was used to fabricate all above-mentioned Sb_2Se_3 solar cells. RTE is a process similar to close-space sublimation[2], in which the vapor is limited to a confined space and rapidly deposits on the substrate. The distance from the substrate to the evaporation source is only 0.8 cm, and the whole deposition is performed within 35 s. The small confined space and the rapid deposition increase the difficulty of mixing the vapor particles (Se, Sb and Sb_xSe_y) evenly, potentially promoting defect formation. The formation of defects, such as interstitial and antisite defects, accelerates nonradiative recombination and degrades device performance[13–16]. Furthermore, limited by our RTE facility, a simple one-zone tube furnace, the source and substrate temperatures are strongly correlated, which seriously hinders the independent optimization of both substrate and source temperature. These problems in our RTE technique have seriously restricted the development of Sb_2Se_3 solar cells. Therefore, we urgently need to explore alternative strategies to further improve Sb_2Se_3 film quality and device performance.

Here, we develop a vapor transport deposition (VTD) process to fabricate record efficiency Sb_2Se_3 thin film solar cells. In the VTD process, both the substrate temperature and the distance between source and substrate are adjustable, enabling not only highly oriented Sb_2Se_3 film, but also enormously improved film crystallinity and reduced bulk and interfacial defects in Sb_2Se_3 solar cells. In addition, the VTD process is a proven low-cost and fast-turnaround manufacturing method for commercial CdTe solar cells[17, 18], and adopting this technique for Sb_2Se_3 technology could facilitate the commercial competitiveness of Sb_2Se_3 solar cells. After optimizing the Sb_2Se_3 films via VTD process, we obtain the champion indium tin oxide (ITO)/CdS/Sb_2Se_3/Au solar cells with a certified efficiency of 7.6%, which is a record of all Sb_2Se_3 thin film solar cells by far[1, 2, 4–12, 19, 20] and represents a net 2% efficiency gain over previous report with the same device configuration[2]. We comparatively analyze the physical properties of VTD-fabricated and RTE-fabricated Sb_2Se_3 devices by X-ray diffraction (XRD), transient absorption (TA) spectroscopy and deep-level transient spectroscopy (DLTS). We find that the VTD-fabricated devices possess much higher film crystallinity, longer carrier lifetime and fewer bulk and interfacial defects than RTE-fabricated devices. Especially, the reduced density of defect complex (Sb_{Se}+Se_{Sb}) enhances the device performance by decreasing the photo-generated carrier recombination.

Results

Fabrication of Sb_2Se_3 films via VTD process. A schematic representation of VTD system is shown in Fig. 1a. The Sb_2Se_3 powder and the substrate were placed in the center and at the right end of the heater, respectively. The full deposition details are provided in experimental section. Hereby, the heating temperature of the evaporation source, the pressure in quartz tube and the substrate temperature are the key factors that determining the quality of final Sb_2Se_3 films. The distance between the substrate and the heating center was varied to achieve adjustable substrate temperature. We deposited Sb_2Se_3 films at different heating temperatures, pressures and substrate temperatures. XRDs of all Sb_2Se_3 films were measured to characterize the crystallinity and orientation of these films, which is shown in Supplementary Fig. 1. All the Sb_2Se_3 films had a preferred [221] orientation with the only difference being the intensity of the diffraction peaks. As Sb_2Se_3 is composed of one-dimensional $(Sb_4Se_6)_n$ ribbons stacking together via weak van der Waals force, a proper film orientation is crucial for facile carrier transport in the film[1, 2]. Our previous reports have demonstrated that [221]-orientation enhances carrier transport across Sb_2Se_3 film[1, 2, 6, 8]. Therefore, with the film thickness and measurement details kept strictly identical, we utilized the intensity of (221) XRD peaks in Sb_2Se_3 films to evaluate their crystallinity. The crystallinity evolution of Sb_2Se_3 films deposited on CdS layers with varied evaporation temperature, pressure and distance was investigated, as shown in Fig. 1b. By carefully optimizing the three key factors, Sb_2Se_3 film with the highest crystallinity was obtained when the evaporating temperature was set at 510 °C, the pressure was 3.2 Pa and the distance from the substrate to the heating center was 21 cm. Here, the actual temperature curves of powder and substrate were

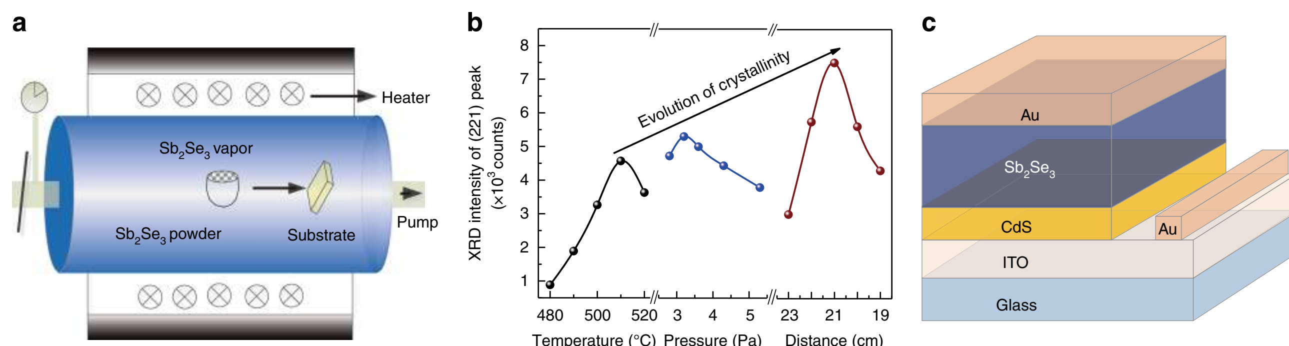

Fig. 1 Fabrication of CdS/Sb_2Se_3 solar cells. **a** Schematics of our VTD system. **b** Evolution of crystallinity with the optimization of deposition condition. **c** The device structure of our Sb_2Se_3 solar cells

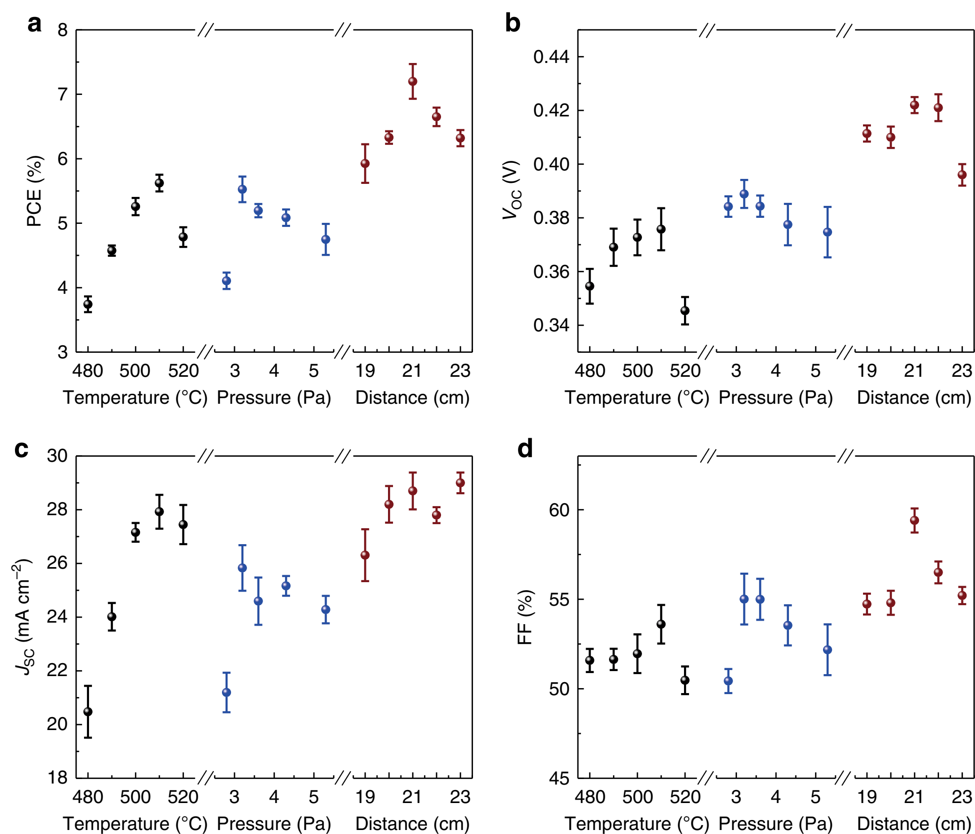

Fig. 2 Deposition condition-dependent photovoltaic characteristics. **a** Power conversion efficiency (PCE), **b** open-circuit voltage (V_{OC}), **c** short-circuit current density (J_{SC}) and **d** fill factor (FF) of the CdS/Sb_2Se_3 solar cells fabricated by VTD process. A total of 135 devices are included for the statistics analysis. Solid sphere symbols and error bars indicate average values and standard deviations, respectively

monitored during the heating and cooling steps. The input temperature program and the measured temperature curves of substrate and powder are shown in Supplementary Fig. 2. This heating profile and substrate distance corresponded to the maximum actual source and substrate temperatures of 540 °C and 390 °C, respectively, as monitored by the thermocouples.

The crystallinity evolution of Sb_2Se_3 films indicates the importance of evaporation temperature, pressure and substrate temperature in VTD process. High evaporation temperature increases the kinetic energy of vapor particles and the surface mobility of adatoms on the substrate[21]. On the other hand, high pressure can increase in-flight collisions with background gas atoms, and then reduced the kinetic energy of vapor particles[21,22]. In addition, increasing the substrate temperature will lead to the increased surface mobility of adatoms[22]. Hence, the kinetic energy of vapor particles and surface mobility of adatoms are ultimately defined by combination of evaporation temperature, pressure and substrate temperature. During the Sb_2Se_3 film deposition, vapor particles with proper kinetic energy and adatoms with proper surface mobility are mandatory for high-quality Sb_2Se_3 films. Energetic vapor particles and high mobility of adatoms may increase the instability of adatoms, causing displacements of lattice and consequently creating lattice defects[21,22]. Such defects may act as new nucleation sites and increase nucleation density of adatoms[22]. In the extreme, the increased lattice defects and nucleation density may result in decreased crystallinity and quality of the film. That is why the crystallinity of the Sb_2Se_3 film decreased when deposited at overly high evaporation temperature, lower pressure and closer distance to evaporation source.

Device performance. The Sb_2Se_3 absorber layers were fabricated under the above-mentioned conditions, and the corresponding device structure ITO/CdS/Sb_2Se_3/Au is shown in Fig. 1c. The dependence of device performance on different evaporation temperatures, pressures and distances is summarized in Fig. 2. The variation trend of PCE is similar to the crystallinity evolution of Sb_2Se_3 films (Fig. 1b), which indicates that device performance strongly correlates with the crystallinity of Sb_2Se_3 film. As can be seen from Fig. 2, the best PCE, open-circuit voltage (V_{OC}), short-circuit current density (J_{SC}) and fill factor (FF) were obtained under the deposition condition where the highest film crystallinity was achieved (Fig. 1b). After carefully optimizing Sb_2Se_3 films and devices, the champion device with a certified power conversion efficiency of 7.6% was obtained (certificate included in Supplementary Fig. 3). This value represents the highest PCE of all Sb_2Se_3 thin film solar cells reported so far[1,2,4–12], which is 2% higher than previous 5.6% certified efficiency with the same device configuration[2]. Figure 3a shows the light current density-voltage (*J-V*) curve of the champion VTD-fabricated CdS/Sb_2Se_3 solar cell with certified PCE of 7.6%, V_{OC} of 0.42 V, J_{SC} of 29.9 mA cm^{-2} and FF of 60.4%. The *J-V* curve of a RTE-fabricated solar cell with PCE of 5.6% ($V_{OC} = 0.39$ V, $J_{SC} = 25.3$ mA cm^{-2} and FF = 56.4%) is also included in Fig. 3a for comparison. Obviously, every performance parameter of the VTD-fabricated solar cell, especially J_{SC}, is larger than that of the RTE-fabricated device.

We further checked the external quantum efficiency (EQE) of the two devices (Fig. 3b) to investigate their photo-response. The EQE spectrum of VTD-fabricated device demonstrated a higher photo-response from 520 nm (the absorption onset of CdS layer)

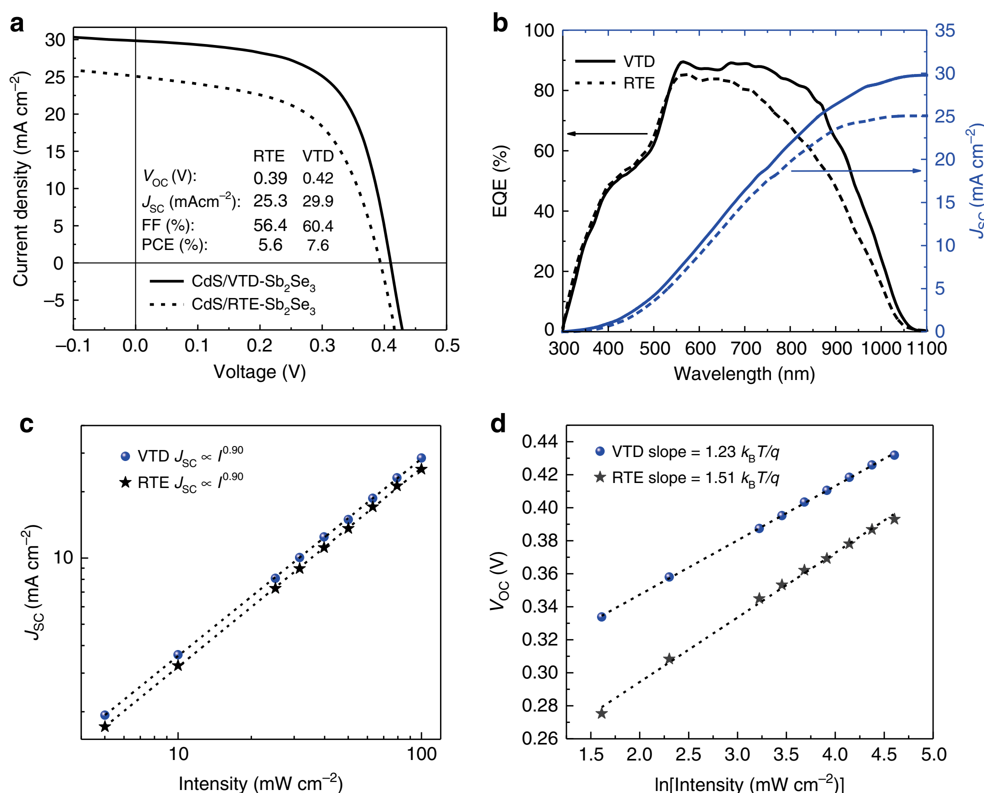

Fig. 3 Device performance and light intensity-dependent J_{SC} and V_{OC} of devices. **a** The light *J-V* curves of VTD- and RTE-fabricated devices under AM1.5 G illumination. The *J-V* curve of the VTD-fabricated device with certified efficiency of 7.6% (area = 0.091 cm^2) was measured by National Institute of Metrology on 1 September 2017. The calibration certificate number is GXtc2017-1987 (Supplementary Fig. 3). **b** EQE and integrated J_{SC} of the VTD- and RTE-fabricated devices. Light intensity-dependent **c** J_{SC} and **d** V_{OC}. Neutral-density filters (THORLABS) were used to control the light intensity

to 1100 nm than that of RTE-fabricated device. The maximum EQE of VTD-fabricated device was close to 90% between 540 and 720 nm. For comparison, the device fabricated by our RTE technique only had the maximum EQE of about 85%. This suggests the VTD-fabricated devices possess very low recombination losses of photo-generated carriers and long carrier lifetimes at CdS/Sb_2Se_3 interface and in the whole Sb_2Se_3 absorber[23]. In Fig. 3b, we derived the current density of 29.8 and 25.1 mA cm^{-2} by integrating the EQE spectra with standard AM1.5 spectrum to further validate our J_{SC} values, which agreed with the experimental values of 29.9 and 25.3 mA cm^{-2} very well, respectively. Furthermore, a solar cell with initial PCE of 7.25% was stored in ambient air for about 40 days without encapsulation. This representative device was measured every week to monitor the stability of Sb_2Se_3 film solar cell, and the results are displayed in Supplementary Fig. 4a. The PCE remained unchanged during the whole process. For the stability of device under continuous illumination, Supplementary Fig. 4b shows slight decrease for CdS/Sb_2Se_3 device but no decrease for ZnO/Sb_2Se_3 device, which is consistent with the previous report[1]. These results indicate that VTD process is a simple and effective technique for producing high-efficiency and stable Sb_2Se_3 thin film solar cells.

Carrier recombination in CdS/Sb_2Se_3 solar cells. From the improved EQE of VTD-fabricated devices, we inferred that the carrier transport was enhanced, and recombination loss was reduced in the active Sb_2Se_3 layer by VTD process. Therefore, to further clarify the carrier recombination processes in Sb_2Se_3 solar cells, we performed light-intensity-dependent J_{SC} and V_{OC} measurements on the VTD- and RTE-based photovoltaic devices. The complete sets of *J-V* curves are given in Supplementary Fig. 5.

Figure 3c illustrates J_{SC} as a function of light intensity (I). Herein, J_{SC} was fitted according to the power law dependence ($J_{SC} \propto I^{\alpha}$) by the log–log scale plot. The power value α for both devices is 0.9, close to unity (first-order). This means that trap-assisted recombination is present in both solar cells and is the dominating loss mechanism[24, 25]. The light-intensity-dependent V_{OC} can provide critical insights into the recombination mechanism in the solar cells[26]. For V_{OC} measurement, the device is open circuit, so there is no current extraction from the devices, and all photo-generated carriers recombine in Sb_2Se_3 film. Thus, the carrier recombination process can be reflected based on the relationship of $V_{OC} \propto n(k_BT/q)\ln(I)$, where k_B is the Boltzmann constant, T is the temperature and q is elementary charge[26–29]. $n(k_BT/q)$ is the slope of V_{OC} vs. the natural logarithm of light-intensity $\ln(I)$. For trap-free solar cells, the slope of V_{OC} vs. $\ln(I)$ should be k_BT/q (i.e., $n = 1$)[26, 29]. For our devices, as shown in Fig. 3d, the slopes obtained by linear fitting were $1.23(k_BT/q)$ for the VTD-fabricated device and $1.51(k_BT/q)$ for the RTE-fabricated device. This, again, indicates the presence of trap-assisted Shockley–Read–Hall (SRH) recombination in both devices[29, 30]. The slope was decreased from $1.51(k_BT/q)$ to $1.23(k_BT/q)$ by using VTD process, suggesting reduced trap-assisted recombination in VTD-fabricated devices[28, 31]. We measured the TA decay of the two devices to investigate the carrier lifetime (Supplementary Fig. 6). For the steady-state absorption (Supplementary Fig. 7) of VTD- and RTE-fabricated Sb_2Se_3 films, the absorption rose to the maximum at around 940 nm. Thus, the transient kinetic decay was monitored at 940 nm. By fitting the kinetic decay data, the longer carrier lifetime (1339 ps) was obtained in VTD-fabricated device than that (1149 ps) of RTE-derived device. Longer carrier lifetime not only permits more efficient carrier collection and hence larger J_{SC} (VTD 29.9 mA cm^{-2} vs. RTE 25.3 mA cm^{-2}),

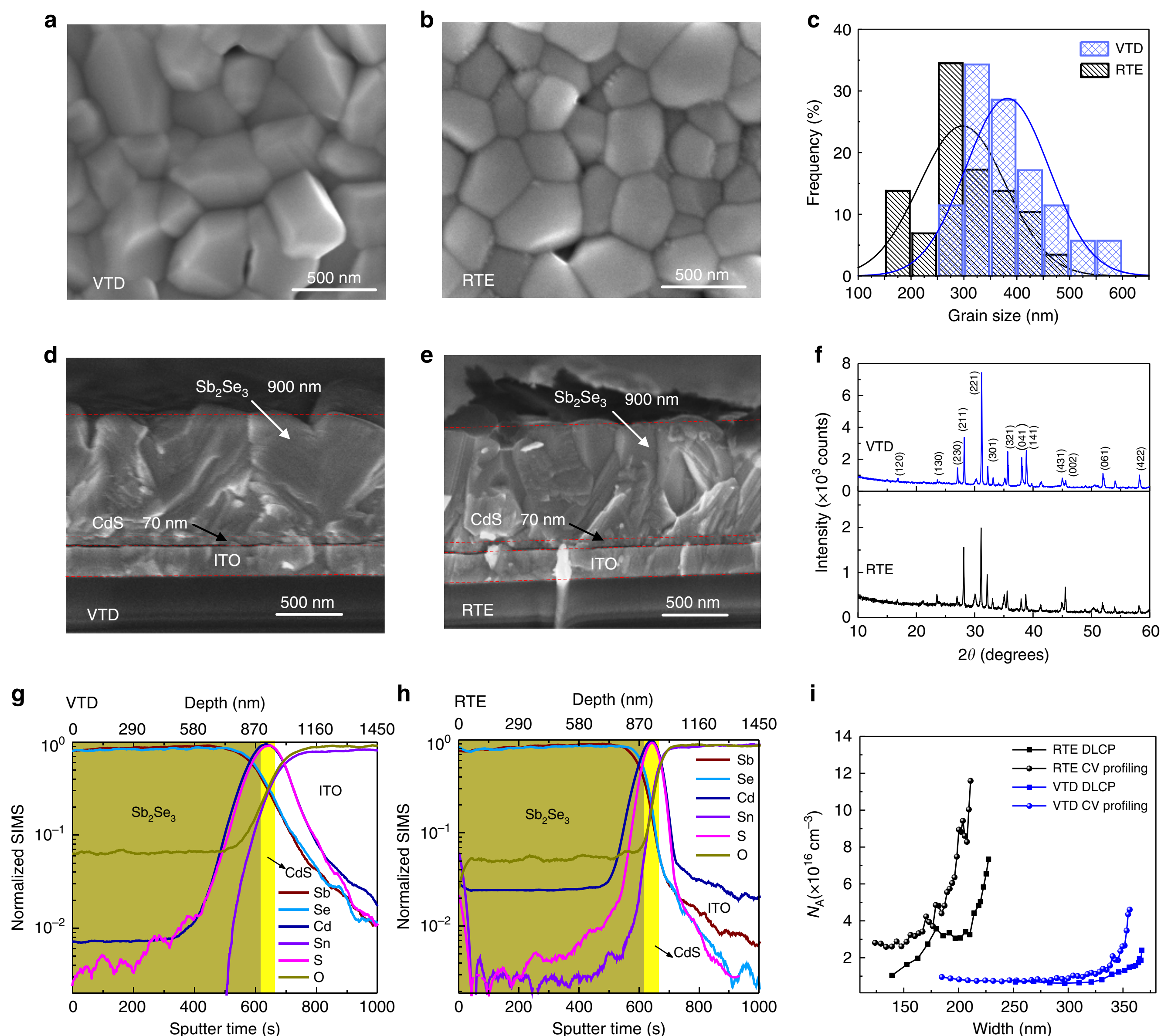

Fig. 4 Characterization of Sb_2Se_3 films and interface analysis of CdS/Sb_2Se_3 devices. SEM top-view images of **a** VTD-fabricated and **b** RTE-fabricated Sb_2Se_3 films. **c** Histogram of grain size in VTD-fabricated and RTE-fabricated Sb_2Se_3 films. Cross-sectional SEM images of **d** VTD-fabricated and **e** RTE-fabricated CdS/Sb_2Se_3 devices. **f** XRD of VTD-fabricated and RTE-fabricated Sb_2Se_3 films. SIMS depth analysis of **g** VTD-fabricated and **h** RTE-fabricated devices. **i** *C-V* profiling and DLCP for VTD- and RTE-fabricated devices

but also enables higher carrier concentration within the absorber layer and therefore wider quasi-Fermi level splitting and improved V_{OC} (VTD 0.42 V vs. RTE 0.39 V).

Morphology and crystallization of Sb_2Se_3 films. We now study the material origin of the improved device performance. The scanning electron microscopy (SEM) top view images of Sb_2Se_3 films deposited on glass/ITO/CdS substrates by VTD and RTE are shown in Fig. 4a, b, respectively. The grains of VTD-fabricated film are obviously larger than that of Sb_2Se_3 film from RTE process. We statistically analyzed the distribution of grain size from the two SEM top view images. Figure 4c depicts the histograms of the grain size. The average grain size of VTD-fabricated film was 382 nm with a standard deviation of 79 nm, whereas the RTE-derived Sb_2Se_3 film had an average size of 297 nm and a standard deviation of 82 nm. The cross-sectional SEM images of Sb_2Se_3 solar cells fabricated by VTD and RTE methods are shown in Fig. 4d, e, respectively. Device structures in both cases were the same: ITO/CdS/Sb_2Se_3/Au. The Sb_2Se_3 layers were compact and well adherent to the CdS with the same thickness of about 900 nm. We compared XRD patterns of the two Sb_2Se_3 layers, measured under identical conditions, as shown in Fig. 4f. Obviously, both films were favorably orientated along [221] direction. However, the XRD intensity of VTD-fabricated film was much stronger than that of RTE-fabricated film, indicating much higher crystallinity was obtained by VTD process. The SEM and XRD results both demonstrate VTD-fabricated Sb_2Se_3 films have larger grains and higher crystallinity compared with RTE-fabricated films. It should be noted that, for RTE-fabricated Sb_2Se_3 film, the distance between evaporation source and substrate was merely 0.8 cm, and the deposition was carried out on 350 °C substrate for 35 s[1, 2], while the corresponding value in the VTD process was 21 cm, 390 °C and 2 min, respectively. Longer traveling distance could increase the collision probability between Sb_xSe_y particles and gas molecules, reduce the momentum of these particles when impinge onto the substrate and hence

decrease the occurrence of nucleation. Less nucleus within the film, accompanied with higher substrate temperature and longer film growth duration, enabled the VTD-derived Sb_2Se_3 film with larger grain size and better grain crystallinity[21].

Interfacial properties of the devices. For all thin film photovoltaic devices with CdS as buffer layer, Cd diffusion at the interface is always observed[32, 33]. To check the Cd diffusion in our devices, we measured their composition distribution by secondary ion mass spectroscopy (SIMS) depth profiling. As shown in Fig. 4g, h, Cd diffusion was observed in both VTD-fabricated and RTE-fabricated CdS/Sb_2Se_3 devices. The deeper Cd diffusion (greater than 200 nm) than that (greater than 100 nm) in RTE-fabricated device was found in VTD-fabricated device. As CdS buffer layer was prepared following identical procedures, we deduced that the different Cd-diffused depth was certainly caused by the different deposition techniques: for VTD process, substrate temperature was about 390 °C and deposition lasted for 2 min, while in RTE process the corresponding values were 350 °C and 35 s, respectively[1, 2]. Because diffusion is driven thermally, higher substrate temperature and longer deposition time resulted in more Cd diffusion in VTD-fabricated device. As we reported before[32], Cd diffusion converted p-type Sb_2Se_3 into n-type, and resulted in a buried homojunction at CdS/Sb_2Se_3 interface. This could reduce the interface defects and recombination at the heterojunction interface[34], being beneficial for device performance.

Therefore, we further measured interfacial defects using capacitance-voltage (C-V) profiling and deep-level capacitance profiling (DLCP) techniques[1, 35, 36]. Generally, the defects density obtained from C-V profiling (N_{CV}) includes the response of free carriers, and bulk and interfacial defects, while the defect density obtained from DLCP measurement (N_{DLCP}) represents the response only from the free carrier and the bulk defects[1, 36]. Thus, we can characterize the defect density at CdS/Sb_2Se_3 interface by the difference between N_{CV} and N_{DLCP}. As shown in Fig. 4i, obviously, the difference between N_{CV} and N_{DLCP} of RTE-fabricated device is much higher than that of VTD-fabricated device, indicating lower defect density at VTD-fabricated CdS/Sb_2Se_3 interface. Because the doping concentration of CdS was much higher than in Sb_2Se_3 film[3, 6], almost all depletion width (W_d) extended in Sb_2Se_3 layer. Here the volume to surface ratio is W_d, the interfacial defect density of RTE-fabricated and VTD-fabricated devices was calculated to be about 2.1×10^{11} cm^{-2} and 2.8×10^{10} cm^{-2}, respectively. The interfacial defect density in VTD-fabricated Sb_2Se_3 solar cell is also much lower than that (1.22×10^{11} cm^{-2}) in RTE-fabricated Sb_2Se_3 solar cell with ZnO as buffer layer[1]. Consequently, we concluded that the promoted interfacial diffusion had effectively reduced interface defects. This is reminiscent of our previous observation that the performance of RTE-fabricated and thermally evaporated CdS/Sb_2Se_3 solar cells always improved when stored in ambient air for a few days[2, 6]. Similar effect has also been demonstrated in CdS/CdTe solar cells that the interfacial diffusion reduced interfacial lattice mismatch and defects, then reduced the current loss and improved device efficiency[33].

Deep defects in VTD- and RTE-fabricated devices. We subsequently investigated the deep defects in CdS/Sb_2Se_3 solar cells fabricated via VTD and RTE processes to demonstrate how the trap-assisted recombination was reduced in VTD-fabricated device. DLTS is a well-accepted powerful tool to investigate defect energy level, type and concentration in thin film photovoltaics[14, 15, 37–40]. It uses the transient capacitance of p–n junction at different temperature as a probe to monitor the changes in charge state of a deep defect center[41]. Traps in the device are filled by carriers through applying a voltage pulse to the device, which changes the capacitance associated with p–n junction of the device[42].

We comparatively analyzed the deep-level defects in VTD-fabricated and RTE-fabricated Sb_2Se_3 films by DLTS. Herein, we adopted DLTS with minority carriers injection (inj-DLTS) to detect both electron and hole traps in Sb_2Se_3 films[37, 38, 40, 43]. As shown in Fig. 5a, during the measurement, a quiescent reverse bias ($V_{reverse}$) was first applied to the junction for forming a depletion width in Sb_2Se_3 layer. Then, a forward pulse voltage (V_{fill}) was applied to fill the traps in the depletion region. If we set $V_{fill} < 0$, the junction was under reverse bias, and there were only holes injected into the depletion region to fill the traps, and only hole traps were detected. If we set $V_{fill} > 0$, under forward bias condition, both electrons and holes were injected into the depletion region, and thus both electron and hole traps could be detected (inj-DLTS)[37, 38, 40].

Here, we take the hole traps as an example to elaborate the change of transient capacitance caused by holes capture and emission (Fig. 5a). Figure 5b shows the corresponding variation of depletion width (W_d) and the process of holes being trapped and emitted, before and after the pulse voltage applied. C_0 represents the steady-state junction capacitance at $V_{reverse}$ bias. When V_{fill} was applied and held for a while, W_d narrowed down to W_{t0-} and the hole trap defects were filled. Once V_{fill} pulse relaxed, W_d broadened to W_{t0+} and capacitance decreased to C_{t0+} instantaneously. W_{t0+} was even larger than W_0 because some holes had been trapped in depletion region. Over the course of time, the trapped holes were gradually and eventually completely emitted from the occupied deep level. Then, W_d shrank to W_0 and the capacitance returned to steady state (C_0). As the state of activated defects was determined by the temperature, a sequence of transient capacitance was thus measured at different sample temperature, and capacitance changes within a time window vs. the different temperatures was sampled as DLTS signal. We took a fixed time window between t_1 and t_2 (Fig. 5a), and then the corresponding hole emission rate e_p can be expressed by Eq. (1):[15]

$$e_p = \frac{\ln(t_2/t_1)}{t_2 - t_1}. \quad (1)$$

As shown in Fig. 5a, the capacitance change within the time window is $\Delta C = C_{t2} - C_{t1}$, which depends on the sample temperature. DLTS signal can be reflected from the variation of $\Delta C/C_0$ with different sample temperatures. Besides, based on the changing of capacitance during the discharging process of traps, the hole traps and electron traps can be differentiated by positive and negative ΔC, respectively.

DLTS results of VTD-fabricated and RTE-fabricated CdS/Sb_2Se_3 devices are shown in Fig. 5c. One negative and two positive peaks were found in both devices, indicating one electron trap (E1) and two hole trap defects (H1 and H2) in Sb_2Se_3 films. The activation energy and capture cross-section of traps can be obtained from Arrhenius plot based on Eqs. (2) and (3):[15, 38]

$$\ln\left(\frac{e_p}{T^2}\right) = \ln\left(\sigma_p \frac{16\pi k_B{}^2 m_p^*}{h^3}\right) - \frac{E_T - E_V}{k_B T}, \quad (2)$$

$$\ln\left(\frac{e_n}{T^2}\right) = \ln\left(\sigma_n \frac{16\pi k_B{}^2 m_n^*}{h^3}\right) - \frac{E_C - E_T}{k_B T}, \quad (3)$$

where e_n and e_p represents electron and hole emission rate, respectively, which can be obtained by Eq. (1); σ_p and σ_n are

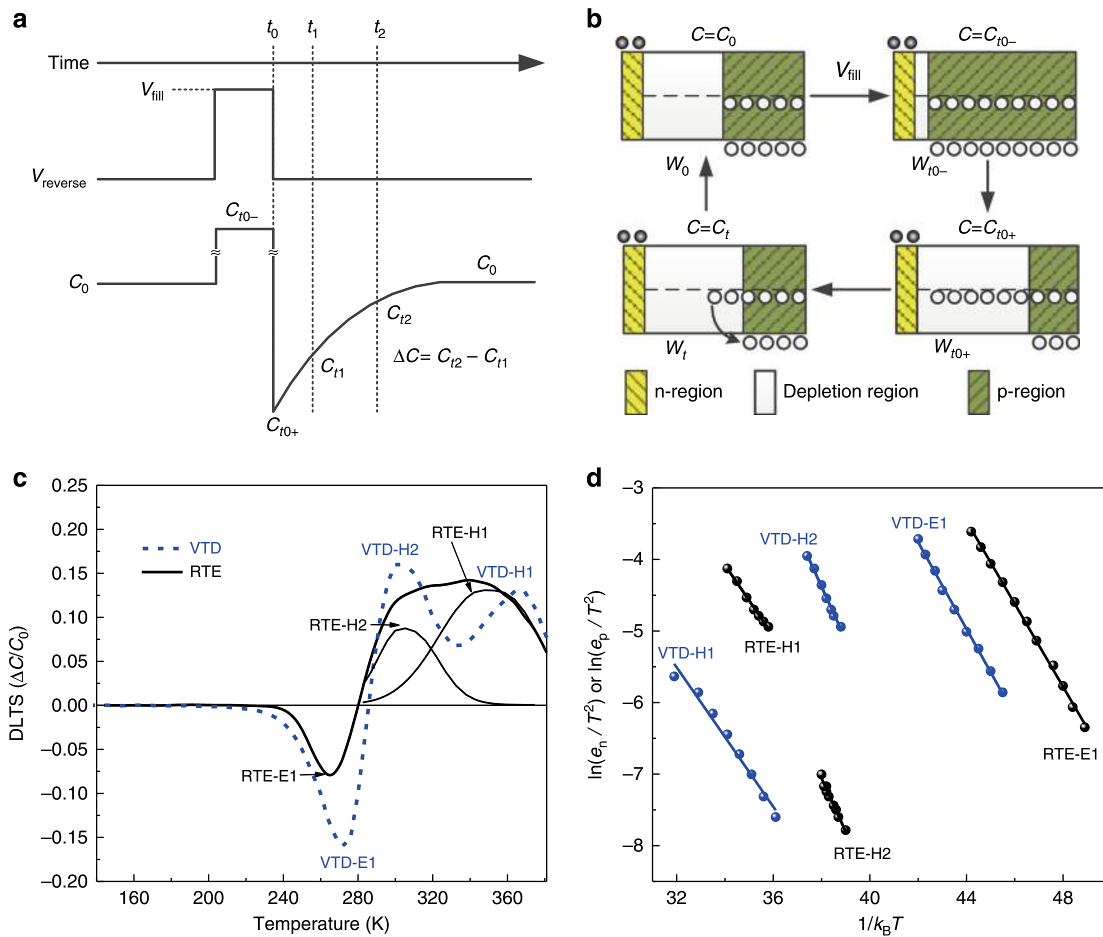

Fig. 5 DLTS analysis of VTD- and RTE-fabricated CdS/Sb_2Se_3 solar cells. **a** Schematic demonstration of the mechanism of DLTS measurement. **b** Variation of depletion width and the process of holes being trapped and emitted during the measurement. **c** DLTS signals of VTD-fabricated and RTE-fabricated devices at $t_1/t_2 = 1$ ms/10 ms. **d** Arrhenius plots obtained from DLTS signals. C_{t0-} and W_{t0-} are the junction capacitance and the depletion width at the moment before pulse voltage ended, respectively. C_{t0+} and W_{t0+} are the junction capacitance and the depletion width at the moment after pulse voltage ended, respectively

capture cross-section of hole and electron traps, respectively, T is the temperature, and k_BT is the thermal energy. In addition, m_p^* and m_n^* respectively represent effective mass of hole and electron, and E_T, E_C and E_V are the energy level of defect, conduction and valence bands, respectively. Figure 5d shows the Arrhenius plot obtained from Fig. 5c, by the varied e (hole or electron emission rate) corresponding to the DLTS peak positions in temperature according to Eqs. (2) and (3). Activation energy ($E_T - E_V$ or $E_C - E_T$) of the trap can be calculated from the slope of $\ln(e_p/T^2)$ or $\ln(e_n/T^2)$ vs. $1/k_BT$ plot, and the capture cross-section could be extracted from the y-intercept. The trap concentration (N_T) can be obtained from the Eq. (4)[15, 39]:

$$N_T = \frac{2\Delta C_{max}}{C_0} N_A, \quad (4)$$

here N_A is the net acceptor concentration in Sb_2Se_3 film, which can be obtained from C-V profiling (Fig. 4i); ΔC_{max} equals to the difference between C_{t0+} and C_0 (Fig. 5a).

Based on the above fitting results and calculation, the defect parameters of VTD- and RTE-fabricated Sb_2Se_3 solar cells are summarized in Table 1. The properties of deep defects in Sb_2Se_3 film are experimentally uncovered. By comparing the activation energies of these trap defects, we find that they are similar in both devices, indicating the same origins of these defects. To investigate whether Cd diffusion affects the DLTS results, we measured the variation of depletion width with the applied bias, as shown in Supplementary Fig. 8. The depletion width of VTD- and RTE-fabricated devices decreased from 430 and 324 nm to 240 and 255 nm with the bias pulse changing from −0.5 V to 0.4 V, respectively. However, the Cd diffusion depths in VTD- and RTE-fabricated Sb_2Se_3 layers are about 200 nm and 100 nm from SIMS results, respectively. Thus, the Cd ions located outside the detected depletion region and had no effect on DLTS result. The defects only originate from the intrinsic Sb_2Se_3.

Table 1 Defect parameters of VTD- and RTE-fabricated Sb_2Se_3 solar cells

Defects	E_T (eV)	σ (cm^2)	N_T (cm^{-3})
VTD-H1	$E_V + 0.48 \pm 0.07$	1.5×10^{-17}	1.2×10^{15}
VTD-H2	$E_V + 0.71 \pm 0.02$	4.9×10^{-13}	1.1×10^{14}
VTD-E1	$E_C - 0.61 \pm 0.03$	4.0×10^{-13}	2.6×10^{14}
RTE-H1	$E_V + 0.49 \pm 0.03$	2.2×10^{-16}	1.2×10^{14}
RTE-H2	$E_V + 0.74 \pm 0.04$	7.7×10^{-13}	2.3×10^{15}
RTE-E1	$E_C - 0.60 \pm 0.02$	1.6×10^{-12}	1.7×10^{15}

In our VTD and RTE facilities, Se vapor is always excess for its higher vapor pressure than Sb and Sb_2Se_3, so the Sb_2Se_3 films are actually slightly Se rich[1, 2]. Our previous ab initio calculation of the intrinsic defects in Sb_2Se_3 has demonstrated that the dominant

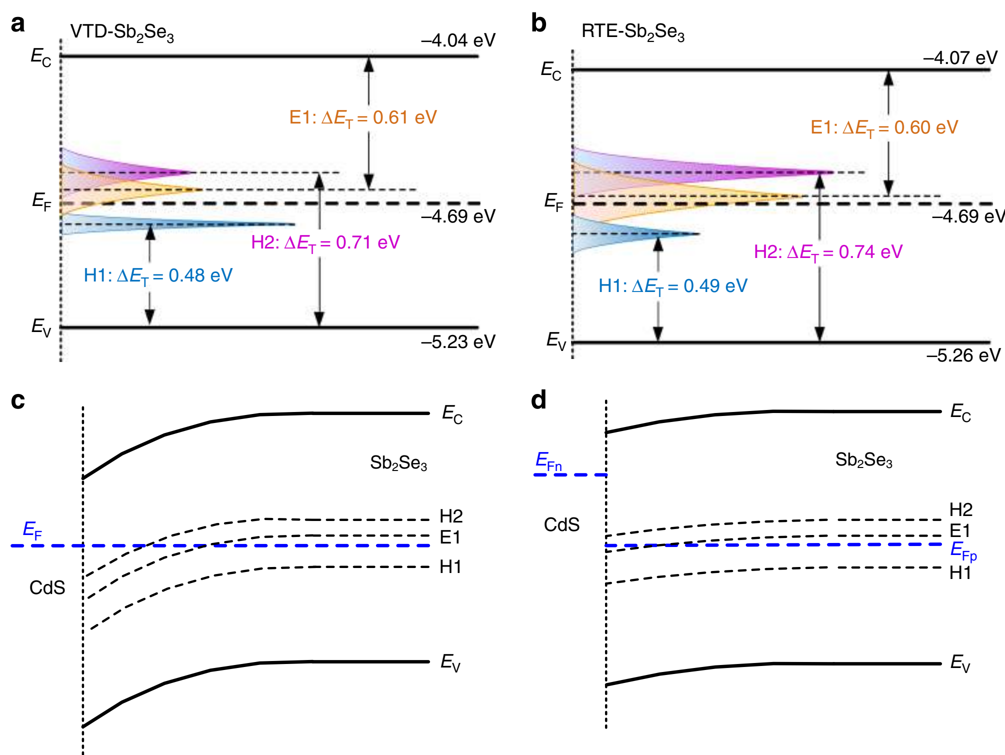

Fig. 6 Influence of defect levels on the CdS/Sb_2Se_3 solar cells. Energy states and defect level of **a** VTD-fabricated and **b** RTE-fabricated Sb_2Se_3 films. Energy band diagrams at CdS/Sb_2Se_3 interface **c** in the dark and **d** under illumination

acceptor defects are antimony vacancy (V_{Sb}) and selenium antisite (Se_{Sb}) defects under Se-rich condition[11]. Therefore, we tentatively attributed H1 and H2 defects to V_{Sb} and Se_{Sb} defects, respectively. As reported by Tumelero et al.[44], the antisite defects dominated the distribution of defects in trichalcogenides due to the similar sizes of the constituent atoms. Our previous simulation also showed that Se_{Sb} and antimony antisite (Sb_{Se}) are acceptor and donor defects, respectively[11]. Consequently, the E1 defect is most likely associated with the formation of Sb_{Se} antisite defects. Interestingly, E1 and H2 always have similar densities with each other in both VTD- and RTE-fabricated samples, which indicate that antisite defect pairs formed in Sb_2Se_3 films, presumably forming [Sb_{Se}+Se_{Sb}] complex. Please also note that using VTD process reduced the density of these antisite defect pairs by more than an order of magnitude (Table 1).

The energy levels of defects in the two samples are depicted in Fig. 6a, b, respectively. Herein, the conduction band, valence band and Fermi levels were obtained from ultraviolet photoelectron spectroscopy (UPS) and Tauc plots by transmission spectra of Sb_2Se_3 films (Supplementary Fig. 9). Clearly, the energy levels of H2 and E1 are above the Fermi level (E_F) in both samples, and H1 is under E_F. To analyze the influence of defects on the photo-generated carrier recombination, energy band and defect energy levels of CdS/Sb_2Se_3 device in the dark and under illumination are depicted in Fig. 6c, d, respectively. Due to thermal equilibrium, the energy band of Sb_2Se_3 bended downward around the hetero-interface, which led to the same Fermi level in CdS and Sb_2Se_3 layers. Under illumination, as depicted in Fig. 6d, the photo-generated electrons were driven into CdS layer, prompting electron quasi-Fermi level (E_{Fn}) to move upward in CdS. Meanwhile the photo-generated holes resulted in the hole quasi-Fermi level (E_{Fp}) shifting downward in Sb_2Se_3 layer. The shift of quasi-Fermi levels is positively correlated with the nonequilibrium carrier concentration. The difference between the two quasi-Fermi levels determines V_{OC} of the solar cell[14].

We now discuss influence of defects in working conditions. The position of E_{Fp} is always dependent on illumination intensity, and Fig. 6d revealed the situation under AM1.5 irradiation. The intersections of E_F and defect levels can be used as boundaries to differentiate whether the defects are charged or not during the shifting of quasi-Fermi level[45]. Clearly, H1 state is under Fermi level and submersed in electrons, so H1 defects always stay inert. In contrast, H2 and E1 defect states are mostly above E_F and they are active in trapping holes and electrons, respectively. These trapped photo-generated carriers would most probably contribute to recombination loss. Furthermore, the energy levels of H2 and E1 are located near to the midgap, which significantly increase the recombination possibility of photo-generated carriers[46]. Therefore, the H2 and E1 are the dominant defects that influence the shift of quasi-Fermi levels and trap-assisted recombination, and then the V_{OC} and J_{SC} of the solar cells. Moreover, due to the higher defect density of H2 and E1 than carrier concentration (about 10^{13} cm^{-3}) in Sb_2Se_3 layer[3], the E_{Fp} would be more likely to be pinned near E1 and H2 levels. Obviously, both of H2 and E1 have lower defect density in VTD-fabricated sample, which could lead to relatively larger E_{Fp} downshifting and suppressed trap-assisted recombination, explaining the better V_{OC} and J_{SC} in VTD-fabricated Sb_2Se_3 solar cells.

Discussion

We have demonstrated that VTD technique can greatly enhance the performance of Sb_2Se_3 thin film solar cells by increasing the crystallinity of Sb_2Se_3 films, reducing the interface and bulk defects in the devices, and prolonging the carrier lifetime. Specifically, we believe the advantages of VTD over RTE are based on two features. First, the substrate temperature in VTD process can be regulated independently by changing the distance between source and substrate, thus permitting higher substrate temperature (VTD 390 °C vs. RTE 350 °C). The higher substrate temperature resulted in improved crystallinity (threefold enhancement in XRD peak intensity) and

average grain size (VTD 382 nm vs. RTE 297 nm) of Sb_2Se_3 films. Second, the slower deposition of Sb_2Se_3 films (VTD 2 min vs. RTE 35 s) enables less film imperfection (Se_{Sb}+Se_{Sb} antisite complex and V_{Sb} vacancy), as reflected by the reduced bulk defect density (VTD 10^{14} cm^{-3} vs. RTE 10^{15} cm^{-3}) and interfacial defect density (VTD 2.8×10^{10} cm^{-2} vs. RTE 2.1×10^{11} cm^{-2}), and increased carrier lifetime (VTD 1339 ps vs. 1149 ps). Overall, all these advantages facilitated the fabrication of high-quality Sb_2Se_3 films, leading to increased V_{OC}, J_{SC} as well as FF (VTD: 0.42 V, 29.9 mA cm^{-2}, 60.4% vs. RTE: 0.39 V, 25.3 mA cm^{-2}, 56.4%). The champion device achieved the efficiency record 7.6%, much higher than SnS, Cu_2O and FeS_2 solar cells which have been studied for many years[47–49]. The fabrication of record efficiency Sb_2Se_3 solar cells employing vapor transport deposition, a technique with proven high turn-around and low cost for commercial CdTe solar cells, further strengthens the great potential of our Sb_2Se_3 thin film photovoltaics.

On the other hand, we find that the deep defect density in the best-performing Sb_2Se_3 solar cells is about 10^{14} to 10^{15} cm^{-3}, which is much higher than that (10^{11} to 10^{13} cm^{-3}) in CdTe solar cells[50]. These abundant deep defects could pin the quasi-Fermi level near H2 and E1 defect states, which provides a plausible explanation for the low V_{OC} observed in all Sb_2Se_3 solar cells reported so far, despite various device configuration and film preparation methods have been explored[1–12, 19, 32, 51]. We suggest that future research on tightly controlling Se and Sb components in the vapor, their strictly stoichiometric condensation into the film and the growth of highly crystalline film should be carried out to minimize these deep defects and maximize device performance.

In summary, we have obtained the superstrate CdS/Sb_2Se_3 thin film solar cell with a certified efficiency of 7.6% (V_{OC} of 0.42 V, J_{SC} of 29.9 mA cm^{-2} and FF of 60.4%), which was promoted by the VTD-fabricated Sb_2Se_3 absorber layer. Compared with the previous reports on Sb_2Se_3 solar cells[1–6, 8–12, 19, 20], VTD process reduced the density of deep defects and subsequently suppressed trap-assisted recombination in Sb_2Se_3 films, resulting in longer carrier lifetime and better device performance. These encouraging results highlight the potential of Sb_2Se_3 solar cells for high-efficiency photovoltaic devices.

Methods

Sb_2Se_3 solar cell fabrication. All solar cells were deposited on ITO (In_2O_3:Sn) transparent conductive glass supplied by Kaivo, with sheet resistance of 6.5 to 6.8 ohm sq^{-1}, transmittance of 78.8 to 79.6% and ITO thickness of about 200 nm. The ITO substrates were cleaned using detergent, acetone, isopropanol, ethanol and deionized water in sequence. CdS buffer layer was deposited by chemical bath deposition[7]. CdS layers were treated with H_2O_2 (30 wt%) and 20 mg ml^{-1} $CdCl_2$ (Aladdin) absolute methanol solution by spin coating, respectively, baked on the hotplate at 400 °C for 5 min in air ambient and then cooled down naturally. Following that, VTD process was used to deposit Sb_2Se_3 films. As shown in Fig. 1a, 0.25 g Sb_2Se_3 powder (99.999% purity, Jiangxi Ketai) was put into a quartz crucible and placed in the center of VTD system (a single temperature zone tube furnace, MTI, Hefei, China). The ITO/CdS substrate was immobilized on a graphite support and then placed at the right end of the quartz tube. Substrate temperature was regulated by changing the distance between substrate and the center of the heater. Vacuum was pumped by a mechanical pump and the stabilized chamber pressure was controlled by varying the ventilation power of the pump. The heating temperature of VTD system was raised to the targeted evaporation temperature with a ramp rate of 20 °C min^{-1} and kept for 2 min to obtain a desired Sb_2Se_3 film thickness. Then, we turned off the power to stop the deposition and finally took the sample out when it was naturally cooled down to about 100 °C. After that, gold back-contact electrodes (0.091 cm^2 area, 100 nm thick) were evaporated by the resistance evaporation thin film system (Beijing Technol Science) under a vacuum pressure of 5×10^{-3} Pa. To optimize the quality of Sb_2Se_3 film and the performance of device, we systematically investigated the evaporation temperature of VTD system from 480 to 520 °C, the pressure from 2.8 to 5.3 Pa and the substrate distance from 19 to 23 cm. When the evaporation temperature was investigated, the pressure and the distance were set as 4 Pa and 22 cm, respectively. The optimized evaporation temperature and the distance of 22 cm were adopted for pressure investigation, and then the optimized temperature and pressures were used to investigate the substrate distance.

Material characterization. Material and device characterization are similar to previous report[1, 2, 11]. XRD of Sb_2Se_3 films was performed using a Philips X'Pert Pro diffractometer with Cu Kα radiation ($\lambda = 1.54$ Å). SEM measurement was carried out with FEI Nova Nano SEM450. SIMS (IMS-4f, CAMECA instruments) was used to investigate the element distribution along the depth in the devices. UPS was used to investigate the Fermi level and valence band of Sb_2Se_3 films. Experiments were performed using a He I (21.21 eV) gas discharge lamp in a Kratos AXIS-ULTRA DLD-600W x-ray photoelectron spectroscopy measurement system and recorded at 0 V samples bias in an ultrahigh vacuum chamber. The surface of Sb_2Se_3 films was etched before UPS measurement. Ultraviolet–visible near-infrared transmission spectra (Perkin Elmer Instrument, Lambda 950 using integrating sphere) were measured to determine the bandgap of Sb_2Se_3 films.

Device characterization. *J-V* curve and PCE of the champion CdS/Sb_2Se_3 solar cell was independently measured by National Institute Metrology (NIM), using the Class AAA Solar Simulator with double-light source (SAN-EI ELECTRIC, XHS-2350M1, 100 mW cm^{-2}, AM1.5 illumination) in air ambient at room temperature. A metal mask was used to define the area of incident light. The area (9.099 mm^2) was also measured by NIM. The light intensity was calibrated by a standard Si-reference solar cell. A Keithley 2400 Source Meter was used to acquire *J-V* data. The external quantum efficiency of solar cells was measured using the light source generated by a 300 W xenon lamp of Newport (Oriel, 69911) and then split into specific wavelengths by a Newport Oriel Cornerstone 130 1/8 Monochromator (Oriel, model 74004). A standard silicon detector (70356_70316NS_455) was used for the calibration. The capacitance-voltage (*C-V*) profiling and DLCP data were measured using Keithley 4200. *C-V* measurements were performed at room temperature in an electromagnetic shielding box at a frequency of 100 kHz and a.c. amplitude of 30 mV. The d.c. bias voltage was scanned from −1.0 V to 0.3 V. DLCP measurements were performed with a.c. amplitude from 0.02 V to 0.14 V and d.c. bias voltage from −0.2 V to 0.2 V. DLTS measurement were performed by Semetrol DLTS system (Semetrol, LLC, USA) on the two typical devices. The temperature was scanned between 100 and 380 K, at a heating rate of 2 K min^{-1}. The reverse bias voltage was −0.5 V. The filling pulse voltage and width were 0.4 V and 1 ms, respectively. At every scanning temperature point, the transient capacitance was measured 20 times for obtaining the average value. Transient absorption spectroscopy was pumped by 500 nm laser pulses (Light Conversion, Pharos, 350 fs duration pulses, 5 kHz repetition rate) and probed at 940 nm. The time delay was adjusted by changing the path length of the probe.

Data availability. The data that support the findings of this study are available from the corresponding author on request.

Received: 22 December 2017 Accepted: 19 April 2018
Published online: 05 June 2018

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Acknowledgements

This work was financially supported by the Major State Basic Research Development Program of China (2016YFA0204000), the National Natural Science Foundation of China (61725401, 91433105 and 51602114), the Special Fund for Strategic New Development of Shenzhen, China (JCYJ20160414102210144), and the Project funded by China Postdoctoral Science Foundation (2017M622445). The authors thank the Analytical and Testing Center of HUST and the facility support of the Center for Nanoscale Characterization and Devices, WNLO. We also thank J. Luo and J. Li for X-ray diffraction measurements, Q. Hu for his help in SEM measurements, and Y. Zhong and S. Sun from Zhengzhou University for their help in DLTS measurements.

Author contributions

X.W. and J.T. conceived the idea, designed the experiments and analyzed the data. X.W., C.C., and S.L. carried out the device optimizations. Y.Z. prepared the gold electrodes. X. W. carried out most of material and device characterizations. L.G. carried out the TA characterization. C.C., S.L., K.L., W.C., R.K., C.W., J.Z. and G.N. assisted in data analysis. X.W. and J.T wrote the paper. All authors commented on the manuscript.

Additional information

Supplementary Information accompanies this paper at https://doi.org/10.1038/s41467-018-04634-6.

Competing interests: The authors declare no competing interests.

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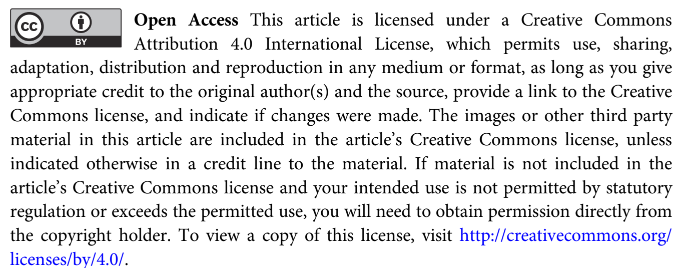

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