Variability and Ripple Analysis of an On-Chip All-Digital AVS System

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Abstract— **Adaptive voltage scaling (AVS) brings energy savings by dynamic adaptation of the operating conditions to process corners and environmental variations. We investigate here the opportunity to use a switched-capacitor converter and a ring oscillator as parts of the AVS unit. The ring oscillator purposes are both monitoring of the circuit delay and generation of its clock signal. We show that jitter induced by the voltage ripple of a switched-capacitor converter is mitigated by averaging effect if the ripple frequency is at least the circuit operating frequency. Simulations on the AVS unit show an efficiency of 70% for the voltage conversion.**

Keywords- CMOS integrated circuit, low-power design, variability, adaptive voltage scaling, clock generation.

I. INTRODUCTION

Electronics has become ubiquitous in human life. In the last years, research efforts were mainly focused on reaching higher and higher speed performances. However, some emerging applications change this trend. Wireless sensor networks, for instance, allow a lot of sensors to communicate with each other. They are used in applications as various as human or environmental monitoring, and object tracking [1-2]. A node of such a network does not need a high computing power. On the other hand, battery replacement can be a concern when the number of nodes is increased or when the sensors are hard to reach. Therefore, reducing the power consumption of circuits in advanced technology is today a hot topic. Unfortunately, variability is becoming more important as CMOS technology scales down, leading to higher guardband on the supply voltage and therefore to power consumption overhead.

Fig. 1a shows a typical organization of management units for digital circuits. A margin is taken either on V_{DD} or on the clock frequency f_{CLK} to ensure that the critical paths of the circuit always meet the timing constraints. Indeed circuits can face die-to-die process, voltage and temperature (PVT) variations, ripple on the supply voltage, clock jitter and local within die (WID) variations. If that architecture is suitable for high performance processors, it may not be the case for the new low-power circuits. Indeed, as the dynamic power decreases quadratically with the supply voltage, V_{DD} is aggressively scaled down in low-power circuits. This leads to a higher sensitivity to PVT and WID variations. The architecture shown in Fig. 1a may thus lead to unreasonable margins inducing energy waste.

This motivated the development of other kinds of power management unit. They are based on the fact that we do not actually care about the exact V_{DD} value of the circuit as long as it works at the target frequency and as its consumption is kept in the power budget. A new solution is thus to adapt dynamically the supply voltage to the operating conditions. This is known as adaptive voltage scaling (AVS) technique [3-7]. With an AVS system it is interesting to merge the clock and power management feedback loop into a single loop as shown in Fig. 1b. As we try to build an AVS system we face a large choice of implementation possibilities: logically adjustable frequency divider [3] or voltage controlled ring oscillator [4] for the clock generation, bang-bang [7], PID [5] or sliding mode [6] controller, switched buck [6], LDO, or switched-capacitor converter. Particularly switched-capacitor converters are promising for the voltage conversion in low-power applications [8-9]. Unfortunately these converters induce ripple whose magnitude is inversely proportional to the switching frequency and proportional to the transfer capacitors over load capacitor ratio [10]. As on-chip load capacitance is limited by die area concern, and as load power is proportional to switching frequency and transfer capacitors, ripple cannot be avoided. Finally, the frequency loop may be easily achieved with a ring oscillator controlled by the converter output voltage, but it may be sensitive to noise and ripple present there. In this paper, we investigate the feasibility of coupling such a ring oscillator with switching converters.

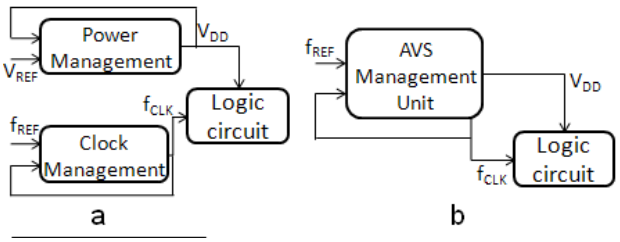

Figure 1. (a) Conventional management unit architecture for a digital circuit. (b) AVS architecture for low-power circuits.

This paper is organized as follows. Impact of PVT and WID variations is studied in Section II. Section III describes the proposed management unit. Simulation results and their analysis are given in Section IV.

II. IMPACT OF PVT VARIATIONS ON CIRCUIT DELAY

Let us first take a look at the sensitivity of a digital circuit to PVT variations. Table 1 shows two examples of low-power circuits operating conditions and power consumption [11-12]. SPICE simulations have been performed on 65nm low-power

TABLE I. TYPICAL APPLICATION KEY FIGURES.

Typical application	A: Mobile processor (Low-Power)	B: Wireless Sensor Node (Ultra-Low-Power)
Consumption	2W	100µW/MHz
Operating Voltage	1.2V	0.65V
Crystal oscillator frequency	32MHz	32kHz
Critical path depth	20FO4	50FO4
Main clock frequency	1GHz	10MHz

CMOS industrial models to extract the sensitivity of these digital circuits to PVT variations.

Simulated circuits are critical path replicas (CPRs) of low-power logic. They are made of inverters chains with 4 inverters connected to the output of each node (FO4). Circuit A represents a critical path of mobile processors for low-power applications such as smartphones. It comprises 20 stages (20FO4 chain) powered at 1.2V. A second circuit, called circuit B, made of 50 stages (50FO4 chain) with a low 0.65V V_{DD} represents ultra-low-power processors for e.g. wireless sensors nodes. Critical path depth of circuit A is lower because pipelining in such processors is more important. Fig. 2 shows the delay changes of these chains for temperature, and voltage variations with extreme process corners. For circuit B, the delay increases by a factor 15 at low temperature [13]. This leads to the needs of high margin on the supply voltage in order to ensure that the circuit is able to work under each temperature condition. At 1.2V the delay of the circuit A is less dependent to PVT variations. However the delay still varies by a factor 2.

A 500-run Monte Carlo simulation has been performed to extract the impact of WID variations on the delay of the circuits. Results are shown on Fig. 3. The circuit B has a ratio σ/µ of 5.5% whereas it is only 2% for the circuit A. Again circuit B exhibits higher sensitivity to local WID variation. This is because the supply voltage is closer to the threshold value. This leads to very high sensitivity to WID V_T variations, although this effect is mitigated by averaging between each stages of the long critical path.

III. PROPOSED MANAGEMENT UNIT.

The proposed architecture of AVS unit is composed of three main parts presented in Fig. 4. The control logic block generates the signals to drive the DC-DC converter. This converter steps down the voltage from the battery to a lower level. It supplies both the circuit and a critical path replica which generates the clock signal used by the circuit. The clock is also sent as a feedback to the control logic block.

A. Control logic

AVS controllers have to ensure that the output voltage range is wide enough to always be able to reach the minimum voltage value. They also have to guarantee robustness and fast response time of the system to variations in operating conditions. A simple controller has been designed for test purposes of the converter and ring oscillator. First a counter

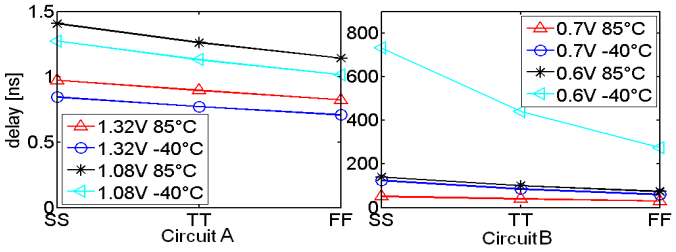

Figure 2. Delay time of the circuits A and B under varying corners (Slow Slow, Typical Typical, and Fast Fast MOS), voltage and temperature conditions.

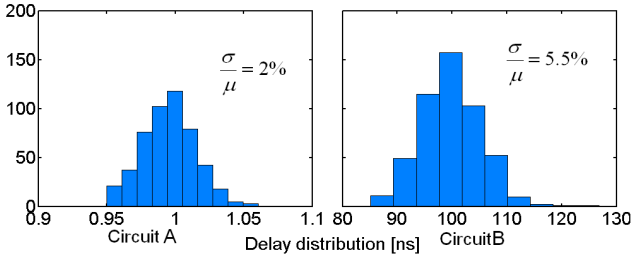

Figure 3. Delay distribution of the circuits A at 1.2V and B at 0.65V V_{DD}, typical corner and 25°C temperature (500-run Monte-Carlo simulation).

serves as a frequency comparator. The counter is enabled when the low frequency real time clock signal (RT_{CLK}) is low. It is increased on each rising edge of the critical path replica clock. When the RT_{CLK} goes up, the count result is transmitted to the regulator and the counter is reset. If the result of the counter is lower than a reference value then a control signal is increased. In the same way, if the result is higher than the reference value the control signal is decreased. However, in order to avoid unwanted oscillations on the output voltage a hysteresis ensures that if f_{CLK} is close enough to the target frequency, no change is applied to the control signal. Finally a decoder block converts the control signal into driving signals for the converter unit. This controller is made of 260 logic cells.

B. Voltage converter

Conventional converters used in AVS are buck converters with pulse width modulation control [4-6]. These converters toggle the output voltage between V_{DD} and GND. This voltage is then filtered with passive components like capacitors and inductors [6]. Linear regulators can be used either to filter the voltage ripple produced by a switching converter or to deliver the output voltage directly from the battery. However, they exhibit linear losses proportional to the V_{OUT}/V_{IN} ratio.

Switched-capacitor converters have been proposed as a new alternative for applications with low-power requirements [8-9]. Their advantage is that they do not use any inductor. In advanced CMOS technology nodes, capacitors are more compact and have better quality factor than inductors. It is therefore possible to avoid the use of external passive components, which allows a reduction of the fabrication costs. A switched-capacitor converter supplies the output voltage of the proposed AVS unit. An oscillator generates a clock which serves as driving signals for the capacitor networks. In order to adjust the output voltage, the frequency of the oscillator can be

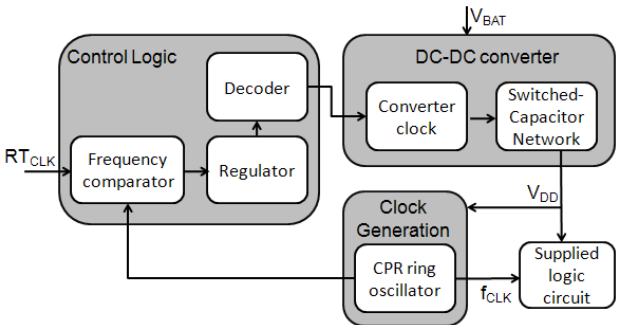

Figure 4. Block diagram of proposed power management unit.

modified. A higher frequency leads to a higher output voltage and inversely. The frequency of the converter clock is selected with the driving signals sent by the decoder. The output voltage of the switched-capacitor converter is supplied to the circuit and to the CPR ring oscillator of the clock generation block. No voltage reference is needed as the converter is only driven by the frequency feedback loop.

C. Clock generation

In most applications, the clock generation unit uses a stable crystal oscillator as input. However, the crystal clock is slower than the targeted operating f_{CLK} frequency. Therefore a PLL is used to multiply the crystal frequency. With this solution the dynamic performances of the circuit are constant and cannot be tuned. AVS systems with a PLL need to monitor on chip if a timing failure occurs at operating voltage [14]. Extra circuitry on the critical paths is needed for the monitoring and the data recovery in case of failure.

The proposed clock generation unit is created from a critical path replica (CPR) based on logic gates representative of the supplied circuit. The CPR is connected in a ring oscillator fashion and designed to match the delay of the critical paths of the supplied circuit. Moreover, the CPR can physically be located inside this circuit to experience similar PVT corners. This way the CPR differs from the actual critical paths only by WID variations.

IV. SIMULATION RESULTS

Simulations have been performed in order to quantify the impact of an internally generated clock in both typical applications presented in Table 1. As presented in Section III, the clock is created from a ring oscillator supplied by the switched-capacitor converter output voltage. SPICE simulations have been performed with models of an industrial 65nm low-power technology.

First, the ripple shape on the output voltage of the switched-capacitor converter has been extracted. The ripple depends on the switching frequency of the converter. A higher frequency induces a lower ripple magnitude as charges are transferred more frequently to the output. The ripple has been added to the supply voltage of the CPR ring oscillator. The 50F04 inverters chain of circuit B is also supplied with this voltage as shown in Fig. 5. It mimics a critical path of an ULP circuit. Its input is the signal generated by the CPR ring

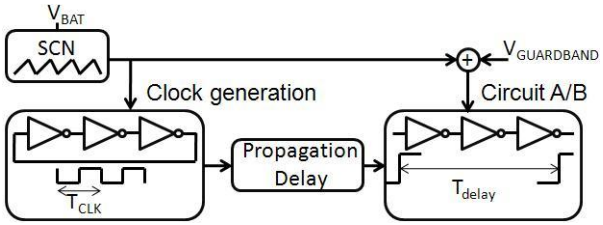

Figure 5. Simulated circuit: calculation of the guardband needed to compensate ripple on the supply voltage .

oscillator. Finally we measured the delay of this inverter chain in the worst case (i.e. with the highest frequency of the CPR ring oscillator) for varying propagation delays between the CPR ring oscillator and circuit B. Fig. 6 shows the V_{DD} guardband needed on the inverter chain to ensure that its delay is shorter than the clock period generated by the ring oscillator. The 25mV ripple at 1MHz frequency shows that as the delay increases the guardband needed increases as well. This is because the CPR ring oscillator in the worst case operates with an average higher supply voltage than the logic circuit. The average voltage difference increases as the clock propagation delay gets higher. Eventually for long delays the clock propagation delay almost matches the ripple period and the average voltage difference decreases. It decreases faster than it rises due to the ripple shape of a switched-capacitors converter. The maximum V_{DD} guardband is smaller than the ripple magnitude thanks to the averaging of the supply voltage during a clock cycle. At higher frequency the ripple magnitude is lower. Additionally the averaging effect has more impact thereby reducing the ratio of maximum V_{DD} guardband over ripple amplitude. Let us note that for intermediate ripple frequency of 5MHz and a short clock propagation delay the V_{DD} guardband required may be higher than for lower frequency ripple. Indeed the triangular shape of V_{DD} guardband gets symmetric. This is caused by the averaging effect becoming more important, and therefore the lost of the benefit of a slowly decreasing voltage.

Fig. 7 shows the V_{DD} guardband required in the case of a management unit using a PLL in combination with a fixed voltage reference and of the proposed AVS management unit. Without AVS, for both circuits A and B, an extra margin around 20% of V_{DD} has to be taken in order to compensate the PVT variations leading to 44% of extra dynamic power costs ($\approx V_{DD}^2$). On the other hand a clock generated from a ring oscillator suffers from WID variations. Extra margin must be taken to ensure that the timing of this ring is slower than the delay of each critical path of the circuit. For the circuit A, this leads to a 50% higher WID contribution to the V_{DD} guardband than for an ideal clock generated with a PLL. For the circuit B, thanks to averaging of the WID variations in a longer chain, the increase is only of 33%. Eventually the ripple due to switching converters is generally considered as loss because the supply voltage has to be increased by half the ripple magnitude to ensure that the supply voltage never drops under a minimum value. As shown on Fig. 6 this is not the case with a clock generated from a ring oscillator. Indeed if the ripple frequency is at least the same as the operating frequency, the requested

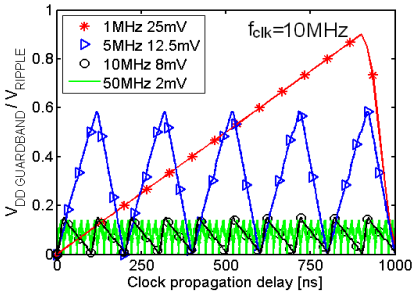

Figure 6. Minimum ratio V_{DD} Guardband over V_{RIPPLE} to balance clock jitter induced by supply voltage for circuit B with typical condition at 25°C.

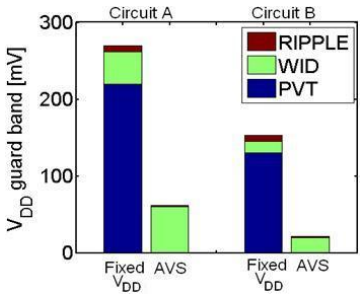

Figure 7. Total V_{DD} guardband for safe operation.

V_{DD} guardband drops below 20% of the ripple magnitude thanks to averaging of the supply voltage over a clock cycle.

Fig. 8 shows the regulated output voltage and frequency of the proposed management unit for an ultra-low-power typical application (circuit B) as presented in Table 1. At each clock cycle of the crystal clock RT_{CLK}, the output voltage is here lowered. The ring oscillator clock frequency is therefore lowered until the desired 10MHz frequency, corresponding to a count result of 50 is almost reached. When the error on the frequency counter is lower or equal to 4 no more change is applied to the control signals until the error increases again. The converter output takes 2µs to adapt to a change of control signal. This is due to charging time of its output capacitor. Before the regulation of the output voltage the circuit may operate under a higher or lower frequency. However as the supply voltage is also higher (resp. lower) at that time no timing violations occurs. Simulations give an efficiency of 70% for the switched-capacitor converter with V_{BAT} of 1.5V and 1mW load.

V. Conclusion

Adaptive voltage scaling (AVS) allows a cancellation of the PVT-induced V_{DD} guardband as observed on two 65nm low-power circuits. In more aggressive technology nodes AVS will be of prime importance due to higher sensitivity to PVT variations. However, its implementation can become quite complex. In this paper we show that the clock generation for AVS with switched-capacitor converter can be designed with a simple ring oscillator with the same delay as the critical paths. The jitter on the ring due to V_{DD} ripple is mitigated by averaging effect if the supply voltage is shared by the ring oscillator and the supplied circuit. Indeed, if the ripple frequency is at least the same as the circuit operating

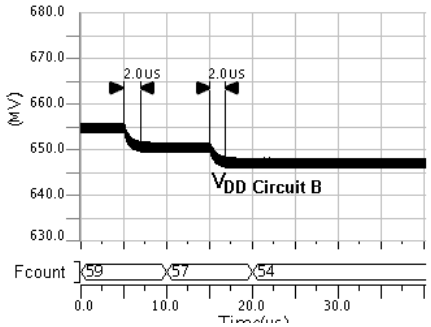

Figure 8. Transient simulation of the AVS loop regulating the output frequency (f_{COUNT} target=50±4) with V_{BAT}=1.5V, typical corners and 25°C.

frequency, averaging reduces the required V_{DD} guardband to less than 20% of the ripple magnitude which is negligible when compared to the impact of WID variations.

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