Variation-sensitive Monitor Circuits for Estimation of Die-to-Die Process Variation

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***Abstract*—We propose a set of variation-sensitive ring oscillators (RO) to estimate Die-to-Die process parameter variation. ROs are designed to have different sensitivity to each parameter variation. A method suitable to estimate variation from different ROs is proposed. We have fabricated test chip and successfully estimated process parameter variation. Variation results are correlated with that in Process Control Module data.**

I. Introduction

As the scaling of Silicon CMOS process technology progresses, variation in transistor performance has been becoming serious problem. In 65nm process and beyond, this variability plays a major role in chip performance. To improve yield under PVT (Process, Voltage and Temperature) fluctuation, worst case design methodology is being followed which results in suboptimal chip performance [1]. As variation increases with every new process node and impact of variation increases under low supply voltage operation, we are facing a serious problem that is how to get maximum benefit from the future nodes. A solution to this scenario can be to tune chip performance in post-silicon. Adaptive techniques such as Adaptive Body Bias (ABB) and Adaptive Supply Voltage (AVS) have been proposed to reduce design margin and control chip performance [2], [3].

Variation in CMOS transistor performance can be divided into die-to-die (D2D) and within-die (WID) variation. As the technology scaling continues, WID variation is becoming more significant [4]. However, WID variation is mainly random and thus its impact gets reduced by the number of stages. On the other hand, D2D variation affects the performances of all transistors in a chip in the same direction (fast or slow) and therefore, D2D variation plays major role in determining chip performance such as leakage current, frequency etc. Major of the D2D Variation in CMOS transistor performance are mainly due to MOS gate length and threshold voltage variation [5]. For fine tuning of chip performance using adaptive techniques, on-chip measurement of process parameters such as threshold voltage and gate length are needed.

Many of the monitor circuits proposed so far to monitor process variation use either device arrays [6] or op-amps [7] and thus require huge area and measurement time that makes them unsuitable for on-chip parameter estimation. A method to calculate the saturated current of each MOS transistor is also proposed [8]. But, to compensate chip performance we need to know the variation of individual process parameter. Because of easy implementation and fast on-chip measurement RO is a good choice for this purpose [9]. But, RO frequency is affected by many process parameter variations simultaneously and thus it is difficult to extract single parameter variation. This paper proposes a set of variation-sensitive ROs to estimate D2D process variation from on-chip measurement values. We fabricate test chip in 65nm process and are able to estimate variation of each process parameter from measured values. Our estimation results are well within the SPICE corner model and correlated with that in PCM data.

The remainder of this paper is organized as follows. In section II, an estimation method to extract process parameter variation is proposed. In section III, some design techniques to realize variation-sensitive ROs is demonstrated. In section IV, test chip structure and measurement results are discussed. Estimation results and their validation are also discussed here. Finally, section V concludes our discussion.

II. Proposed Estimation Method

In order to estimate process parameter variations simultaneously, an estimation method is needed. We propose an estimation method which combines circuit technique and transistor model for estimation. Monitor circuits suitable for this method will be discussed in section III.

A. RO Frequency Model

In this work, we focus on the estimation of D2D variation in three key parameters of pMOS threshold voltage (V_{THP}), nMOS threshold voltage (V_{THN}) and gate length (L). Suppose ΔV_{THP}, ΔV_{THN} and ΔL are D2D variations of those parameters to be estimated and Δf is the corresponding frequency shift that we can measure. If ΔV_{THP}, ΔV_{THN} and ΔL are small, those variations can be related in a linear equation as shown in Eq. (1) where k_{P}, k_{N} and k_{L} are sensitivity coefficients.

$$\Delta f = f_{\mathrm{M}} - f_{\mathrm{Ref}} = k_{\mathrm{P}}\Delta V_{\mathrm{THP}} + k_{\mathrm{N}}\Delta V_{\mathrm{THN}} + k_{\mathrm{L}}\Delta L \quad (1)$$

Here, f_M is measured frequency and f_{Ref} is reference or nominal frequency. We can get f_{Ref} by SPICE simulation

using RC extracted netlist from layout. In order to cancel within-die random effect, RO with large number of stages or average value from many ROs should be used. Sensitivity coefficients can be calculated from SPICE simulation. RC extracted netlist should be used because parasitic capacitances affect frequency sensitivity.

B. Estimation Procedure

In Eq. (1), there are three unknown parameters. So, at least three equations are needed to extract variation of these three unknown values. The three equations can be derived from three ROs whose sensitivity vectors form a non-singular matrix and have small condition number. The amount of variation of each process parameter will be calculated by solving Eq. (2).

$$\vec{V} = \mathbf{S}^{-1}\vec{F} \tag{2}$$

where

$$\vec{V} = \begin{pmatrix} \Delta V_{\mathrm{THP}} \\ \Delta V_{\mathrm{THN}} \\ \Delta L \end{pmatrix}, \mathbf{S} = \begin{pmatrix} k_{\mathrm{P1}} & k_{\mathrm{N1}} & k_{\mathrm{L1}} \\ k_{\mathrm{P2}} & k_{\mathrm{N2}} & k_{\mathrm{L2}} \\ k_{\mathrm{P3}} & k_{\mathrm{N3}} & k_{\mathrm{L3}} \end{pmatrix}, \vec{F} = \begin{pmatrix} \Delta f_1 \\ \Delta f_2 \\ \Delta f_3 \end{pmatrix} \tag{3}$$

Here, $\vec{V}$ is the vector for the variations of V_{THP}, V_{THN} and L. $\mathbf{S}$ is the sensitivity matrix and $\vec{F}$ is the vector for the frequency shift from the nominal value. $(k_{\mathrm{P1}}, k_{\mathrm{N1}}, k_{\mathrm{L1}})$, $(k_{\mathrm{P2}}, k_{\mathrm{N2}}, k_{\mathrm{L2}})$ and $(k_{\mathrm{P3}}, k_{\mathrm{N3}}, k_{\mathrm{L3}})$ are sensitivity vectors for three ROs. By considering the effects of other parameters and the error in the measurement, the vectors should separate from each other sufficiently.

Solving Eq. (2) may not give us accurate result because of the non-linear nature of RO frequency according to process variation. In order to cope with this non-linear nature, we propose an iterative estimation method shown in Fig. 1. Here, we guess the initial values for each process parameter and simulate the corresponding frequencies for the ROs. Initial values for these parameters can be derived from SPICE model. We then get the measured values from chip and build linear models for each circuit. We get estimated variations by solving Eq. (2). In the next iteration, initial values are updated by adding the estimation results from the previous iteration. This procedure is then iterated until the result convergences (difference between measured value and simulated value is zero). From experiments, we found that this method convergences after 4 iterations in most of the cases.

III. ROs for Estimation of Process Variation

In this section, we demonstrate some design techniques to realize variation-sensitive ROs. Sensitivities are checked by SPICE simulation. Commercial 65nm process technology is assumed in our simulation. Based on the simulation results, we propose a set of ROs which is best suited for estimation.

A. RO Design

A general guideline to design ROs with enhanced sensitivities is demonstrated in Fig. 2. We can modify the transistors in an inverter or control the passing current while charging

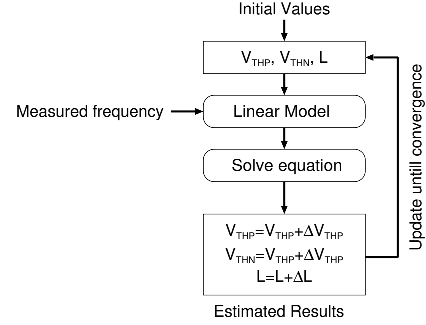


Fig. 1. Proposed estimation procedure of process parameters

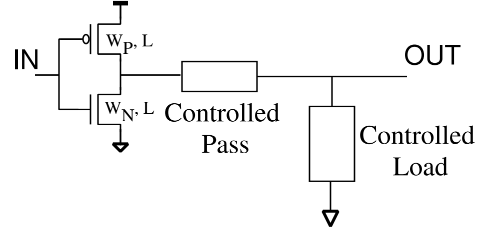


Fig. 2. Tunable parameters in a inverter structure

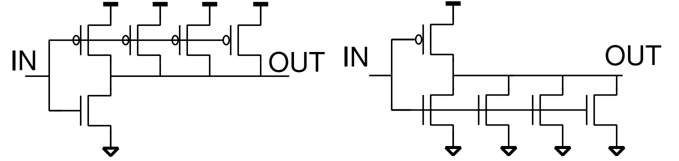


Fig. 3. pMOS rich inverter

Fig. 4. nMOS rich inverter

and discharging the output load to get enhanced process sensitivity. We can control the output load also to change the sensitivities. Changing the gate length will affect the sensitivity to gate length variation. However, in order to avoid unnecessary influence from unknown sources, we have used MOS transistors with identical layout. Therefore, we avoided changing gate length in our design. Modifying gate width changes the charging and discharging current flow and thus the sensitivities change. Below are some examples of inverter structures to realize several variation-sensitive ROs.

1) RO with Parallel MOS: Increasing pMOS transistor's size in the inverter structure will make the RO frequency more sensitive to nMOS parameters. We can increase gate width of pMOS transistor or we can place multiple pMOS transistors in parallel. In order to maintain regularity, we have designed inverters with parallel pMOS transistors. Fig. 3 shows an inverter where pMOS is 4 times larger than that of the standard cell. Similarly, inverter structure shown in 4 will be more sensitive to pMOS parameters. From simulation results for a pMOS rich inverter cell RO, 21% increase in V_{THN} sensitivity and 20% decrease in V_{THP} sensitivity is calculated compare to that of the standard inverter cell RO.

2) RO with Pass Gate: Authors in [9] used ROs with pass gates for estimation of threshold voltage variation since this kind of structure makes RO frequency highly sensitive to

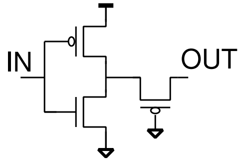


Fig. 5. Inverter with a pMOS pass gate

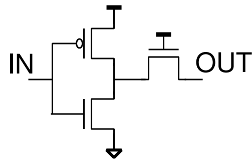


Fig. 6. Inverter with a nMOS pass gate

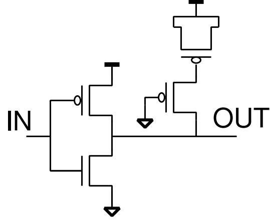


Fig. 7. Inverter with pMOS controlled load

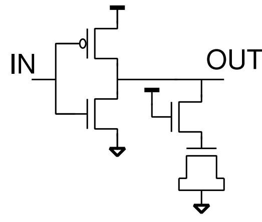


Fig. 8. Inverter with nMOS controlled load

TABLE I
SENSITIVITY COEFFICIENTS OF ROS

RO Type	Gate Length[nm]	k_P	k_N	k_L
Standard	60	-0.038	-0.035	-0.026
pMOS pass gate	60	-0.24	0.052	-0.085
nMOS pass gate	60	0.054	-0.34	-0.029
pMOS rich	60	-0.031	-0.041	-0.026
nMOS rich	60	-0.046	-0.034	-0.027
pMOS load	60	-0.020	-0.048	-0.023
nMOS load	60	-0.044	-0.022	-0.027

threshold voltage change. We therefore have used pass gates to increase sensitivity to threshold voltage. Figs. 5 and 6 show inverters with a pMOS and a nMOS pass gates. For a RO with pMOS pass gate, V_{THP} sensitivity increases by 5 times than that of a standard cell RO. For a RO with a nMOS pass gate V_{THN} sensitivity increases by 7 times than that of a standard cell RO.

3) RO with MOS Controlled Load: Figs. 7 and 8 are ROs with an extra load in the output. Here, the extra load is controlled by MOS pass gate. For Fig. 7, when V_{THP} increases, resistance for the pMOS pass gate increases. As a result, the inverter sees smaller load and hence delay decreases. Thus, the effect of V_{THP} variation gets reduced. Sizing of the load determines the sensitivity for this structure. For RO in Fig. 7 where the extra load is equivalent to 4 inverter cells, sensitivity to V_{THP} decreases by 45% than that of a standard cell RO.

Table I summarizes sensitivity coefficients for these ROs to V_{THP}, V_{THN} and L.

B. RO Set for Process Parameter Estimation

Fig. 9 shows frequency changes for various types of ROs according to V_{THP} variation. The question is how to choose the ROs for process parameter estimation. ROs whose sensitivity vectors form large angles between them are most suitable for this. Fig. 10 shows sensitivity vectors for ROs with pass gates and rich inverters along with a standard inverter. From Fig. 10, we observe that ROs with pass gates are suitable for monitoring threshold voltage variation. But, to get gate length variation also we need another RO along with ROs with pass gates to form Eq. (2). A well-conditioned sensitivity matrix is needed so that estimation result will be robust against uncertainties. Table II shows condition numbers of sensitivity matrices for different RO sets. Condition number is a good indicator on how robust estimation result will be against the uncertainties in sensitivity coefficients or in measurement values. In Table II, RO set with ROs with pass gates and a standard cell RO has the smallest condition number. Considering layout complexity and area, the combination of a standard inverter RO and ROs with pass gates are the best choice for process parameter estimation.

TABLE II
CONDITION NUMBER OF SENSITIVITY MATRICES FOR DIFFERENT RO SETS

No.	RO Set			Condition Number
	RO #1	RO #2	RO #3	
1	Standard	pMOS Pass	nMOS Pass	34.2
2	Standard	pMOS rich	nMOS rich	126.6
3	Standard	pMOS Load	nMOS Load	40.0

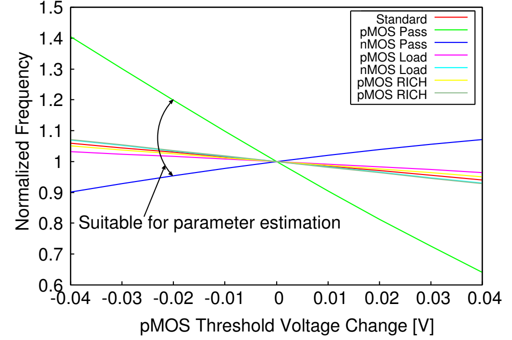


Fig. 9. Frequency changes for ROs to pMOS threshold voltage change

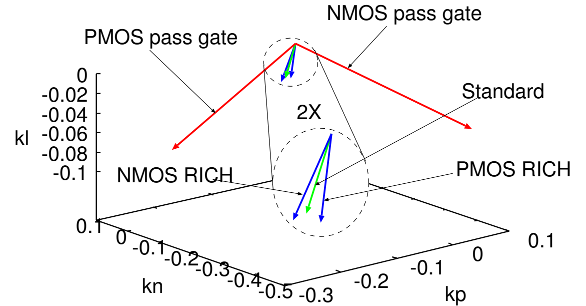
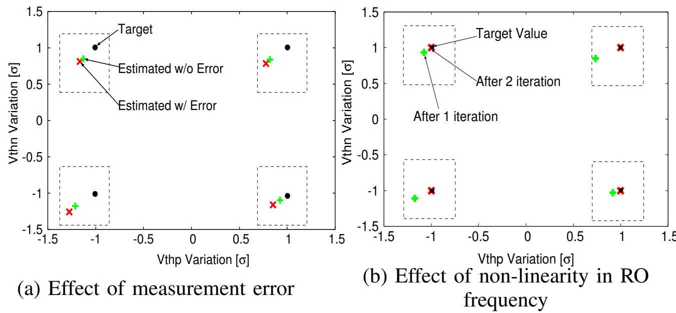


Fig. 10. Sensitivity vectors of various types of ROs

C. Validation by Simulation

We propose a standard inverter RO and ROs with pass gates as monitor circuits for process parameter estimation. We need to check how accurate estimation results will be when some uncertainties are there in measurement or when some effect of parameters other than our interest are involved. In order to show validity, we first show that our monitor circuits can estimate process variation correctly even if some amount of error exists in the measurement. Next, we show that by doing iteration error becomes less.



(a) Effect of measurement error

(b) Effect of non-linearity in RO frequency

Fig. 11. Experimental results of V_{TH} variation estimation

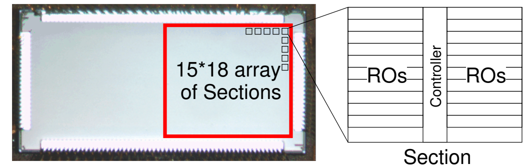


Fig. 12. Test chip in 65nm process

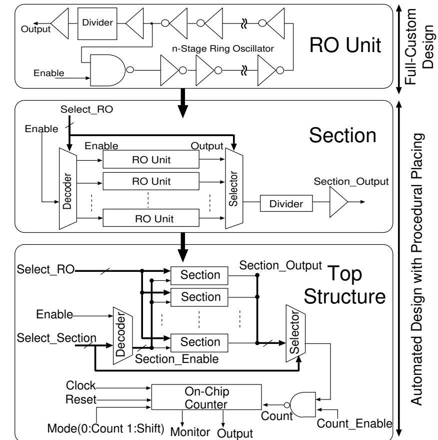


Fig. 13. Block diagram of test structure

1) Simulation Setup: To emulate real chip condition where some amount of variation in process parameters are involved, experiment based on SPICE simulation is conducted. First, some amount of variation in each process parameter is inserted in SPICE model and the corresponding frequencies for our circuits are simulated. Simulated frequencies are then assumed to be the measured values. Next, our proposed monitor circuits are used to estimate the inserted amount of variation for each parameter. Finally, estimated results are compared with the inserted values. Following two scenarios are considered in the experiment.

1) Effect of error in RO frequency measurement
2) Effect of non-linearity in RO frequency to process variation

For simplicity, we demonstrate experimental results for $(\pm\sigma, \pm\sigma)$ variation for V_{THP} and V_{THN} only.

2) Simulation Results: Fig. 11 shows the estimation results for our proposed set of ROs. In Fig. 11 X-axis and Y-axis refer to V_{THP} and V_{THN} variation respectively. "•" points are the inserted variations. In Fig. 11(a) "+" points are estimated variations when no error exists in measurement and "×" points are estimated results when 1% error exists in measurement. In Fig. 11(b) "+" and "×" points are estimated variations after 1 and 2 iterations. In Fig. 11 we see that target variation is achieved with maximum error of 25% when no error exists in the measured value. This error is due to the non-linear nature of RO frequency. The important thing here is in spite of 1% error in the frequency, estimation results do not move from the original values. Fig. 11(b) shows that after 2 iterations the error improves from 25% to 1%. So, our proposed circuits are able to estimate process variations correctly even if some error exists in the measurement.

IV. Estimation Result from Test Chip

We fabricated test chip in 65nm process to check our proposed monitor circuits. In this section, we describe our test structure and estimation results.

A. Chip Design

We designed the ROs of various types described in Section III. We put 270 sections in the chip in an array of 15×18 sections. Each section contains various types of ROs. Therefore, 270 ROs of the same type are integrated in a single die. Fig. 12 shows the layout of our chip. Fig. 13 shows the block diagram of our test structure. On-chip counter is used to capture RO frequency. RO are frequencies are divided by 64 to capture on-chip. Each RO is 13 staged. The purpose of this kind of design is to get both WID and D2D variation. D2D variation is used to estimate D2D process parameter variation and WID variation will be used to determine the number of stages needed for each RO to estimation variation correctly.

TABLE III
Simulation and Measurement Result of RO Frequencies

RO Type	Simulation[at TT] [MHz]	Measurement [MHz]	Variation(σ/μ)[%]	
			WID	D2D
Standard	2583	2976	1.05–1.2	1.47
pMOS Pass	546	613	3.73–4.72	4.34
nMOS Pass	446	674	4.24–5.32	3.26
pMOS Load	1558	1805	1.09–1.32	1.27
nMOS Load	1573	1839	1.05–1.26	1.30
pMOS Rich	1731	1881	0.939–1.14	1.30
nMOS Rich	1590	1879	0.919–1.13	1.26

B. Measurement Result

Table III shows measured data from our test chip. Measurement value shown in Table III is the average of all frequency measurements from 20 chips. SPICE simulation results of our ROs at TT (Typical-Typical) corner model are also presented. Large difference between simulated and measured values are observed. These differences are caused because of variation in process parameters. The amount of difference varies from RO-structure to RO-structure which suggests that process parameter the variation have different impacts on circuits based on their structure. WID and D2D variations are also shown in Table III. Large variation in frequency for ROs with pass gates are observed because these ROs are highly sensitive to threshold voltage variation.

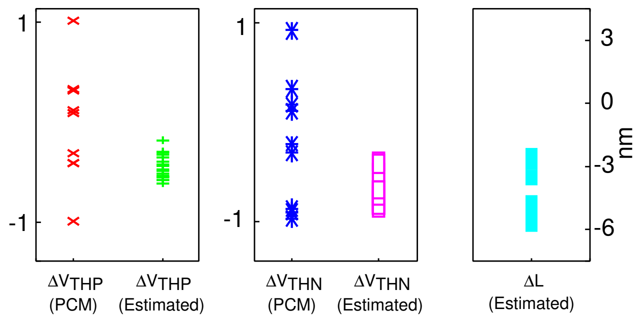


Fig. 14. Comparison between process parameter variation in our estimation result and that in PCM data

C. Estimation Result

Values of $\Delta V_{\rm THP}$, $\Delta V_{\rm THN}$ and ΔL are estimated using our proposed monitor circuits for 20 chips. In this fabrication, 9 PCM (Process Control Module) transistor performance are provided from the foundry. We therefore compared our estimated D2D variation of $V_{\rm THP}$ and $V_{\rm THN}$ with those in PCM data. Fig. 14 shows the estimated D2D variation and those in PCM data. Y-axis is normalized to -1 to 1 by the variation in PCM data. From Fig. 14 we see that the estimated variation is within the variation range of PCM data. PCM data contains both the D2D and WID variation. As we estimated only D2D variation, our estimated variation range is smaller than that in PCM data. Fig. 14 also shows the estimated amount of gate length variation which spans from -6nm to -2.5nm.

Our method takes the difference between measured value and simulated value of RO frequencies at TT SPICE model and extract process parameter variation from these differences. Our estimation method is iterated until this difference becomes zero. So, simulation results using estimation result should match with measurement values. Table IV shows comparison between measurement and simulation values for all RO frequencies for a particular chip. Estimated amount of variation for each parameter is inserted in SPICE model during simulation. As first three ROs in Table IV are used for estimation, simulation and measurement results for the first three ROs match completely. This validates that our proposed estimation technique works correctly. If the estimations are correct and major of the D2D variation can be expressed by the variation in the parameters of our interest, then we should get close values between measurement and simulation for other ROs also. Small amount of difference is there for other ROs in Table IV which suggest that major of the D2D variation can be expressed by $V_{\rm THP}$, $V_{\rm THN}$ and L variation. However, relatively large difference is observed for pMOS rich RO. One possible reason for this difference may be the effect of strain in nMOS transistors. This is because in the pMOS rich inverter cell design, we made a mistake by not placing dummy transistors below the duplicated pMOS transistors, and hence there are wide STI regions between nMOS transistors which may affect nMOS characteristics.

TABLE IV
COMPARISON BETWEEN MEASUREMENT AND SIMULATION USING ESTIMATED RESULTS FROM OUR PROPOSED ROS

RO Type	Measurement[MHz]	Simulation[MHz]	Difference[%]
Standard	2934	2934	0.0
pMOS Pass	586	586	0.0
nMOS Pass	673	673	0.0
pMOS Load	1777	1773	-0.3
nMOS Load	1813	1774	-2.2
pMOS Rich	1849	1922	4.0
nMOS Rich	1856	1840	-0.8

V. CONCLUSION

In this paper, we propose a set of variation-sensitive ROs for estimation of $V_{\rm THP}$, $V_{\rm THN}$ and L variation. We develop a method based on linear model to extract process parameter variation from these ROs. General guideline on how to design variation-sensitive ROs is demonstrated. Experimental results based on SPICE simulation show that our proposed circuits are suitable for process parameter estimation under the presence of uncertainties. We fabricate test chip to verify our circuits and successfully estimated process variation. $V_{\rm THP}$ and $V_{\rm THN}$ variation range in our estimated result is within the variation range in PCM data. SPICE simulation results using our estimated amount of variation match closely with measured values for all ROs. In future, we will define the number of stages needed for on-chip parameter estimation correctly.

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