Variational Circuit Compiler for Quantum Error Correction

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Quantum error correction is vital for implementing universal quantum computing. A key component is the encoding circuit that maps a product state of physical qubits into the encoded multipartite entangled logical state. Known methods are typically not "optimal" either in terms of the circuit depth (and therefore the error burden) or the specifics of the target platform, i.e., the native gates and topology of a system. This work introduces a variational compiler for efficiently finding the encoding circuit of general quantum error-correcting codes with given quantum hardware. Focusing on the noisy intermediate-scale quantum regime, we show how to systematically compile the circuit following an optimizing process seeking to minimize the number of noisy operations that are allowed by the noisy quantum hardware or to obtain the highest fidelity of the encoded state with noisy gates. We demonstrate our method by deriving efficient encoders for logic states of the five-qubit code and the seven-qubit Steane code. We describe ways to augment the discovered circuits with error detection. Our method is applicable quite generally for compiling the encoding circuits of quantum error-correcting codes.

I. INTRODUCTION

Quantum error correction is the key for building large-scale universal quantum computers [1–3] and is essential for mitigating errors in noisy intermediate-scaled quantum (NISQ) computing [4–6]. By encoding the logical state as a multipartite entangled state of several physical qubits, it allows us to detect and even further correct errors of the physical qubit without destroying the logical state. The five-qubit "perfect" code is one of the earliest known codes [7,8]. Being the smallest code that is capable of correcting an arbitrary physical error, the code is also advantageous with low-weight stabilizer operators. An even earlier example is the seven-qubit Steane code [9]. Also known as the smallest two-dimensional (2D) color code, it has low-weight and symmetrical X and Z stabilizers. As a CSS code it further allows transversal Clifford operations, thus the logical gates of the entire Clifford group are inherently fault tolerant.

In experiment, quantum error-detecting and -correcting codes have been implemented in different platforms ranging from superconducting circuits [10–14], trapped ions [15–18], N-V centers in a diamond [19], optics [20–23], and others [24,25]. However, those experiments are limited to handling only a certain type of error or with a particular

logical state. Comprehensive demonstration of full error correction remains a challenge for the field, mainly due to experimental imperfect controls of the physical qubits and theoretical inefficient compiling of the encoding and decoding processes. Achieving proof-of-principle realizations using near-term noisy quantum devices is therefore difficult, as the encoding, parity checks, and decoding processes may include several dozens of imperfect gates as well as nontrivial environmental decoherence, so that the error burden may go beyond the capability that a code can correct and therefore lead to a logical error that cannot be detected and corrected.

Therefore, realizing error correction with NISQ hardware requires both theoretical and experimental advances. Theoretically, the use of classical approaches to reinforce the performance of error-correction codes has been exploited [26,27]. From the experimental perspective, the manipulation of qubits should be improved to the highest accuracy. However, different physical systems have different hardware arrangements, control pulses, native types of multiqubit gates, etc. For example, the natural entangling operation between two qubits with certain superconducting circuits and N-V centers is a form of CNOT or CPHASE gate [28–31], while it is a Mølmer-Sørensen gate for many trapped ion systems [32,33], and sqrt-SWAP gate may be the native operation in quantum-dot systems [34,35]. Meanwhile, conventional methods for the realization of error-correcting codes do not necessarily involve rigorous analytic or numerical optimization and therefore

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may have an unnecessarily large number of gates. It is thus theoretically necessary to more efficiently compile quantum error-correcting protocols against a specific hardware target.

There are a number of approaches to quantum compilation documented in the literature. These range from classical methods based on exploiting perfect circuit isomorphisms (e.g., gate commutation) [36–40], to methods that can "discover" near-equivalent circuits using a quantum device for the compilation (or, for small circuits, an emulator) [41–44]. In this work, we adopt an approach more closely related to the latter, since we compile in such a fashion to support any given noisy quantum hardware where formal circuit equivalence may be difficult or impossible to determine. We construct a variational compiler to automatically search for circuits that encode a target logical state of an error-correcting code. The procedures we describe aim to seek circuits that are optimized in a defined way, such that they meet all the constraints under the particular condition and they are most favorable by design. For example, the "optimized" circuit can be one that has the minimum number of two-qubit gates. Our procedures cannot guarantee that the best solution found is the strictly optimal solution. However we expect that this may indeed be the case when our solution is more efficient than the best circuits previously reported in the literature, or when the automated process "rediscovers" a previously known compact solution.

Our compiler first maps the problem into a ground-state searching problem where the desired logical state is the ground state of the given (synthetic) Hamiltonian. Different from the conventional variational quantum eigensolver cases where the energy spectra are unknown, here the energy spectra are known and can be altered. Next, we consider a set of parameterized ansatz circuits and make use of the variational imaginary-time-evolution method [45,46] to find the ground state, thus discovering the encoding circuit. The ansatz circuit can be tailored to meet specific requirements of any hardware system and any optimization target. For example, when considering quantum hardware with only single- and two-qubit gates, we might either minimize the number of two-qubit gates or minimize the overall infidelity of the prepared state.

The structure of the paper is as follows. In Sec. II, we first review the framework of quantum error correction and introduce the problem of circuit compiling. In Sec. III, we introduce the variational compiling algorithm including the construction of the Hamiltonian, the design of ansatz, and the variational imaginary time evolution. In Sec. IV, we show numerical realizations of the compiling algorithm for different logical states of the five-qubit and seven-qubit codes. We consider both the noise-free and noisy circuits, and for the latter case, we show the fidelity of the prepared state can be boosted through different levels of postselection. We compare our results to existing circuits and

discuss its applicability in NISQ computing. We discuss applications of our results and summarize in Sec. V.

II. BACKGROUND: QUANTUM ERROR CORRECTION

The main idea of quantum error correction is to encode logical qubit(s) with a greater number of noisy physical qubits. Many quantum error-correcting codes can be described by the stabilizer formalism, where the code space is determined by the joint positive eigenspace of a set of commutative stabilizer operators. Specifically, considering the Pauli group G_n on n qubits,

$$G_n \equiv \{\pm I, \pm iI, \pm X, \pm iX, \pm Y, \pm iY, \pm Z, \pm iZ\}^{\otimes n}, \quad (1)$$

the set of stabilizers S for a quantum error-correcting code is a subset of G_n such that $-I \notin S$ and elements in S commute with each other. Suppose S is generated by $G = \langle g_1, \ldots, g_l \rangle$, then the code space corresponds to quantum states $|\Phi\rangle_L$ satisfying $g_i |\Phi\rangle_L = |\Phi\rangle_L$ for all stabilizers g_i. Here we introduce two of the most well-known small quantum error-correcting codes—the five-qubit perfect code and the seven-qubit Steane code, which encode one logical qubit state with five and seven physical qubits, respectively. A stabilizer set for the five-qubit code is

$$\{XZZXI, IXZZX, XIXZZ, ZXIXZ\},$$

and for the Steane code is

$$\{IIIXXXX, XXIIXXI, XIXIXIX, IIIZZZZ, ZZIIZZI, ZIZIZIZ\}.$$

In the logical subspace, the code is further uniquely determined by the logical Z_L operator, with $Z_L |0\rangle_L = |0\rangle_L$ and $Z_L |1\rangle_L = -|1\rangle_L$. A general logical pure state can be thus represented as $|\Phi\rangle_L = a|0\rangle_L + b|1\rangle_L$. For the five- and seven-qubit codes, all the logical Pauli operators can be transversely realized with corresponding identical local Pauli operators. That is, we have $Z_L = ZZZZZ$ and $Z_L = ZZZZZZZ$ for the five- and seven-qubit codes, respectively. For example, the logical $|0\rangle_L$ and $|1\rangle_L$ states of the five-qubit code are defined by

$$
\begin{aligned}
|0\rangle_L = \frac{1}{4}[&|00000\rangle - |00011\rangle + |00101\rangle - |00110\rangle \\
& + |01001\rangle + |01010\rangle - |01100\rangle - |01111\rangle \\
& - |10001\rangle + |10010\rangle + |10100\rangle - |10111\rangle \\
& - |11000\rangle - |11011\rangle - |11101\rangle - |11110\rangle], \\
|1\rangle_L = \frac{1}{4}[&-|00001\rangle - |00010\rangle - |00100\rangle - |00111\rangle \\
& - |01000\rangle + |01011\rangle + |01101\rangle - |01110\rangle \\
& - |10000\rangle - |10011\rangle + |10101\rangle + |10110\rangle \\
& - |11001\rangle + |11010\rangle - |11100\rangle + |11111\rangle].
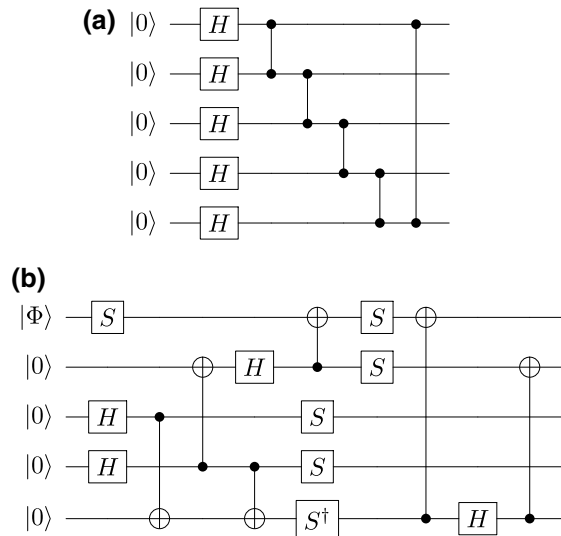\end{aligned}
$$

$$(2)$$

FIG. 1. Encoding circuit for the five-qubit code. (a) Circuit to encode the logical minus state $|-\rangle_L$ [47]. (b) Circuit to encode an arbitrary logical state [11].

FIG. 2. Previously known encoding circuits for the seven-qubit code. (a) Circuit to encode a logical zero state $|0\rangle_L$[48]. (b) Circuit to fault tolerantly encode a logical zero state $|0\rangle_L$ [49]. Note that logical Clifford eigenstates can also be prepared with this circuit by applying transversal logical Clifford gates after the error-detection process. Three CNOT gates are applied to the ancilla qubit, which is then measured in {0, 1} basis. If the measurement result is 1, indicating more than one bit-flip errors occurring, the whole circuit is abandoned and restarted from the beginning, until the ancilla qubit is measured to be 0. (c) Circuit to encode an arbitrary logical state [47].

In this work, we focus on the problem of how to prepare a logical quantum state $|\Phi\rangle_L = a|0\rangle_L + b|1\rangle_L$ by applying an encoding circuit to a given easily prepared initial state.

We aim to find suitable circuits automatically and in a fashion that is more optimal according to some user-specified criteria. As context for our work, we now exhibit a few previously reported examples of encoding circuits for the five-qubit code and the Steane code.

For the five-qubit code, at minimum five two-qubit gates are required to prepare a logical state. The circuit shown in Fig. 1(a) encodes a logical minus state $|-\rangle_L$ with five single-qubit gates and five CPHASE gates [47]. However, to encode an arbitrary logical state, an extra two-qubit gate is required; a suitable circuit is shown in Fig. 1(b) and was recently reported in Ref. [11].

Encoding a logical qubit with the seven-qubit Steane code requires more multiqubit gates. Figure 2(a) shows the circuit to prepare a logical zero state $|0\rangle_L$ with eight CNOT gates [48]. This circuit can also be fault tolerant given three additional two-qubit gates and one ancilla qubit [49], as shown in Fig. 2(b). To encode an arbitrary logical state, one may use the circuit shown in Fig. 2(c), which has 11 CNOT gates [47].

It is in general nontrivial to find an efficient encoding circuit for a given error-correcting code, and the circuit found by hand may not be optimal or compatible with specific experimental hardware. The present work solves this problem by introducing a variational way of compiling the encoding circuit. We show in the following that even the presented encoding circuits for the five- and seven-qubit codes are not necessarily optimal in terms of the number of two-qubit gates.
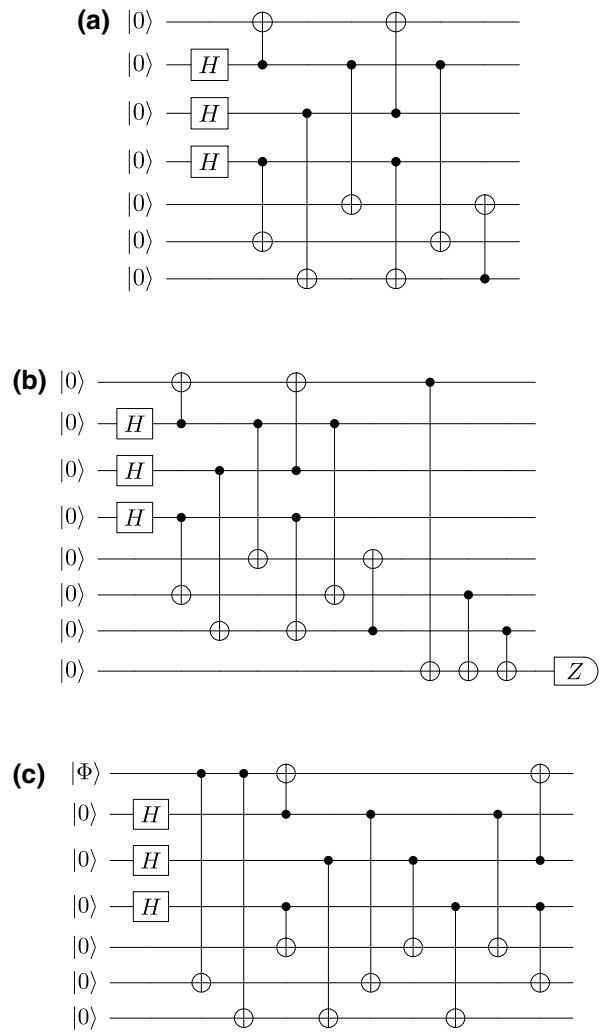
III. VARIATIONAL CIRCUIT COMPILING FOR QUANTUM ERROR CORRECTION

Here we introduce the variational circuit compiler for preparing a logical state of an error-correcting code. The key idea is to construct a Hamiltonian so that the target logical state is its ground state. Then with a parameterized ansatz circuit, we optimize the parameters in order to find the ground state of the Hamiltonian and hence the encoding circuit of the target logical state. We can either realize the

variational circuit compiler with a classical emulator for small error-correcting codes, or with a quantum computer for the general case. In the following, we first introduce the variational circuit compiler and show how to design the Hamiltonian. Then we review the recently proposed variational imaginary time evolution for finding the ground state of the Hamiltonian. We also present the realization of the compiler with quantum circuits. Finally we discuss ansatz design with respect to different quantum hardware.

A. Variational circuit compiler

We first show that any logical state of a stabilizer code can be straightforwardly described as the ground state of a Hamiltonian. Suppose an error-correcting code is stabilized by the generator set $\{g_i\}$. By definition we have

$$g_i \left| \Phi \right\rangle_L = \left| \Phi \right\rangle_L, \quad \forall i, \tag{3}$$

where $\left| \Phi \right\rangle_L$ is an arbitrary logical state. The stabilizers only force the state into the code space. Suppose the logical state is a single-qubit state, it can be further uniquely determined by an additional logical operator

$$O_L = \left| \Phi \right\rangle_L \left\langle \Phi \right|_L - \left| \Phi \right\rangle_L^{\perp} \left\langle \Phi \right|_L^{\perp}. \tag{4}$$

Suppose $\left| \Phi \right\rangle_L = \alpha \left| 0 \right\rangle_L + \beta \left| 1 \right\rangle_L$, it can be further decomposed as a linear sum of logical Pauli operators X_L, Y_L, and Z_L as

$$\begin{aligned} O_L = {} & (\alpha\beta^* + \alpha^*\beta)X_L - i(\alpha^*\beta - \alpha\beta^*)Y_L \\ & - (\beta\beta^* - \alpha\alpha^*)Z_L, \end{aligned} \tag{5}$$

which satisfies $O_L \left| \Phi \right\rangle_L = \left| \Phi \right\rangle_L$. In general, when the error-correcting code encodes more than one qubit, one can always construct a set of logical operators that determines any logical state. Therefore, we can construct a Hamiltonian,

$$H = -\sum_i c_i g_i - c_o O_L, \tag{6}$$

and the target state $\left| \Phi \right\rangle_L$ is its unique ground state

$$H \left| \Phi \right\rangle_L = -\left(\sum_i c_i + c_o \right) \left| \Phi \right\rangle_L, \tag{7}$$

with energy $E_0 = -\left(\sum_i c_i + c_o \right)$. As the terms of the Hamiltonian commute with each other, its eigenstate should be the eigenstate of each term. Thus, it is not hard to see that the first excited state has an energy $E_1 = E_0 + 2\min\{c_i, c_o\}$.

To find the encoding circuit that prepares the target logical state $\left| \Phi \right\rangle_L$, we employ variational methods for determining a Hamiltonian's ground state (an approach of much current interest). We first prepare a trial state via a parameterized quantum circuit, called an ansatz, $\psi(\vec{\theta}) = V(\vec{\theta}) \left| \bar{0} \right\rangle$, where $\left| \bar{0} \right\rangle$ refers to a quantum register of which all the data qubits are initialized at $\left| 0 \right\rangle$, and $V(\vec{\theta})$ is described with m parameters, $V(\vec{\theta}) = V_m(\theta_m) \cdots V_2(\theta_2) V_1(\theta_1)$. Suppose the ground state of the Hamiltonian H can be represented by the circuit ansatz, then the problem is rephrased as finding a set of parameters $\vec{\theta}_{\min}$, which minimizes the energy

$$E_{\min} = \min \left\{ \left\langle \psi(\vec{\theta}) \right| H \left| \psi(\vec{\theta}) \right\rangle \right\}. \tag{8}$$

The minimization can be accomplished by any optimization algorithm, such as simple gradient descent or the imaginary time evolution [45,46] as we presently review. The design of ansatz with respect to different quantum hardware is also discussed shortly.

In practice, we may not be able to find the exact ground state, for example because it lies outside the set of states reachable from the ansatz, or because of the existence of gate noise, etc. Suppose the minimal energy we can find is $E_{\min}$, then we can also lower bound the fidelity between the state ρ we find and the target logical state $\left| \Phi \right\rangle_L$ according to

$$F = \left\langle \Phi \right| \rho \left| \Phi \right\rangle_L \geq 1 - (E_{\min} - E_0)/c, \tag{9}$$

where we denote $c = 2\min\{c_i, c_o\}$ and assume $E_{\min} \in [E_0, E_1]$. The proof of Eq. (9) can be found in the appendix. Therefore, when observing an energy that is close to the ground-state energy, we are assured that the state is indeed close to the exact ground state. In the rest of this paper, we thus focus only on minimizing the energy of the Hamiltonian.

B. Variational simulation with imaginary time evolution

In previous studies we have find that the imaginary-time-evolution method can outperform conventional optimization methods [45,46], therefore we opt to use the variational imaginary time approach as our ground-state finding strategy. Needless to say, other variational methods could equivalently be substituted and this is an area for future study. We briefly review the theory here for self-consistency, including both the pure- and mixed-state cases thus supporting both noiseless and noisy operations in realizing the encoding circuit.

1. Pure state

The imaginary time evolution is defined as

$$\left| \phi(\tau) \right\rangle = \frac{e^{-H\tau} \left| \phi(0) \right\rangle}{\sqrt{\left\langle \psi(0) \right| e^{-2H\tau} \left| \phi(0) \right\rangle}} \tag{10}$$

or equivalently

$$\frac{\partial |\phi(\tau)\rangle}{\partial \tau} = -(H - E_\tau)|\phi(\tau)\rangle, \quad (11)$$

with τ being imaginary time and $E_\tau = \langle\phi(\tau)|H|\phi(\tau)\rangle$. As the amplitudes of all excited eigenstates decay faster than the ground state, we always have $|\phi(\infty)\rangle$ being the ground state of the Hamiltonian H. While the imaginary time evolution cannot be directly realized via a unitary quantum circuit, it can be emulated via the variational algorithm. Assuming the state $|\phi(\tau)\rangle$ can be well approximated by a parameterized state $|\phi(\tau)\rangle = |\psi(\theta_1, \theta_2, \ldots)\rangle$ with real parameters θ_i, the imaginary time evolution of the quantum state $|\psi(\tau)\rangle$ can be mapped to the evolution of the parameters as

$$\sum_j A_{i,j} \dot\theta_i = -B_i, \quad (12)$$

where

$$A_{i,j} = \text{Re}\Big(\frac{\partial \langle\psi[\vec\theta(\tau)]|}{\partial\theta_i} \frac{\partial |\psi[\vec\theta(\tau)]\rangle}{\partial\theta_j}$$
$$+ \frac{\partial \langle\psi[\vec\theta(\tau)]|}{\partial\theta_i}|\psi[\vec\theta(\tau)]\rangle \frac{\partial \langle\psi[\vec\theta(\tau)]|}{\partial\theta_j}|\psi[\vec\theta(\tau)]\rangle\Big),$$

$$B_i = \text{Re}\Big(\frac{\partial \langle\psi[\vec\theta(\tau)]|}{\partial\theta_i} H |\psi[\vec\theta(\tau)]\rangle\Big), \quad (13)$$

Suppose for the initial state we have $|\phi(\tau)\rangle = |\psi\rangle [\theta_1(0), \theta_2(0), \ldots]$, thus we can update the parameters $\vec\theta = (\theta_1, \theta_2, \ldots)$ via $\vec\theta(\tau + \Delta\tau) = \vec\theta(\tau) + \Delta\tau * \dot{\vec\theta}(\tau)$ to emulate imaginary time evolution. Here we choose $\Delta\tau$ to be a sufficiently small step size.

2. Mixed state

When the state is a mixed state, the imaginary time evolution obeys [46]

$$\frac{\partial}{\partial\tau}\rho(\tau) = -\{[H, \rho(\tau)] - 2\langle H\rangle\rho(\tau)\}. \quad (14)$$

When considering a parameterized density matrix $\rho[\vec\theta(\tau)]$, the imaginary time evolution of $\rho[\vec\theta(\tau)]$ is mapped to the evolution of the parameters as

$$\sum_i C_{j,i}\dot\theta_i = -D_j, \quad (15)$$

where

$$C_{j,i} = \text{Tr}\Big(\frac{\partial\rho[\vec\theta(\tau)]}{\partial\theta_j}\frac{\partial\rho[\vec\theta(\tau)]}{\partial\theta_i}\Big),$$
$$D_j = \text{Tr}\Big(\frac{\partial\rho[\vec\theta(\tau)]}{\partial\theta_j}\{H, \rho[\vec\theta(\tau)]\}\Big) \quad (16)$$

C. Implementation on quantum circuits

Our variational circuit compiler can be emulated with a classical computer for small error-correcting codes or it can be implemented with quantum circuits for general codes. Here we briefly discuss the implementation of the pure-state case with quantum circuits and we refer to Ref. [46] for the discussion of the mixed-state case.

As the target logical state is the unique ground state of a Hamiltonian, we thus make use of the variational imaginary-time-evolution method to find the ground state. For the pure-state case, we need to measure every term of A and B defined in Eq. (13). Suppose we consider an ansatz $\psi(\vec\theta) = V(\vec\theta)|0\rangle$, where each $V_i(\theta_i)$ is a single-qubit rotation around the X, Y, or Z axis of the Bloch sphere. We can then decompose the derivative of the state as

$$\frac{\partial |\psi(\vec\theta)\rangle}{\partial\theta_i} = f_i |\varphi_i(\vec\theta)\rangle, \quad (17)$$

where

$$|\varphi_i(\vec\theta)\rangle = U_i(\vec\theta)|0\rangle$$
$$= V_m(\theta_m)\cdots\sigma_i V_i(\theta_i)\cdots V_2(\theta_2)V_1(\theta_1)|0\rangle.$$

Thus each term of A consists of

$$\frac{\partial \langle\psi(\vec\theta)|}{\partial\theta_j}|\psi(\vec\theta)\rangle$$
$$= f_j^* \langle\varphi_j(\vec\theta)|\psi(\vec\theta)\rangle = f_j^* \langle 0|U_j^*(\vec\theta)V(\vec\theta)|0\rangle,$$
$$\frac{\partial \langle\psi(\vec\theta)|}{\partial\theta_j}\frac{\partial |\psi(\vec\theta)\rangle}{\partial\theta_i} = f_i f_j^* \langle 0|U_j^*(\vec\theta)U_i(\vec\theta)|0\rangle. \quad (18)$$

Similarly, each B_j is the real part of

$$\frac{\partial \langle\psi(\vec\theta)|}{\partial\theta_j}H|\psi(\vec\theta)\rangle = \sum_k f_j^* l_k \langle 0|U_j^*(\vec\theta)H_k V(\vec\theta)|0\rangle, \quad (19)$$

where we assume $H = \sum_k \lambda_k H_k$ with H_k representing a tensor product of Pauli matrices. As all those terms are in a general form of

$$a\text{Re}\left(e^{i\theta}\langle\bar 0|U|\bar 0\rangle\right),$$

they can be efficiently measured with the Hadamard test quantum circuit or equivalent but simpler methods [50,51].

D. The ansatz

Our variational circuit compiler assumes the logical state can be prepared by a parameterized ansatz. For different quantum hardware, the ansatz can have different structures. Here, we introduce the general structure of the
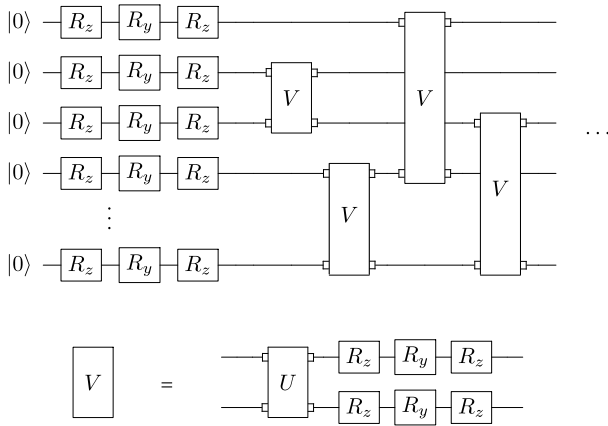
FIG. 3. Building block of the ansatz. The circuit starts with three single-qubit gates applied to each of the data qubits. Then elementary blocks are randomly inserted into the circuit. Each elementary block consists of one two-qubit gate followed with three single-qubit gates on both of the two data qubits. R_y and R_z represent a single-qubit rotation over the Y and Z axes of the Bloch sphere, respectively, where the rotation angle is the parameter to be updated over time.

ansatz considered in this work, as shown in Fig. 3. We consider parameterized single-qubit gates rotating along the Pauli basis. For example, the gate R_x is defined as $R_x = \exp(-i\theta X/2)$ with the rotation angle being a variable parameter θ. The definitions of R_y and R_z are similar. We also consider general two-qubit gates composed by a fixed two-qubit gate followed by six parameterized single-qubit gates. The overall structure of the ansatz is shown in Fig. 3, where three single-qubit rotations with different parameters are firstly applied to each of the data qubits following the order of $R_z R_y R_z$. The gate set is chosen such that an arbitrary single-qubit rotation can be realized. With given constraints in the connectivity of the qubits and the type of two-qubit gates that can be realized in a given quantum hardware, a certain number of multiqubit sets are then inserted into the circuit, where one gate set consists of a multiqubit gate followed with three single-qubit gates applied to each of the data qubits.

For a given ansatz, which is either randomly generated or following a certain procedure, we update the parameters of the single-qubit gates in order to minimize the energy of the Hamiltonian. Based on different ansatzes or different initial values of parameters, we could either reach the ground state verified by the ground-state energy, or we may reach a local minimum. In the latter case, it may indicate that the ansatz cannot represent the target state, so the experiment is abandoned and restarted until the energy reaches close to the ground-state energy. In order to minimize the number of parameters or single-qubit gates, circuit compilation is applied with the following rule: after each several steps, gates with small parameters are removed; this process continues until the energy starts

to increase. The technique cannot guarantee to find a circuit with minimum number of parameters, though many equivalent circuits can be found and selected.

In practice, one may also need to change the structure of the ansatz when the previously selected ansatz is not powerful enough to represent the target state. Different strategies can be applied here by either adding more single and two-qubit gates or fully adopting a different ansatz structure. Trying all possible ansatz structures is in general impossible for a large error correcting code. Therefore, one may either systematically explore a given family of ansatz structures, or alternatively we may apply some kind of circuit morphing algorithm to the ansatz (as recently discussed in Ref. [42,52,53]). In the following, we focus on the five- and seven-qubit codes, and show numerical emulation of the variational compiler for these two codes with different ansatz structures.

IV. NUMERICAL SIMULATIONS

In this section we present numerical simulations for the variational circuit compiler. The simulation is performed on a classical computer with the Quantum Exact Simulation Toolkit (QuEST) package [54], which is a high-performance classical simulator written in C/C++. We focus on the five- and seven-qubit codes and consider two scenarios with noiseless and noisy gates. Several particular states are considered in the simulation, including eigenstates of the Pauli basis $|0\rangle_L$, $|-\rangle_L$ and the magic state $|T\rangle_L = (|0\rangle + e^{\pi i/4} |1\rangle)/\sqrt{2}$. For the Hamiltonian, we set the coefficients of all the terms to be the same and normalize them so that the ground-state energy is -1. In particular, the Hamiltonian corresponding to a logical state $|\Phi\rangle_L$ of the five- or seven-qubit code is

$$H = -\frac{1}{n}\left(\sum_i g_i + O_L\right), \qquad (20)$$

where g_i are the stabilizers for the five- or seven-qubit code, O_L is the logical operator defined in Eq. (4), $n = 5$ for the five-qubit code, and $n = 7$ for the seven-qubit code. We can verify that $H |\Phi\rangle_L = E_0 |\Phi\rangle_L$ with $E_0 = -1$ and $E_1 = -(n-2)/n$ for the first excited state. Following Eq. (9), when we find a state ρ with energy $E_{\min}$, its fidelity to the target state $|\Phi\rangle_L$ is lower bounded by

$$F \geq 1 - \frac{n}{2}(E_{\min} + 1), \qquad (21)$$

when $E_{\min} \in [-1, -(n-2)/n]$.

We also consider different constraints of the circuit topology for different hardware structures, as revealed in the choice of ansatzes. The constraints could be from practical experimental limitations or inferred from preferences in a future experimental design. In this paper, we take three constraints as examples to illustrate our method.

(1) Minimize the number of two-qubit gates, as most quantum hardware has a lower fidelity for two-qubit gates.

(2) Only use a single type of two-qubit gate, reflecting the fact that hardware typically supports one entangling process at the physical level.

(3) Only apply nearest-neighbor interactions, such as in superconducting qubit systems.

Note that while searching for circuits satisfying (2) or (3), (1) is also applied by default, as more simplified circuits are usually preferred. At the start of one experiment, an ansatz is generated based on the constraints, with all parameters initialized from a small value around zero. The parameters are then updated through the variational imaginary time algorithm, until the energy becomes static in a local minimum, in which case the ansatz is abandoned, or goes to the ground-state energy, in which case we consider the current ansatz is successfully configured. The number of parameters is also gradually reduced in the simulation process: if a certain parameter is found to be around zero, a further simulation is attempted with that gate omitted. This procedure continues until the energy starts to increase. With this trick, we manage to substantially reduce the number of parameters and accelerate the searching process.

In the following, we give several examples of applying our compiler for certain logical states prepared with the five- and seven-qubit code.

A. Compiling with ideal gates

We first consider the case where gates are assumed to be perfect. In this case, we can focus on the optimization with pure-state imaginary time evolution.

We begin with the five-qubit code. By considering the circuit with the minimum number of two-qubit gates, we first rediscover circuits for encoding the $|-\rangle_L$ state, which are consistent with the latest conventional circuit as shown in Fig. 1(a). We also note that with five controlled phase gates, the circuit is capable of encoding the $|0\rangle_L$ state with additional transversal single-qubit gates. As our method is capable of discovering different but equivalent circuits, we show one example in Fig. 4(a), which encodes a logical minus state $|-\rangle_L$.

Next, we apply our compiler for the magic state $|T\rangle_L$ and we find the encoding circuit as shown in Fig. 4(b). The encoding circuit for the magic state is also consistent with the circuit for encoding an arbitrary logical state as shown in Fig. 1(b). Therefore, our method has matched but not surpassed the efficiency of a known circuit for encoding the magic state.

In addition to rediscovering existing encoding circuits, our compiler can also find efficient encoding methods when considering a variety of constraints on the circuit structure. First, we consider the case where sqrt-SWAP gates

are considered as the only type of two-qubit gate in the ansatz. The sqrt-SWAP gate is a non-Clifford gate, so it is not often seen in conventional error-correction encoding circuits. On the other hand, it may be a natural two-qubit gate [55]. The canonical approach would be to convert this gate into a CNOT/CPHASE gate in a circuit design. As one CNOT gate is decomposed into two sqrt-SWAP gates and several single-qubit rotations, at minimum ten sqrt-SWAP gates are then required to encode a $|-\rangle_L$ state. We show here that by applying the sqrt-SWAP gate into the ansatz directly, the number of the sqrt-SWAP gates can be reduced to eight as shown in Fig. 4(c). Next, we consider the case where the ansatz is restricted to allow only nearest-neighbor interactions, which is common for solid-state qubits. We present in Fig. 4(d) a circuit satisfying the constraint, which prepares the magic state $|T\rangle_L$ with seven nearest-neighbor CPHASE gates. (Note that here we specify that CPHASE gates should be the only two-qubit gates; if we relax this and subsume certain single-qubit and CPHASE gates into CNOT gates, then this circuit simplifies further.)

For the seven-qubit Steane code, we also first rediscover the encoding circuits for the $|0\rangle_L$ state as shown in Fig. 2(a), which has eight CNOT gates. For the magic state, we find a circuit that only uses nine CNOT gates, in contrast to the encoding circuit for an arbitrary state, which requires 11 CNOT gates as shown in Fig. 2(c).

B. Noise-robust circuits

In this section, we consider the practical scenario with noisy gates. For each gate, we apply a small probability of depolarizing noise as follows:

$$\rho' \to (1-r)\rho + \frac{r}{3}(X\rho X + Y\rho Y + Z\rho Z). \quad (22)$$

We emphasize that *any* theoretically given noise model in a simulator or any practical noise model in physical hardware could be employed here; we consider depolarizing noise for this first study in order to more readily compare to known methods and results. Then we aim to find the most "noise-robust" encoding circuit for preparing a target logical state. Here, we also consider an ancillary qubit, which is applied to the circuit and postselected in a similar way to fault-tolerant state preparation. Note that when the ancilla is not entangled with the physical qubits, it reduces to the previous case where there is no ancilla. As the encoded state is a mixed state, we make use of the mixed-state mode of the QuEST and the imaginary time evolution for mixed states. We search over a large number (order 10 000) of different ansatzes, and we obtain the circuit corresponding to the lowest energy. We then verify that this circuit performs better in the presence of small gate noise than the circuits found in the earlier section, which are found under the zero-noise assumption.
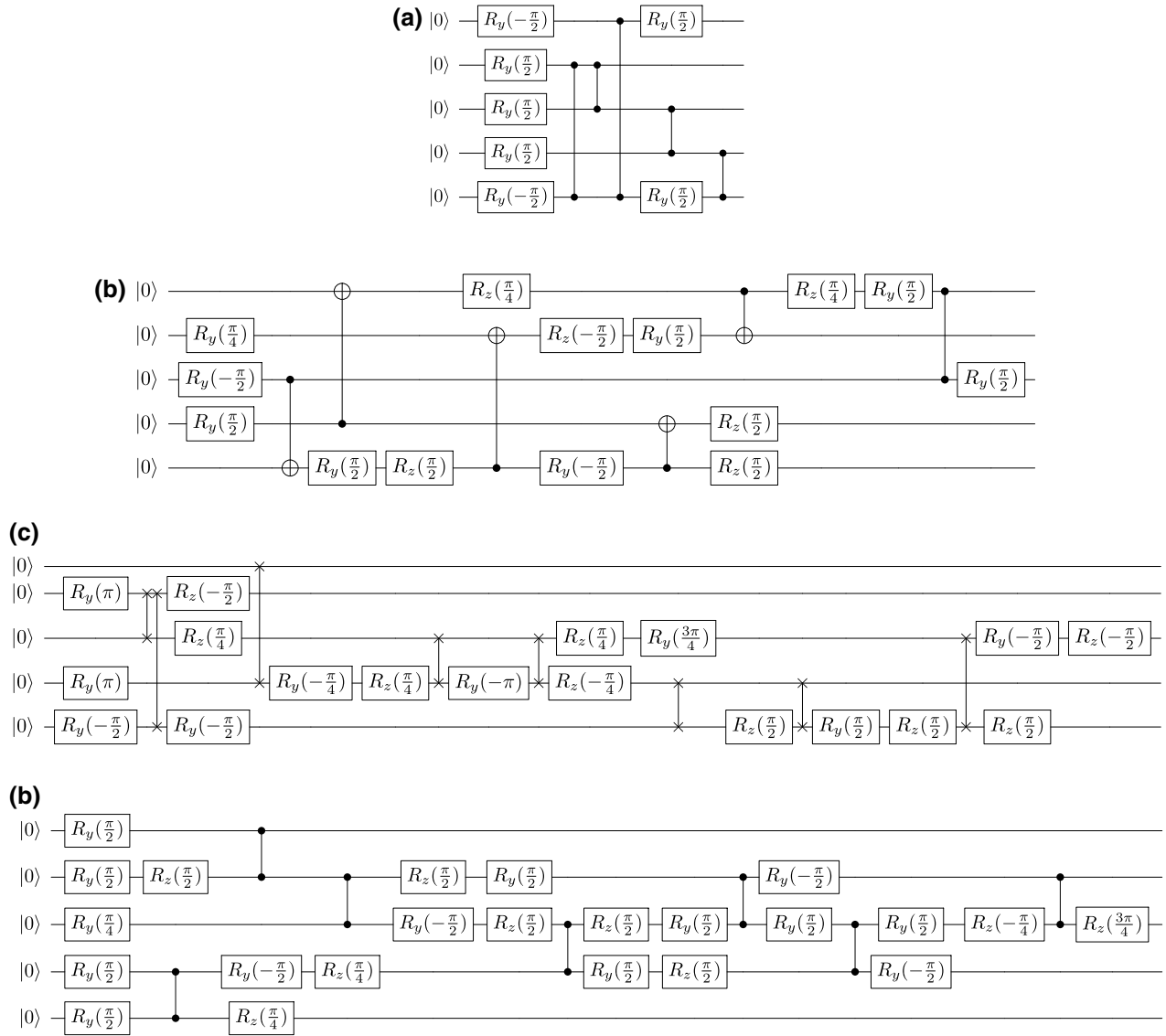
FIG. 4.   (a) Circuit to encode a logical minus state $|-\rangle_L$, with the five-qubit code. This circuit is equivalent to Fig. 1(a). (b) Circuit to encode a logical magic state $|T\rangle_L = \frac{\sqrt{2}}{2}(|0\rangle_L + e^{\frac{\pi}{4}i}|1\rangle_L)$, with the five-qubit code. Our method found at minimum six two-qubit gates are required to prepare the state. (c) Circuit to encode a logical minus state $|-\rangle_L$ with the five-qubit code. The two-qubit gate is restricted to be a sqrt-SWAP gate. (d) Circuit to encode a logical magic state $|T\rangle_L = \frac{\sqrt{2}}{2}(|0\rangle_L + e^{\frac{\pi}{4}i}|1\rangle_L)$. Only nearest-neighbor CPHASE gates are permitted in this case.

For the five-qubit code, a noise-robust circuit is found for encoding the logical minus state $|-\rangle_L$ as shown in Fig. 6. The circuit contains two parts, with the first part (gates on the data qubits) preparing a logical minus state, while the second part (gates between the data qubits and the ancilla) detecting and postselecting errors. Note that the second part is a logical X_L operator, which does not change the logical state.

C. Error detection for general encoding circuits

It is interesting to reflect further on the principle of the circuit, which our automated method has found.

We could generalize the rule to any error-correction codes with transversal Pauli gates. For example, a noise-robust circuit to encode any of the logical states $|0\rangle_L, |1\rangle_L, |+\rangle_L, |-\rangle_L, |+i\rangle_L, |-i\rangle_L$ could be realized by preparing the states with the non-fault-tolerant (non-FT) circuits first and applying a transversal logical operator (which does not change the logical state) for detecting and postselecting errors. We notice that by combining the transversal logical operator with the stabilizer operator, some Pauli terms can be cancelled out. If replaced with this operator for error detection, the circuit is noise robust. Note that the circuit shown in Fig. 6 is not fully fault tolerant,
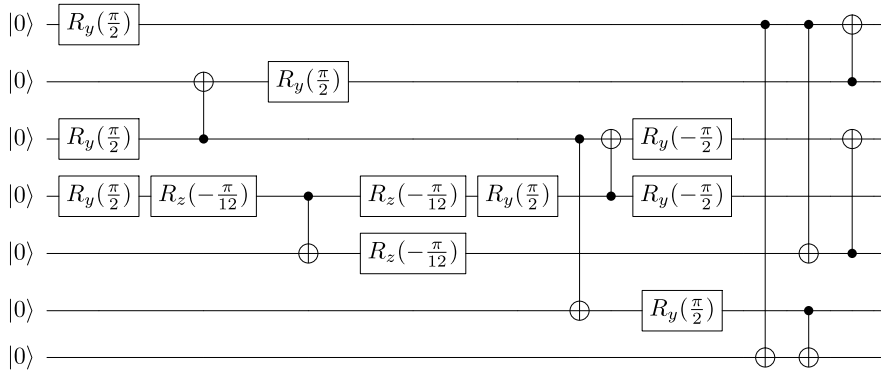
FIG. 5. Circuit to encode a logical magic state $|T\rangle_L = \frac{\sqrt{2}}{2}(|0\rangle_L + e^{\frac{\pi}{4}i}|1\rangle_L)$ with the seven-qubit code. Minimally nine two-qubit gates are required to prepare the state.

as the logical state prepared with the five-qubit code can be corrupted by any single error, while measuring out one logical operator and applying postselection cannot guarantee FT detection of any single error. However, circuits to prepare some logical states with the Steane code applied with error detection can be realized fault tolerantly, as the error detection needs only to detect a certain type of noise, while the logical states are immune to the other type of noise. For example, a logical $|0\rangle_L$ encoded with the Steane code is immune to any phase noise. The circuit discovered by Goto [49] to prepare a FT logical zero state $|0\rangle_L$ with the Steane code [as shown in Fig. 2(b)] is an example.

For the Steane code, one can implement transversal Clifford gates, so one may feel that the same trick can be applied. That is, to test the fault tolerance of the circuit, we measure the logical operator P, when it belongs to the Clifford group and satisfies $P|\Phi\rangle_L = |\Phi\rangle_L$, with $|\Phi\rangle_L$ being the target logical state. Unfortunately, if an error occurs to a data qubit, an extra gate needs to be applied to the data qubit even if the ancilla is measured to be $+$. Therefore, a subsequent error-detection or error-correction procedure is

still required to remove the single error, as pointed out in Ref. [49,56].

In general, there are no universal transversal logical operators for small error-correcting codes. Thus we cannot apply the same trick to fault tolerantly prepare an arbitrary logical state, such as the magic state of the five- and seven-qubit code. However, a FT circuit can be realized by measuring all the stabilizer operators and applying postselections: the ancilla should always be measured to be 1, otherwise the circuit is abandoned and restarted from the beginning. Note that measuring all the stabilizer operators cannot guarantee fault tolerance of the circuit—a logical error created before the error detection cannot be found. As it takes a relatively long time to prepare a logical state, this approach may not be ideal for systems with short coherence time. On the other hand, one can measure one of the stabilizer operators and still benefit partially.

We also note that measuring the stabilizer operators can also be fault tolerant with an extra flag qubit, as shown in Fig. 7. After a logical state is prepared nonfault tolerantly with the five-qubit code, we measure one of the stabilizer operators. The flag qubit is to detect errors occurring between one of the two-qubit gates as shown in the figure.

Finally, we compare the fidelity of the prepared logical state with different encoding circuits as discussed above. In Fig. 8, we show the fidelity change with respect to an
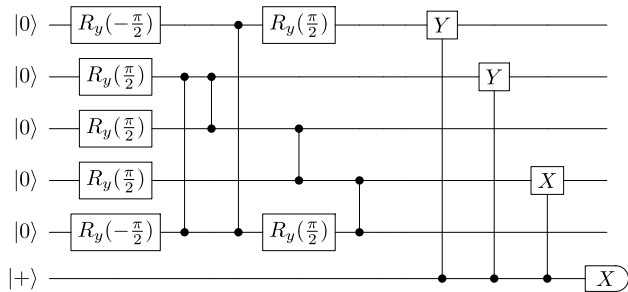

FIG. 6. A noise-robust circuit to encode a logical minus state $|-\rangle_L$ with the five-qubit code. In addition to the first part of the circuit [Fig. 4(a)], which prepares $|-\rangle_L$, three two-qubit gates are applied from the ancilla qubit, which is then measured in the $\{+, -\}$ basis. If measured to be $-$, the output is abandoned and reprepared until the measurement result is $+$.
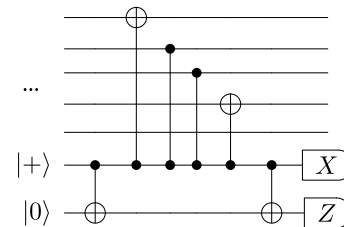

FIG. 7. Circuit to fault tolerantly measure one stabilizer operator with the five-qubit code. The first and second ancillae need to be measured to be $+$ and 0, or otherwise the output is abandoned.
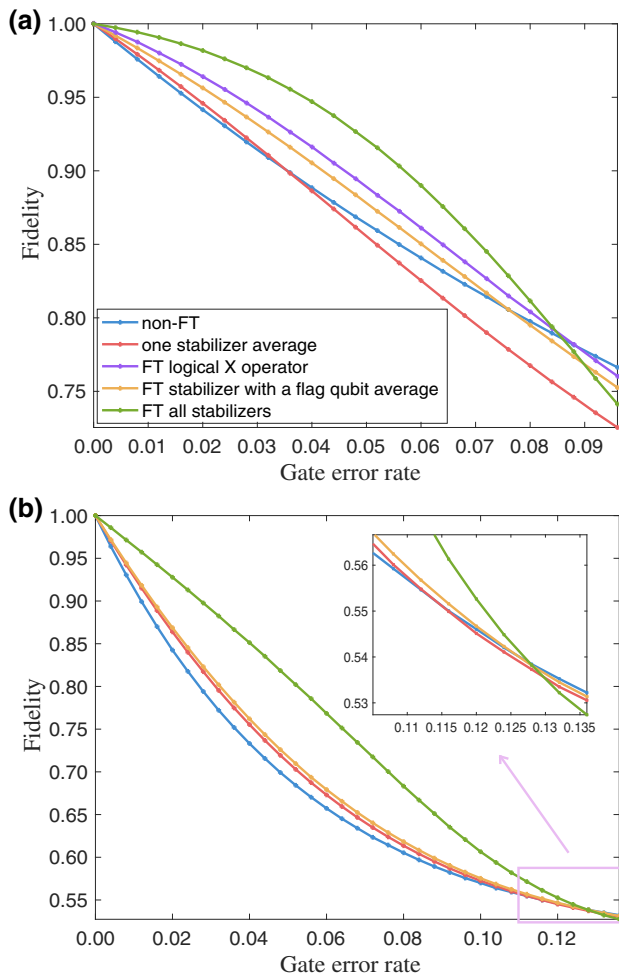
FIG. 8. The fidelity change with the increasing gate error rate in preparation of (a) a logical minus state $|-\rangle_L$ with the five-qubit code and (b) a logical magic state $|T\rangle_L = \frac{\sqrt{2}}{2}(|0\rangle_L + e^{\frac{\pi}{4}i}|1\rangle_L)$ with the seven-qubit code. The error rate for single-qubit gates, two-qubit gates, and measurements is the same. The blue curves represent the case where the logical state is prepared with the non-FT circuits in Fig. 4(a) and Fig. 5 for the two codes, respectively. If one of the four or six stabilizer operators is measured with one ancilla and postselection is applied, the average behavior of the four or six cases is shown as the red curves, while the orange ones refer to the same scenario but the operators are measured fault tolerantly with two ancillae. The purple curve in (a) refers to the case where a logical X operator is measured, with the circuit shown in Fig. 6, except that the error detection is conducted fault tolerantly with additional ancilla. The greens refer to the case where all the stabilizer operators are measured with two ancillae.

increasing gate error rate. The error rate is the same for single-qubit gates, two-qubit gates, and measurement and noise is applied for both the state-preparation and error-detection processes. A logical minus state is prepared with the five-qubit code with the circuit shown in Fig. 4(a). We see that with small noise, applying error detection always

leads to a higher fidelity. However, as the gate error rate gradually increases, the extra noise introduced with the extra gates negates the advantage of error detection. In Fig. 8(a), there is a small gap between the blue and the red curves, indicating that measuring one stabilizer operator nonfault tolerantly gains only a small benefit over the case where no error detection is performed. However, such an advantage increases if the measurement is conducted fault tolerantly with one more ancilla. The purple curve, representing postselection by measuring the X operator, has an overall higher fidelity than the red and orange ones probably due to one fewer two-qubit gate applied. If all the stabilizer operators are measured fault tolerantly with postselection applied, as demonstrated by the green curve, the fidelity is higher than the non-FT circuit when the gate error rate is smaller than 8.6%. Note we verify that in this case, the circuit involving measuring all the stabilizers fault tolerantly is fault tolerant. In Fig. 8(b), a logical magic state $|T\rangle_L = (1/\sqrt{2})(|0\rangle_L + e^{(\pi/4)i}|1\rangle_L)$ is prepared with the seven-qubit code. Compared with (a), we see a group of curves with different shapes but a similar trend, that the curves applied with postselection have a higher fidelity given a small gate error rate. The advantage starts to vanish when the gate error rate is larger than 11%. In this case, we find the circuit involving measuring the full stabilizer set is not fault tolerant but still leads to a notably higher state fidelity. The result suggests the noise robustness of our method.

V. DISCUSSION

In this work, we introduce a variational circuit compiler for efficiently encoding the logical state of an error-correcting code. We construct a Hamiltonian so that the target logical state is its ground state and it can be found with the variational imaginary-time-evolution method. We consider the five- and seven-qubit codes as examples. When having noiseless operations, we show the encoding circuit to prepare different logical states with the minimal number of gates for different hardware structures. When considering noisy gates, it is discovered by applying postselection, the fidelity of the encoded state can be boosted. Therefore, we can simplify the compiling process by searching for more optimal non-FT circuit first with given constraints and noise models, and applying postselection after the state-preparation process.

We also compare the fidelity of logical states prepared with different encoding circuits with respect to different gate error rates. Our work thus opens an avenue for automatically compiling circuits for implementing error-correcting codes. Future studies may focus on the design and searching of ansatzes for different codes and the realization of the compiler with a real quantum computer.

It is natural that some of the highest-performing circuits found by our approach were previously known, since

we opt to explore two very well-studied codes and moreover we employ a noise model (depolarizing noise), which has been the canonical model of choice for previous work. However we emphasize that our approach is by no means limited to these choices and can be used to optimize circuits for newly emerging codes—it is even practical to seek optimization of larger codes, as we can start from the previously discovered circuit and search for better ones, based on bespoke error models that are matched to specific hardware implementations.

ACKNOWLEDGMENTS

APPENDIX: PROOF OF EQ. (9)

Here we prove Eq. (9). Suppose we have a Hamiltonian H with ground and first excited energy denoted by E_0 and E_1, respectively. Given a quantum state ρ with averaged energy $E = \text{Tr}[\rho H]$ satisfying $E \in [E_0, E_1]$, we want to prove

$$F = \langle \psi_0 | \rho | \psi_0 \rangle \geq 1 - (E - E_0)/c, \qquad (A1)$$

where we denote $c = E_1 - E_0$ and $|\psi_0\rangle$ being the ground state of H.

Proof. Denote the eigenstates of H by $|\psi_i\rangle$ with corresponding eigenvalues E_i satisfying $E_i \leq E_j$ when $i \leq j$. Then we have

$$H = \sum_i E_i |\psi_i\rangle \langle \psi_i|,$$

and

$$
\begin{aligned}
E &= \text{Tr}[\rho H], \\
&= \sum_i E_i \langle \psi_i | \rho | \psi_i \rangle, \\
&= E_0 F + \sum_{i \geq 1} E_i \langle \psi_i | \rho | \psi_i \rangle, \\
&\geq E_0 F + \sum_{i \geq 1} E_1 \langle \psi_i | \rho | \psi_i \rangle, \\
&= E_0 F + E_1 (1 - F), \\
&= (E_0 + c) - cF. \qquad (A2)
\end{aligned}
$$

In the third line, we make use of the definition of F in Eq. (A1); In the fourth line, we make use of the ordering of the eigenvalues; In the fifth line, we make use of $\sum_{i \geq 1} \langle \psi_i | \rho | \psi_i \rangle = 1 - \langle \psi_0 | \rho | \psi_0 \rangle = 1 - F$. Solving the equation, we thus get the lower bound of the fidelity F based on the energy E as in Eq. (A1). ∎

[1] A. R. Calderbank and Peter W. Shor, Good quantum error-correcting codes exist, Phys. Rev. A **54**, 1098 (1996).

[2] Daniel Gottesman, Theory of fault-tolerant quantum computation, Phys. Rev. A **57**, 127 (1998).

[3] Peter W. Shor, Scheme for reducing decoherence in quantum computer memory, Phys. Rev. A **52**, R2493 (1995).

[4] X. Bonet-Monroig, R. Sagastizabal, M. Singh, and T. E. O'Brien, Low-cost error mitigation by symmetry verification, Phys. Rev. A **98**, 062339 (2018).

[5] Sam McArdle, Xiao Yuan, and Simon Benjamin, Error-Mitigated Digital Quantum Simulation, Phys. Rev. Lett. **122**, 180501 (2019).

[6] Jarrod R. McClean, Zhang Jiang, Nicholas C. Rubin, Ryan Babbush, and Hartmut Neven, Decoding quantum errors with subspace expansions, Nat. Commun. **11**, 1 (2020).

[7] Charles H. Bennett, David P. DiVincenzo, John A. Smolin, and William K. Wootters, Mixed-state entanglement and quantum error correction, Phys. Rev. A **54**, 3824 (1996).

[8] Raymond Laflamme, Cesar Miquel, Juan Pablo Paz, and Wojciech Hubert Zurek, Perfect Quantum Error Correcting Code, Phys. Rev. Lett. **77**, 198 (1996).

[9] Andrew M. Steane, Error Correcting Codes in Quantum Theory, Phys. Rev. Lett. **77**, 793 (1996).

[10] A. D. Córcoles, E. Magesan, S. J. Srinivasan, A. W. Cross, M. Steffen, J. M. Gambetta, and J. M. Chow, Demonstration of a quantum error detection code using a square lattice of four superconducting qubits, Nat. Comms. **6**, 7979 (2015).

[11] Ming Gong, Xiao Yuan, Shiyu Wang, Yulin Wu, Youwei Zhao, Chen Zha, Shaowei Li, Zhen Zhang, Qi Zhao, and Yunchao Liu *et al.*, Experimental verification of five-qubit quantum error correction with superconducting qubits, arXiv preprint arXiv:1907.04507 (2019).

[12] J. Kelly, R. Barends, A. G. Fowler, A. Megrant, E. Jeffrey, T. C. White, D. Sank, J. Y. Mutus, B. Campbell, Yu Chen, Z. Chen, B. Chiaro, A. Dunsworth, I.-C. Hoi, C. Neill, P.

J. J. O'Malley, C. Quintana, P. Roushan, A. Vainsencher, J. Wenner, A. N. Cleland, and J. M. Martinis, State preservation by repetitive error detection in a superconducting quantum circuit, Nature **519**, 66 (2015).

[13] M. D. Reed, L. DiCarlo, S. E. Nigg, L. Sun, L. Frunzio, S. M. Girvin, and R. J. Schoelkopf, Realization of three-qubit quantum error correction with superconducting circuits, Nature **482**, 382 (2012).

[14] D. Risté, S. Poletto, M.-Z. Huang, A. Bruno, V. Vesterinen, O.-P. Saira, and L. DiCarlo, Detecting bit-flip errors in a logical qubit using stabilizer measurements, Nat. Comms. **6**, 6983 (2015).

[15] John Chiaverini, Dietrich Leibfried, Tobias Schaetz, Murray D. Barrett, R. B. Blakestad, J. Britton, Wayne M. Itano, John D. Jost, Emanuel Knill, and Christopher Langer *et al.*, Realization of quantum error correction, Nature **432**, 602 (2004).

[16] Norbert M. Linke, Mauricio Gutierrez, Kevin A. Landsman, Caroline Figgatt, Shantanu Debnath, Kenneth R. Brown, and Christopher Monroe, Fault-tolerant quantum error detection, Sci. Adv. **3**, e1701074 (2017).

[17] D. Nigg, M. Müller, E. A. Martinez, P. Schindler, M. Hennrich, T. Monz, M. A. Martin-Delgado, and R. Blatt, Quantum computations on a topologically encoded qubit, Science **345**, 302 (2014).

[18] P. Schindler, J. T. Barreiro, T. Monz, V. Nebendahl, D. Nigg, M. Chwalla, M. Hennrich, and R. Blatt, Experimental repetitive quantum error correction, Science **332**, 1059 (2011).

[19] Tim Hugo Taminiau, Julia Cramer, Toeno van der Sar, Viatcheslav V. Dobrovitski, and Ronald Hanson, Universal control and error correction in multi-qubit spin registers in diamond, Nat. Nanotechnol. **9**, 171 (2014).

[20] B. A. Bell, D. A. Herrera-Martí, M. S. Tame, D. Markham, W. J. Wadsworth, and J. G. Rarity, Experimental demonstration of a graph state quantum error-correction code, Nat. Commun. **5**, 3658 (2014).

[21] Chao-Yang Lu, Wei-Bo Gao, Jin Zhang, Xiao-Qi Zhou, Tao Yang, and Jian-Wei Pan, Experimental quantum coding against qubit loss error, Proc. Natl. Acad. Sci. **105**, 11050 (2008).

[22] T. B. Pittman, B. C. Jacobs, and J. D. Franson, Demonstration of quantum error correction using linear optics, Phys. Rev. A **71**, 052332 (2005).

[23] Xing-Can Yao, Tian-Xiong Wang, Hao-Ze Chen, Wei-Bo Gao, Austin G. Fowler, Robert Raussendorf, Zeng-Bing Chen, Nai-Le Liu, Chao-Yang Lu, and You-Jin Deng *et al.*, Experimental demonstration of topological error correction, Nature **482**, 489 (2012).

[24] Julia Cramer, Norbert Kalb, M. Adriaan Rol, Bas Hensen, Machiel S. Blok, Matthew Markham, Daniel J. Twitchen, Ronald Hanson, and Tim H. Taminiau, Repeated quantum error correction on a continuously encoded qubit by real-time feedback, Nat. Commun. **7**, 11526 (2016).

[25] G. Waldherr, Y. Wang, S. Zaiser, M. Jamali, T. Schulte-Herbrüggen, H. Abe, T. Ohshima, J. Isoya, J. F. Du, and P. Neumann *et al.*, Quantum error correction in a solid-state hybrid spin register, Nature **506**, 204 (2014).

[26] Peter D. Johnson, Jonathan Romero, Jonathan Olson, Yudong Cao, and Alán Aspuru-Guzik, Qvector: an algorithm for device-tailored quantum error correction, arXiv preprint arXiv:1711.02249 (2017).

[27] Hendrik Poulsen Nautrup, Nicolas Delfosse, Vedran Dunjko, Hans J. Briegel, and Nicolai Friis, Optimizing quantum error correction codes with reinforcement learning, Quantum **3**, 215 (2019).

[28] Rami Barends, Julian Kelly, Anthony Megrant, Andrzej Veitia, Daniel Sank, Evan Jeffrey, Ted C. White, Josh Mutus, Austin G. Fowler, and Brooks Campbell *et al.*, Superconducting quantum circuits at the surface code threshold for fault tolerance, Nature **508**, 500 (2014).

[29] Leonardo DiCarlo, Matthew D. Reed, Luyan Sun, Blake R. Johnson, Jerry M. Chow, Jay M. Gambetta, Luigi Frunzio, Steven M. Girvin, Michel H. Devoret, and Robert J. Schoelkopf, Preparation and measurement of three-qubit entanglement in a superconducting circuit, Nature **467**, 574 (2010).

[30] Wolfgang Pfaff, Bas J. Hensen, Hannes Bernien, Suzanne B. van Dam, Machiel S. Blok, Tim H. Taminiau, Marijn J. Tiggelman, Raymond N. Schouten, Matthew Markham, and Daniel J. Twitchen *et al.*, Unconditional quantum teleportation between distant solid-state quantum bits, Science **345**, 532 (2014).

[31] Chuan Wang, Yong Zhang, Rong-zhen Jiao, and Guang-sheng Jin, Universal quantum controlled phase gate on photonic qubits based on nitrogen vacancy centers and microcavity resonators, Opt. Express **21**, 19252 (2013).

[32] T. Monz, K. Kim, A. S. Villar, P Schindler, M. Chwalla, M. Riebe, Christian F. Roos, Hartmut Häffner, and W. Hänsel, and Markus Hennrich *et al.*, Realization of Universal Ion-Trap Quantum Computation with Decoherence-Free Qubits, Phys. Rev. Lett. **103**, 200503 (2009).

[33] Ting Rei Tan, John P. Gaebler, Yiheng Lin, Yong Wan, R. Bowler, D. Leibfried, and David J. Wineland, Multi-element logic gates for trapped-ion qubits, Nature **528**, 380 (2015).

[34] Brandon Buonacorsi, Zhenyu Cai, Eduardo Barrera Ramirez, Kyle S. Willick, Sean M. Walker, Jiahao Li, Benjamin D. Shaw, Xiaosi Xu, Simon C. Benjamin, and Jonathan Baugh, Network architecture for a topological quantum computer in silicon, Quantum Sci. Technol. **4**, 025003 (2019).

[35] Zhenyu Cai, Michael A. Fogarty, Simon Schaal, Sofia Patomäki, Simon C. Benjamin, and John J. L. Morton, A silicon surface code architecture resilient against leakage errors, Quantum **3**, 212 (2019).

[36] Matthew Amy, Dmitri Maslov, and Michele Mosca, Polynomial-time t-depth optimization of clifford+ t circuits via matroid partitioning, IEEE Trans. Comput. Aided Design Integrated Circuits Syst. **33**, 1476 (2014).

[37] Luke E. Heyfron and Earl T. Campbell, An efficient quantum compiler that reduces *t* count, Quantum Sci. Technol. **4**, 015004 (2018).

[38] Dmitri Maslov, Gerhard W. Dueck, D. Michael Miller, and Camille Negrevergne, Quantum circuit simplification and level compaction, IEEE Trans. Comput. Aided Design Integrated Circuits Syst. **27**, 436 (2008).

[39] Yunseong Nam, Neil J. Ross, Yuan Su, Andrew M. Childs, and Dmitri Maslov, Automated optimization of large quantum circuits with continuous parameters, Npj Quantum Inf. **4**, 23 (2018).

[40] Aditya K. Prasad, Vivek V. Shende, Igor L. Markov, John P. Hayes, and Ketan N. Patel, Data structures and algorithms for simplifying reversible circuits, ACM J. Emerging Technol. Comput. Syst. (JETC) **2**, 277 (2006).

[41] Kentaro Heya, Yasunari Suzuki, Yasunobu Nakamura, and Keisuke Fujii, Variational quantum gate optimization, arXiv preprint arXiv:1810.12745 (2018).

[42] Tyson Jones and Simon C. Benjamin, Quantum compilation and circuit optimisation via energy dissipation, arXiv preprint arXiv:1811.03147 (2018).

[43] Sumeet Khatri, Ryan LaRose, Alexander Poremba, Lukasz Cincio, Andrew T. Sornborger, and Patrick J. Coles, Quantum-assisted quantum compiling, Quantum **3**, 140 (2019).

[44] Kunal Sharma, Sumeet Khatri, Marco Cerezo, and Patrick J. Coles, Noise resilience of variational quantum compiling, New J. Phys. **22**, 043006 (2020).

[45] Sam McArdle, Tyson Jones, Suguru Endo, Ying Li, Simon C. Benjamin, and Xiao Yuan, Variational ansatz-based quantum simulation of imaginary time evolution, Npj Quantum Inf. **5**, 1 (2019).

[46] Xiao Yuan, Suguru Endo, Qi Zhao, Ying Li, and Simon C. Benjamin, Theory of variational quantum simulation, Quantum **3**, 191 (2019).

[47] Xiaosi Xu, Niel de Beaudrap, Joe O'Gorman, and Simon C. Benjamin, An integrity measure to benchmark quantum error correcting memories, New J. Phys. **20**, 023009 (2018).

[48] Adam Paetznick and Ben W. Reichardt, Fault-tolerant ancilla preparation and noise threshold lower bounds for the 23-qubit golay code, arXiv preprint arXiv:1106.2190 (2011).

[49] Hayato Goto, Minimizing resource overheads for fault-tolerant preparation of encoded states of the steane code, Sci. Rep. **6**, 19578 (2016).

[50] Ying Li and Simon C. Benjamin, Efficient Variational Quantum Simulator Incorporating Active Error Minimization, Phys. Rev. X **7**, 021050 (2017).

[51] Kosuke Mitarai and Keisuke Fujii, Methodology for replacing indirect measurements with direct measurements, Phys. Rev. Res. **1**, 013006 (2019).

[52] Harper R. Grimsley, Sophia E. Economou, Edwin Barnes, and Nicholas J. Mayhall, An adaptive variational algorithm for exact molecular simulations on a quantum computer, Nat. Commun. **10**, 1 (2019).

[53] Xiaosi Xu, Jinzhao Sun, Suguru Endo, Ying Li, and Simon C. Benjamin, and Xiao Yuan, Variational algorithms for linear algebra, arXiv preprint arXiv:1909.03898 (2019).

[54] Tyson Jones, Anna Brown, Ian Bush, and Simon C. Benjamin, Quest and high performance simulation of quantum computers, Sci. Rep. **9**, 10736 (2019).

[55] I. Alonso Calafell, J. D. Cox, M. Radonjic, J. R. M. Saavedra, F. J. García de Abajo, L. A. Rozema, and P. Walther, Quantum computing with graphene plasmons, Npj Quantum Inf. **5**, 37 (2019).

[56] Christopher Chamberland and Andrew W. Cross, Fault-tolerant magic state preparation with flag qubits, Quantum **3**, 143 (2019).

[57] http://dx.doi.org/10.5281/zenodo.22558.