Verifying RLC Power Grids with Transient Current Constraints

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***Abstract*—Vectorless power grid verification is a powerful method that evaluates worst-case voltage noises without detailed current waveforms using optimization techniques. It is extremely challenging when considering RLC power grids because inductors are difficult to tackle and multiple time steps should be evaluated after the discretization of the system equation. In this paper, we study integrated RLC power grids with both VDD and GND networks, and introduce transient constraints to restrict the waveform of each current source for sign-off verification. We rigorously prove that the vectorless verification can be decomposed into two subproblems—the well-studied power grid transient analysis problem and a linear programming (LP) problem that optimizes an affine function of currents under current constraints—and propose to verify the power grid by transient simulation and noise optimization. A variable reduction algorithm is further proposed to generate reduced-size LP problems with a user-specified error tolerance, so that the conservative bounds of voltage noises can be computed efficiently. Experimental results show that the proposed algorithm achieves significant speedup (e.g., up to more than 100× with 5 mV error) over the standard LP solver in solving the LP problems, and the proposed transient constraints make the noise estimations more realistic.**

***Index Terms*—Current constraint, power grid, vectorless verification, voltage drop.**

I. Introduction

As TECHNOLOGY scaling continues, power supply noises become increasingly important in modern chip designs, since the shrinking interconnect size leads to larger IR drops, and the high operating frequency results in a substantial amount of Ldi/dt noises. Moreover, as supply voltages are lowered to reduce power consumption, while subthreshold voltages are decreased for better performance, the gates have smaller noise margins, thus making them more vulnerable to power supply noises than ever before. Hence, in order to ensure a robust chip design, it is indispensable to verify that the power grid is safe, i.e., the power supply noises in the grid are within some acceptable range for all possible runtime situations to avoid logic errors and timing violations. This procedure is typically referred to as power grid verification. Due to the increasing complexity of modern chips, power grid verification has become very challenging, and plenty of work has been done to explore efficient solutions [1]–[25].

Many power grid verification methods are based on simulation. Typically, the power gird is modeled as an RC/RLC circuit with voltage supplies and current sources, which represent the current drawn by the underlying circuitry. Using waveforms of current sources, one can simulate the power grid to evaluate nodal voltages. Lots of algorithms have been proposed for efficient simulation of power grids [1]–[6]. However, as there are too many current sources with different patterns, it is computationally prohibitive to simulate all possibilities. More importantly, since we have to provide detail current waveforms extracted from the circuit for simulation, simulation-based methods can only be applied when the circuit design is done, while early power grid verification is preferable in practice for ease of grid modification.

To assist power grid verification, vectorless approaches have been proposed [7]–[19]. These approaches use current/power constraints to restrict the feasible set of all possible current waveforms, and then evaluate the worst-case voltage noises by solving optimization problems, which are usually large-scale linear programming (LP). [8] further introduces integer variables to model the uncertain working modes of circuit blocks, and formulates integer linear programming (ILP) problems for grid verification. However, ILP problems are very difficult to solve for large-scale power grids, and most works focus on solving LP problems subject to current/power constraints.

The initial vectorless approach [7] considers the DC analysis model, and it is extended to handle RC and RLC power grids in [9] and [10], respectively. For efficient verification of power grids, [11] uses an approximate inverse technique to generate a reduced-size LP problem for each node, [12] designs a hierarchical matrix inversion algorithm to compute the inverse of the power grid matrix, [13] and [14] propose convex dual algorithms to solve the LP problem fast, [15] exploits the dominance relations among node voltage noises to reduce the number of LP problems, and [16] proposes a fast approach to compute the bounds of voltage noises in an RLC power grid. Moreover, it is proposed in [17] that the VDD network and the GND network of the power grid should be verified together, because their voltage noises have mutual effect through the decoupling capacitors. Among the aforementioned studies, only a few consider RLC power grids as the inductors are difficult to tackle, and all of them are based on steady-state current constraints without considering the transient behaviors, but doing so may be too pessimistic.

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Hierarchical power constraints are recently proposed in [18] for more realistic RLC power grid verification. Due to the hierarchical structure of constraints, the LP problems can be solved very efficiently in $O(n \log n)$ time by a sorting-deletion algorithm. Then, the computational cost is mainly due to formulating the LP problems, and it is further improved in [19] by using model order reduction. However, these studies only consider the VDD network, and cannot be extended to verify both VDD and GND networks, because the LP problems with extra equality constraints, which relate the current sources in VDD and GND networks, cannot be solved by the sorting-deletion algorithm.

In this paper, we consider an integrated RLC power grid model with both VDD and GND networks, and propose to perform sign-off verification with novel transient current constraints. The main contributions are as follows.

1) Novel transient current constraints are proposed to restrict the current waveforms for more realistic scenarios, leading to less pessimistic voltage noise predictions.
2) A general methodology to verify RLC power grids by transient simulation and noise optimization is developed, so that efficient power grid analysis algorithms can be leveraged for vectorless verification. This methodology eliminates the verification difficulty introduced by inductors, since inductors can be properly handled during transient simulation. We rigorously prove that the voltage noise at a node, either at a particular time point or cumulatively over a time interval, can be represented as an affine function of current excitations, which enables us to decompose the vectorless verification problem into two orthogonal subproblems. The first subproblem is a power grid transient analysis problem that computes the affine function, which can be solved efficiently by existing power grid analysis algorithms. The second subproblem is an LP problem that optimizes the affine function under current constraints, which is difficult to solve for practical power grids.
3) A variable reduction algorithm is proposed for solving the LP problem. It removes insignificant current variables according to a user-specified error tolerance, so that the resulting reduced-size LP problem can be efficiently solved by standard LP solvers to obtain conservative bounds of voltage noises. Results show that the proposed algorithm significantly speeds up solving the LP problem for vectorless verification.

Different from previous works [16] and [17], which compute bounds of voltage noises based on DC current constraints (i.e., local, global and equality constraints detailed in Section II-B) only, the proposed approach solves the exact worst-case voltage noises under both DC and transient current constraints. In other words, we study the exact approach for vectorless verification of RLC power grids with more realistic constraint settings. The verification techniques of [16] and [17] cannot be extended to handle transient current constraints, because they iteratively compute bounds of voltage noises at advancing time steps till convergence. The approximate inverse technique [11] may be applied for verifying RLC power grids, but it suffers the major limitation that there is no well-defined accuracy guarantee. Hence, we propose to perform transient simulation to setup the LP problem, so that the computed voltage noise estimations are accurate. Prior works [18] and [19] investigate similar problem but limit the current/power constraints to hierarchical structure for efficient solution of the LP problem, while the proposed approach targets more general constraint settings.

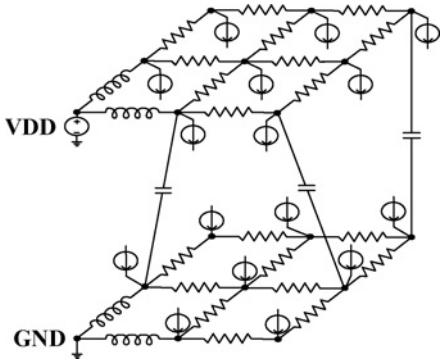

Fig. 1. RLC power grid model.

The rest of this paper is organized as follows. Section II introduces the RLC power grid model and current constraints. Section III proposes vectorless verification with novel transient current constraints. The methodology for vectorless verification is presented in Section IV, and the variable reduction algorithm is detailed in Section V. After experimental results are shown in Section VI, we conclude the paper in Section VII. This paper is an extension of our previous work [20].

II. Background

A. RLC Power Grid Model

We consider an integrated RLC power grid model as illustrated in Fig. 1. It consists of resistors, inductors, capacitors, current sources, VDD and GND pads. Each branch is represented by a resistor, or an inductor, or a capacitor. As this grid contains both VDD and GND networks, we refer to the nodes in the VDD network as *supply nodes*, and the nodes in the GND network as *ground nodes*. Resistors and inductors are only located between two supply nodes or two ground nodes, while capacitors are only located between a supply node and a ground node. For simplicity of illustration, Fig. 1 only shows at most a single capacitor connected with a node. However, it is assumed that a node can be connected with multiple capacitors. The current sources attached to the grid model the behavior of the underlying circuitry, which draws current from the VDD network and injects current to the GND network. In this paper, we assume a single supply voltage, while this RLC power grid model and the proposed vectorless verification approach are also applicable for power grids with multiple supply voltages.

Let n be the total number of nodes that are not VDD/GND pads in the power grid, $u_j(t)$ and $I_j(t)$ be the nodal voltage and the current source at node $j = 1, 2, 3, \ldots, n$, respectively. It is assumed that $I_j(t) = 0$ if node j does not have a current

source attached, and the positive direction of current is from VDD to GND. Let $\mathbf{I}(t)$ be the $n \times 1$ vector of current sources, and $\widehat{\mathbf{I}}(t)$ be the $n \times 1$ vector representing the incoming current source of each node, i.e., its jth element $\widehat{I}_j(t)$ is defined as

$$\widehat{I}_j(t) = \begin{cases} -I_j(t), & \text{if node } j \text{ is a supply node,} \\ I_j(t), & \text{if node } j \text{ is a ground node.} \end{cases} \quad (1)$$

Let $\mathbf{v}(t)$ be the $n \times 1$ vector of voltage noises with its jth element

$$v_j(t) = \begin{cases} u_j(t) - vdd, & \text{if node } j \text{ is a supply node,} \\ u_j(t), & \text{if node } j \text{ is a ground node} \end{cases}$$

where vdd is the supply voltage. As derived in [20], the system equation of the power grid can be formulated as

$$\mathbf{L}\mathbf{v}(t) + \mathbf{G}\mathbf{v}'(t) + \mathbf{C}\mathbf{v}''(t) = \left(\widehat{\mathbf{I}}(t)\right)' \quad (2)$$

where $\mathbf{G}$ is the $n \times n$ conductance matrix, $\mathbf{L}$ is the $n \times n$ matrix similar to the conductance matrix but representing inductance links with its elements being the reciprocals of inductance values, and $\mathbf{C}$ is the $n \times n$ matrix similar to the conductance matrix but representing capacitance links.

Using the backward Euler method or the trapezoidal rule [26], (2) can be discretized in time and rearranged as

$$\begin{aligned} &\left(\mathbf{G} + \Delta t\mathbf{L} + \frac{1}{\Delta t}\mathbf{C}\right)\mathbf{v}(t) = \widehat{\mathbf{I}}(t) - \widehat{\mathbf{I}}(t - \Delta t) + \\ &\left(\mathbf{G} + \frac{2}{\Delta t}\mathbf{C}\right)\mathbf{v}(t - \Delta t) - \frac{\mathbf{C}}{\Delta t}\mathbf{v}(t - 2\Delta t), \text{ or} \\ &\left(\mathbf{G} + \frac{\Delta t}{2}\mathbf{L} + \frac{2}{\Delta t}\mathbf{C}\right)\mathbf{v}(t) = \widehat{\mathbf{I}}(t) - \widehat{\mathbf{I}}(t - 2\Delta t) \\ &\quad + \left(\frac{4}{\Delta t}\mathbf{C} - \Delta t\mathbf{L}\right)\mathbf{v}(t - \Delta t) + \left(\mathbf{G} - \frac{\Delta t}{2}\mathbf{L} - \frac{2}{\Delta t}\mathbf{C}\right) \\ &\quad \mathbf{v}(t - 2\Delta t) \end{aligned} \quad (3)$$

respectively, where Δt is the time step. Clearly, these system equations are similar to the DC analysis equation $\mathbf{G}\mathbf{v} = \mathbf{I}$, where the left-hand-side power grid matrix is a combination of R/L/C components, and the right-hand-side vector is computed from current and previous $\mathbf{I}/\mathbf{v}$ states. In this paper, we employ the trapezoidal rule for grid verification since it has better accuracy. For simplicity of notations, we define $n \times n$ matrix $\mathbf{A}$, $\mathbf{B}$ and $\mathbf{D}$ as

$$\mathbf{A} = \mathbf{G} + \frac{\Delta t}{2}\mathbf{L} + \frac{2}{\Delta t}\mathbf{C}, \ \mathbf{B} = \frac{4}{\Delta t}\mathbf{C} - \Delta t\mathbf{L},$$

$$\mathbf{D} = \mathbf{G} - \frac{\Delta t}{2}\mathbf{L} - \frac{2}{\Delta t}\mathbf{C}.$$

Note that $\mathbf{A}$ is a symmetric $\mathcal{M}$-matrix, so $\mathbf{A}$ is invertible and $\mathbf{A}^{-1}$ is symmetric. $\mathbf{B}$ and $\mathbf{D}$ are also symmetric due to the fact that $\mathbf{G}$, $\mathbf{L}$ and $\mathbf{C}$ are symmetric. Therefore, (3) can be simplified and rearranged as

$$\mathbf{v}(t) = \mathbf{A}^{-1}\left(\widehat{\mathbf{I}}(t) - \widehat{\mathbf{I}}(t - 2\Delta t) + \mathbf{B}\mathbf{v}(t - \Delta t) + \mathbf{D}\mathbf{v}(t - 2\Delta t)\right) \quad (4)$$

which represents the voltage noises at time t as a function of current excitations and the voltage noises at previous time steps, and it will be used to verify the voltage noise across the power grid.

B. Current Constraints

To capture the infinite many current waveforms in the power grid, we employ the framework of current constraints. As studied in [17], the current waveforms of the power grid including both VDD and GND networks can be modeled by three types of constraints: *local constraints*, *global constraints*, and *equality constraints*.

Since the maximum value of each current source is bounded, local constraints are introduced to define an upper bound for individual current source

$$0 \le \mathbf{I}(t) \le \mathbf{I}_L, \forall t, \text{ or } 0 \le \mathbf{I}(k\Delta t) \le \mathbf{I}_L, \forall k,$$

where $\mathbf{I}_L \ge 0$ is an $n \times 1$ upper bound vector. In practice, it is never the case that all the gates or cells draw their peak currents simultaneously. Therefore, global constraints are introduced to define upper bounds for groups of current sources, i.e., the total current drawn by circuit blocks

$$\mathbf{U}\mathbf{I}(t) \le \mathbf{I}_G, \forall t, \text{ or } \mathbf{U}\mathbf{I}(k\Delta t) \le \mathbf{I}_G, \forall k.$$

Let m be the number of global constraints, then U is an $m \times n$ 0/1 matrix indicating the assignments of current sources to groups, and $\mathbf{I}_G \ge 0$ is an $m \times 1$ upper bound vector.

To verify both VDD and GND networks, we need to ensure that the current flowing out of the VDD network is equal to the current flowing into the GND network. For a circuit block, this is also true if the input and output currents are negligible. If we assume that there are b circuit blocks satisfying this equality relationship, then the equality constraints can be formulated as

$$\mathbf{E}\mathbf{I}(t) = 0, \forall t, \text{ or } \mathbf{E}\mathbf{I}(k\Delta t) = 0, \forall k$$

where $\mathbf{E}$ is a $b \times n$ matrix consisting of ± 1s and 0s. For each circuit block, +1s and -1s correspond to the current sources that are attached to the VDD and GND network, respectively, while 0s correspond to other current sources.

Except for the afore-mentioned constraints, some other constraints have also been proposed to characterize current waveforms. Ferzli *et al.* introduce *max delta constraints* [23] to bound the change in current between successive time units. Moreover, [24] uses *current slope constraints* to bound the minimum current transition time. Both of these constraints restrict the transition characteristics of current sources. In addition, *hierarchical power constraints* are proposed in [18] to bound the power consumption of circuit blocks.

III. Vectorless Verification with Transient Current Constraints

In this section, we propose to perform vectorless verification with transient current constraints. Section III-A introduces transient current constraints, Section III-B presents the problem formulation, and a case study is presented in Section III-C.

A. Transient Current Constraints

The current excitations at a particular time t is well defined by local, global and equality constraints. However, these constraints can not model the transient behavior of current sources.

When verifying the power grid, ignoring the transient behavior will lead to pessimistic estimation of the voltage noise, which is caused by unrealistic transient waveforms. For example, consider a node that supplies a gate in a power grid. If we evaluate the voltage noise without considering the transient characteristic of the load current, the worst-case voltage noise may be achieved when the gate draws the maximum current over a long time period, which is never the case.

In order to capture the transient behavior of current sources, we propose novel *transient constraints* to restrict the total amount of current (or more exactly charge) that each current source can draw within a time interval, i.e., a number of continuous time steps. Let N_{ts} be the number of time steps under consideration, then transient constraints can be formulated as

$$\int_0^{N_{ts}\times\Delta t} \mathbf{I}(t)dt \le \mathbf{I}_T \times \Delta t, \text{ or } \sum_{k=1}^{N_{ts}} \mathbf{I}(k\Delta t) \le \mathbf{I}_T$$

where $\mathbf{I}_T \ge 0$ is an $n \times 1$ upper bound vector, and the integration operation is element-wise. For each current source, the transient constraint can be viewed as its power constraint over the time interval. Different from hierarchical power constraints [18], which restrict the power consumption of circuit blocks in a hierarchical manner, transient constraints bound the power consumption of individual current source.

To extract these transient constraints from the underlying circuitry, we must analyze the circuit to derive the maximum amount of switching instants for each gate/cell within N_{ts} time steps, then translate these switching instants into current waveforms, and finally discretize the waveform to get transient upper bounds. As switching activity analysis has already been studied in [21] and [22] to generate realistic stimuli for power grid analysis, we can follow these works to compute $\mathbf{I}_T$.

Theoretically, a combination of all kinds of constraints can better characterize the feasible current excitations for vectorless power grid verification. However, in practice, it may not be possible to verify the grid with all of these constraints, since it is often too computationally expensive or some constraints are not available. Hence, different constraint settings are employed for different applications. In this paper, we consider the sign-off verification of power grids with local constraints, global constraints, equality constraints, and transient constraints, while the proposed vectorless verification approach can also be extended to handle other constraints.

B. Problem Formulation

As studied in [10] and [17], the nodal voltage of an RC/RLC power grid can fluctuate in both directions, i.e., overshot and voltage drop in the VDD network, ground bounce and undershot in the GND network. In many cases, overshot and undershot cannot be neglected. They can be even comparable to voltage drop and ground bounce as shown by the case study in Section III-C and the experimental results in Table II. To verify the power grid conservatively, we need to evaluate the worst-case voltage noises in both directions.

Assume that there is no current excitation for all $t \le 0$, so that $\mathbf{v}(t) = 0$, $\forall t \le 0$. Consider N_{ts} time steps, then the vectorless verification is to solve the following optimization problem for each node $1 \le j \le n$

$$\begin{aligned}&\text{Maximize/Minimize } v_j(t),\ \forall t = k'\Delta t, 1 \le k' \le N_{ts}, \quad (5)\\ &\text{subject to: } \forall 1 \le k \le N_{ts}, \mathbf{v}(k\Delta t) = \mathbf{A}^{-1}\Big(\widehat{\mathbf{I}}(k\Delta t) - \\ &\quad \widehat{\mathbf{I}}\big((k-2)\Delta t\big) + \mathbf{B}\mathbf{v}\big((k-1)\Delta t\big) + \mathbf{D}\mathbf{v}\big((k-2)\Delta t\big)\Big),\\ &\quad 0 \le \mathbf{I}(k\Delta t) \le \mathbf{I}_L, \mathbf{U}\mathbf{I}(k\Delta t) \le \mathbf{I}_G, \mathbf{E}\mathbf{I}(k\Delta t) = 0,\\ &\quad \text{and } \sum_{k=1}^{N_{ts}} \mathbf{I}(k\Delta t) \le \mathbf{I}_T\end{aligned}$$

where $\widehat{\mathbf{I}}(t)$ is defined in (1), and it represents the incoming current source of each node. By maximizing the voltage noise, we get the worst-case overshot or ground bounce. By minimizing the voltage noise, we obtain the worst-case voltage drop or undershot. Clearly, two LP problems need to be solved for each node at each time step. There is a group of constraints at each time step except for the transient constraints, resulting in complicate LP problems.

According to [10], the optimization problems at time $t - \Delta t$ are subproblems of the optimization problems at time t. For each node, the magnitude of the worst-case voltage noise is a nondecreasing function for all $t \ge 0$, and this is also proved in [18]. Therefore, we only need to solve two LP problems for each node at time $t = N_{ts}\Delta t$ to verify the grid. For each node $1 \le j \le n$

$$\begin{aligned}&\text{Maximize/Minimize } v_j(N_{ts}\Delta t), \quad (6)\\ &\text{subject to the same set of constraints as stated in (5).}\end{aligned}$$

Although most works focus on solving the worst-case voltage noise at each node, it is proposed in [25] that verifying the integral of voltage noise (or the mean voltage noise) is more important, because a sharp voltage noise may not affect timing, but a large cumulative voltage noise will. Let us still consider N_{ts} time steps, then the problem for verifying the integral of voltage noise can be formulated as follows. For each node $1 \le j \le n$

$$\begin{aligned}&\text{Maximize/Minimize } \sum_{k=1}^{N_{ts}} v_j(k\Delta t), \quad (7)\\ &\text{subject to the same set of constraints as stated in (5).}\end{aligned}$$

However, it is very challenging to solve either (6) or (7) directly, because the constraints are too complicated, especially the relationships between voltage noises and current excitations. As there are $2n$ LP problems and n is usually large for practical power grids, such LP problems have to be solved very efficiently.

C. Case Study

Before presenting the proposed approach for vectorless verification, we use a case study to demonstrate the importance of vectorless verification with transient constraints.

Consider the simple RLC power grid shown in Fig. 2, we are in particular interested in the voltage noise at node **j**. Since power grid can be viewed as a linear time-invariant (LTI) system, the voltage noise at each node is the sum of voltage noises caused by individual current source (assuming

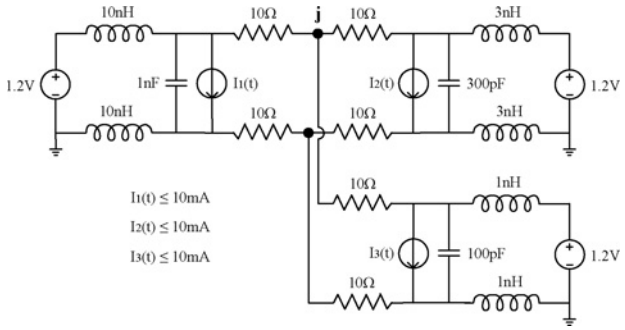

Fig. 2. Simple RLC power grid.

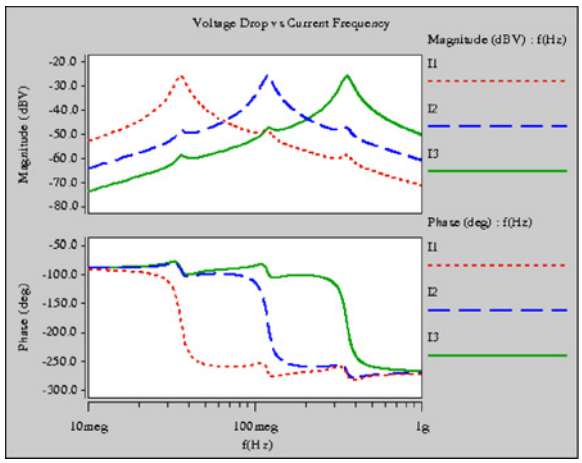

Fig. 3. Frequency response of the voltage noise at node j for each current source.

that other current sources are 0). For this simple grid, the voltage noise at node **j** is attributable to the response of three current sources independently. As shown in Fig. 3, the voltage noise has different frequency response corresponding to each current source, the worst-case current pattern would be a combination of current waveforms at different frequencies with specific phases. However, such worst-case current excitation is not obvious from the standpoint of designers, and it can only be solved under the optimization framework of vectorless verification. Although some realistic current pattern can be extracted for power grid analysis if the circuit design is completed, the pattern extraction is mainly based on the circuit and often overlooks the characteristics of the grid, so the resulting voltage noise estimation may be optimistic. Therefore, vectorless verification is a critical technique to ensure robust power grid design. Except for early power grid verification, it can also serve as an alternative approach to estimate the conservative voltage noise for sign-off verification.

Using time step $\Delta t = 10$ ps and the number of time steps $N_{ts} = 10\,000$, we evaluate the worst-case voltage noise of node **j** at $t = 100$ ns by solving the vectorless verification problem (6). Except for the local constraints that define an upper bound of 10 mA for the three current sources, a transient constraint $\sum_{k=1}^{10\,000} I(k \times 10\,\text{ps}) \leq 10\,000$ mA is specified for each current source to restrict the transient current waveform. As illustrated in Figs. 4 and 5, the computed worst-case current waveforms without transient constraints are regular periodic square waves except I3. Theoretically, the exact worst-case waveforms of I3 without transient constraints should also be regular and periodic like the current pattern from $t = 70$ to 100 ns, the computed worst-case current patterns are not regular because of the round-off error. With transient constraints, the current waveforms are restricted to more realistic scenarios for noise estimation as shown in Figs. 4 and 5. It is worth noting that the worst-case current waveforms with transient constraints have less pulses with possibly smaller pulse width compared to those without transient constraints. The kept pulses under transient constraints are close to the end of the time interval, because the worst-case voltage noise (at $t = 100$ ns) is mainly due to the most recent current excitations. The verification without transient constraints leads to a 35.6% overestimation on the voltage drop and a 38.8% overestimation on the overshot. In practice, such overestimation depends on grid structure and constraints, and may vary case by case. To make more realistic voltage noise predictions, it is important to employ transient constraints for vectorless verification.

IV. Proposed Methodology

In this section, we first introduce two important properties of the system equation in Section IV-A, formulate the expression of voltage noises in Section IV-B, then present the problem decomposition in Section IV-C, and finally propose the methodology for vectorless verification in Section IV-D.

A. Properties of System Equation

Based on the initial condition that the power grid has no stimulus when $t \leq 0$, we can write the system equation of the power grid at different time steps according to (4). For example, at time $t = \Delta t, 2\Delta t,$ and $3\Delta t$, we have

$$\begin{aligned}
\mathbf{v}(\Delta t) &= \mathbf{A}^{-1}\widehat{\mathbf{I}}(\Delta t),\\
\mathbf{v}(2\Delta t) &= \mathbf{A}^{-1}\left(\widehat{\mathbf{I}}(2\Delta t) + \mathbf{B}\mathbf{v}(\Delta t)\right)\\
&= \mathbf{A}^{-1}\widehat{\mathbf{I}}(2\Delta t) + \mathbf{A}^{-1}\mathbf{B}\mathbf{A}^{-1}\widehat{\mathbf{I}}(\Delta t),\\
\mathbf{v}(3\Delta t) &= \mathbf{A}^{-1}\left(\widehat{\mathbf{I}}(3\Delta t) - \widehat{\mathbf{I}}(\Delta t) + \mathbf{B}\mathbf{v}(2\Delta t) + \mathbf{D}\mathbf{v}(\Delta t)\right)\\
&= \mathbf{A}^{-1}\widehat{\mathbf{I}}(3\Delta t) + \mathbf{A}^{-1}\mathbf{B}\mathbf{A}^{-1}\widehat{\mathbf{I}}(2\Delta t) +\\
&\quad \left(\mathbf{A}^{-1}\mathbf{B}\mathbf{A}^{-1}\mathbf{B}\mathbf{A}^{-1} + \mathbf{A}^{-1}\mathbf{D}\mathbf{A}^{-1} - \mathbf{A}^{-1}\right)\widehat{\mathbf{I}}(\Delta t).
\end{aligned}$$

Generally, we have the following lemma.

Lemma 1: There exist a unique series of $n \times n$ matrices $\mathbf{H}_1, \mathbf{H}_2, \ldots, \mathbf{H}_k, \mathbf{H}_{k+1}, \ldots,$ such that $\forall k \geq 1$, we have

$$\begin{aligned}
\mathbf{v}(k\Delta t) &= \sum_{p=1}^{k} \mathbf{H}_p \widehat{\mathbf{I}}\left((k+1-p)\Delta t\right) \qquad (8)\\
&= \mathbf{H}_1\widehat{\mathbf{I}}(k\Delta t) + \mathbf{H}_2\widehat{\mathbf{I}}\left((k-1)\Delta t\right) + \cdots + \mathbf{H}_k\widehat{\mathbf{I}}(\Delta t).
\end{aligned}$$

Proof: According to the expression of $\mathbf{v}(\Delta t)$, $\mathbf{v}(2\Delta t)$, and $\mathbf{v}(3\Delta t)$, we have

$$\mathbf{H}_1 = \mathbf{A}^{-1},\ \mathbf{H}_2 = \mathbf{A}^{-1}\mathbf{B}\mathbf{A}^{-1}, \qquad (9)$$

$$\mathbf{H}_3 = \mathbf{A}^{-1}\mathbf{B}\mathbf{A}^{-1}\mathbf{B}\mathbf{A}^{-1} + \mathbf{A}^{-1}\mathbf{D}\mathbf{A}^{-1} - \mathbf{A}^{-1}. \qquad (10)$$

Based on (4), we can infer that

$$\mathbf{H}_k = \mathbf{A}^{-1}(\mathbf{B}\mathbf{H}_{k-1} + \mathbf{D}\mathbf{H}_{k-2}), \forall k \geq 4. \qquad (11)$$

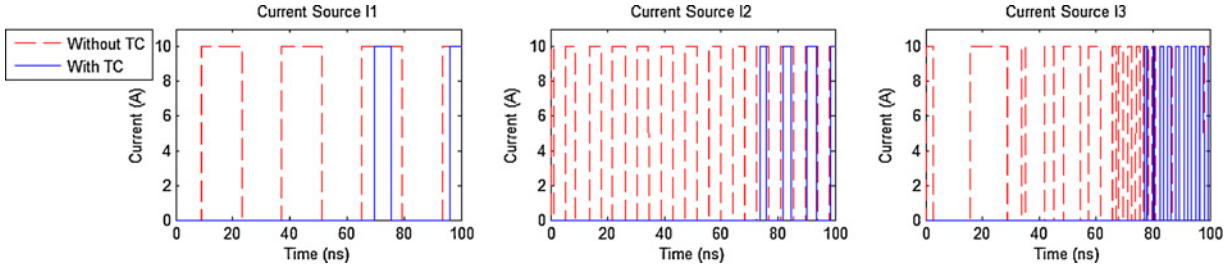

Fig. 4. Worst-case current waveforms for the maximum voltage drop with and without transient constraints (TC). The maximum voltage drops with and without TC are 61.8 and 83.8 mV, respectively. Ignoring TC leads to a 35.6% overestimation on the voltage drop.

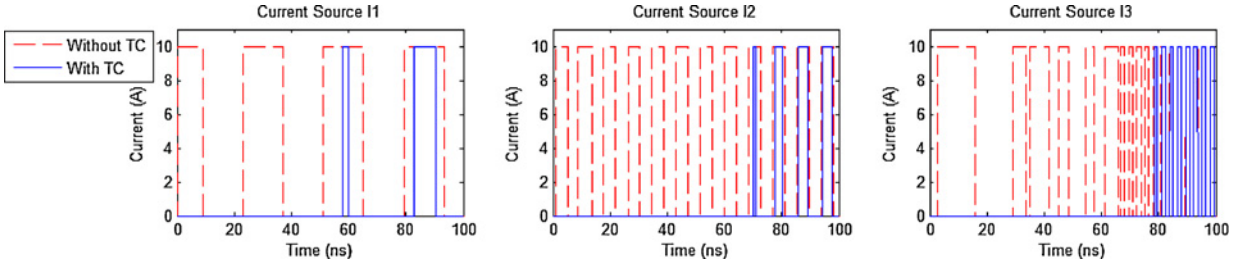

Fig. 5. Worst-case current waveforms for the maximum overshot with and without transient constraints (TC). The maximum overshots with and without TC are 60.8 and 84.4 mV, respectively. Ignoring TC leads to a 38.8% overestimation on the overshot.

Lemma 1 and the formulations of $\mathbf{H}_k$ (9)–(11) can be proved by induction as follows.

Obviously, Lemma 1, (9)–(11) are true when $k = 1, 2, 3, 4$. For $k \geq 5$, assume that

$$\begin{aligned}\mathbf{v}_{k-2} &= \mathbf{H}_1\widehat{\mathbf{I}}_{k-2} + \mathbf{H}_2\widehat{\mathbf{I}}_{k-3} + \cdots + \mathbf{H}_{k-2}\widehat{\mathbf{I}}_1,\\ \mathbf{v}_{k-1} &= \mathbf{H}_1\widehat{\mathbf{I}}_{k-1} + \mathbf{H}_2\widehat{\mathbf{I}}_{k-2} + \cdots + \mathbf{H}_{k-1}\widehat{\mathbf{I}}_1\end{aligned}$$

where $\mathbf{v}_k$ and $\widehat{\mathbf{I}}_k$ represent $\mathbf{v}(k\Delta t)$ and $\widehat{\mathbf{I}}(k\Delta t)$, respectively. Also assume that (9)–(11) hold for $\mathbf{H}_p, \forall 1 \leq p \leq k-1$. Then, according to (4), we have

$$\begin{aligned}\mathbf{v}_k &= \mathbf{A}^{-1}(\widehat{\mathbf{I}}_k - \widehat{\mathbf{I}}_{k-2} + \mathbf{B}\mathbf{v}_{k-1} + \mathbf{D}\mathbf{v}_{k-2})\\ &= \mathbf{A}^{-1}\widehat{\mathbf{I}}_k + \mathbf{A}^{-1}\mathbf{B}\mathbf{H}_1\widehat{\mathbf{I}}_{k-1} +\\ &\quad (\mathbf{A}^{-1}\mathbf{B}\mathbf{H}_2 + \mathbf{A}^{-1}\mathbf{D}\mathbf{H}_1 - \mathbf{A}^{-1})\widehat{\mathbf{I}}_{k-2} + \cdots +\\ &\quad \mathbf{A}^{-1}(\mathbf{B}\mathbf{H}_{k-2} + \mathbf{D}\mathbf{H}_{k-3})\widehat{\mathbf{I}}_2 +\\ &\quad \mathbf{A}^{-1}(\mathbf{B}\mathbf{H}_{k-1} + \mathbf{D}\mathbf{H}_{k-2})\widehat{\mathbf{I}}_1\\ &= \mathbf{H}_1\widehat{\mathbf{I}}_k + \mathbf{H}_2\widehat{\mathbf{I}}_{k-1} + \cdots + \mathbf{H}_{k-1}\widehat{\mathbf{I}}_2 + \mathbf{H}_k\widehat{\mathbf{I}}_1\end{aligned}$$

where (9)–(11) still hold for $\mathbf{H}_p, \forall 1 \leq p \leq k$. Therefore, by induction, Lemma 1 is true, and $\mathbf{H}_k$ satisfies (9)–(11). ■

Lemma 2: $\forall k \geq 1$, $\mathbf{H}_k$ is symmetric.

Proof: Recall that $\mathbf{A}^{-1}$, $\mathbf{B}$, and $\mathbf{D}$ are symmetric, so $\mathbf{H}_1, \mathbf{H}_2$ and $\mathbf{H}_3$ are symmetric. Moreover, it can be verified that $\mathbf{H}_4$ and $\mathbf{H}_5$ are also symmetric. For $k \geq 6$, assume that $\mathbf{H}_p, \forall 1 \leq p \leq k-1$ are symmetric, we have

$$\begin{aligned}\mathbf{H}_{k-2} &= \mathbf{A}^{-1}(\mathbf{B}\mathbf{H}_{k-3} + \mathbf{D}\mathbf{H}_{k-4}) = \mathbf{H}_{k-2}^T\\ &= \mathbf{H}_{k-3}\mathbf{B}\mathbf{A}^{-1} + \mathbf{H}_{k-4}\mathbf{D}\mathbf{A}^{-1},\\ \mathbf{H}_{k-1} &= \mathbf{A}^{-1}(\mathbf{B}\mathbf{H}_{k-2} + \mathbf{D}\mathbf{H}_{k-3}) = \mathbf{H}_{k-1}^T\\ &= \mathbf{H}_{k-2}\mathbf{B}\mathbf{A}^{-1} + \mathbf{H}_{k-3}\mathbf{D}\mathbf{A}^{-1}.\end{aligned}$$

Then

$$\begin{aligned}\mathbf{H}_k &= \mathbf{A}^{-1}(\mathbf{B}\mathbf{H}_{k-1} + \mathbf{D}\mathbf{H}_{k-2})\\ &= \mathbf{A}^{-1}\mathbf{B}(\mathbf{H}_{k-2}\mathbf{B}\mathbf{A}^{-1} + \mathbf{H}_{k-3}\mathbf{D}\mathbf{A}^{-1})\\ &\quad +\mathbf{A}^{-1}\mathbf{D}(\mathbf{H}_{k-3}\mathbf{B}\mathbf{A}^{-1} + \mathbf{H}_{k-4}\mathbf{D}\mathbf{A}^{-1})\\ &= \mathbf{A}^{-1}\mathbf{B}\mathbf{H}_{k-2}\mathbf{B}\mathbf{A}^{-1} + \mathbf{A}^{-1}(\mathbf{B}\mathbf{H}_{k-3}\mathbf{D} +\\ &\quad \mathbf{D}\mathbf{H}_{k-3}\mathbf{B})\mathbf{A}^{-1} + \mathbf{A}^{-1}\mathbf{D}\mathbf{H}_{k-4}\mathbf{D}\mathbf{A}^{-1}.\end{aligned}$$

Since each right-hand-side term is symmetric, $\mathbf{H}_k$ must be symmetric. By induction, Lemma 2 is true. ■

B. Voltage Noise at Each Node

Let $\mathbf{e}_j$ be an $n \times 1$ vector of all 0s except the jth element being 1. Assume that $\widehat{\mathbf{I}}(\Delta t) = \mathbf{e}_j$, and $\widehat{\mathbf{I}}(p\Delta t) = 0, \forall 2 \leq p \leq k$. Define $\mathbf{c}_{j,k}$ as the vector of corresponding voltage noises at time $t = k\Delta t, \forall k \geq 1$. According to (8), we get

$$\mathbf{c}_{j,k} = \mathbf{v}(k\Delta t)|_{\widehat{\mathbf{I}}(\Delta t)=\mathbf{e}_j, \widehat{\mathbf{I}}(p\Delta t)=0, \forall 2\leq p\leq k} = \mathbf{H}_k\mathbf{e}_j.$$

Note that $\mathbf{c}_{j,k}$ is the jth column of $\mathbf{H}_k$. Since $\mathbf{H}_k$ is symmetric, its jth row is equal to $\mathbf{c}_{j,k}^T$. Applying this fact to (8), we can write the voltage noise of each node $1 \leq j \leq n$ at time $t = k\Delta t, \forall k \geq 1$ as

$$\begin{aligned}v_j(k\Delta t) &= \sum_{p=1}^{k} \mathbf{c}_{j,p}^T\widehat{\mathbf{I}}\big((k+1-p)\Delta t\big) \qquad (12)\\ &= \mathbf{c}_{j,1}^T\widehat{\mathbf{I}}(k\Delta t) + \mathbf{c}_{j,2}^T\widehat{\mathbf{I}}\big((k-1)\Delta t\big) + \cdots + \mathbf{c}_{j,k}^T\widehat{\mathbf{I}}(\Delta t),\end{aligned}$$

where the voltage noise is represented as a linear function of current excitations at different time steps.

Consider the power grid as an n-input–n-output LTI system with input current vector $\widehat{\mathbf{I}}(t)$ and output voltage noise vector $\mathbf{v}(t)$. Conventionally, to represent a particular output as an affine function of inputs for such a linear system, we have to compute the impulse response of each input. However,

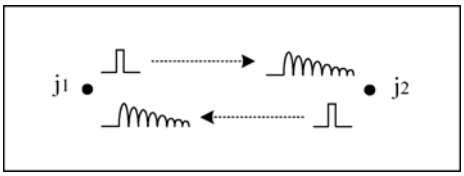

Fig. 6. Symmetric impulse response of two nodes in the power grid.

because of the symmetry of $\mathbf{H}_k$ as stated in Lemma 2, the power grid has symmetric impulse responses. For example, let's consider two nodes j_1 and j_2 shown in Fig. 6. We apply an impulse current excitation at one node, and evaluate the voltage noise response at the other node. These two nodes would have the same response due to symmetry. For each node, its voltage noise responses corresponding to the impulse current excitations at all the nodes are equal to the voltage noise responses of all the nodes corresponding to the impulse current excitation at the node itself. From the circuit perspective, this symmetry is due to the fact that all the R/L/C components are bidirectional and linear. It has been employed to formulate the voltage noise of each node as an affine function of current sources in (12), where $\mathbf{c}_{j,k}$ is the vector of voltage noise responses of all the nodes at time $t = k\Delta t$ corresponding to the impulse current excitation at node j when $t = \Delta t$. Note that (12) can also be viewed as the convolution of impulse responses and inputs.

Summing up (12), we get

$$\sum_{k=1}^{q} v_j(k\Delta t) = \sum_{k=1}^{q} \Big(\sum_{p=1}^{k} \mathbf{c}_{j,p} \Big)^T \widehat{\mathbf{I}}\big((q+1-k)\Delta t\big).$$

Define

$$\widehat{\mathbf{c}}_{j,k} = \sum_{p=1}^{k} \mathbf{c}_{j,p} = \sum_{p=1}^{k} \mathbf{H}_p \mathbf{e}_j = \mathbf{v}(k\Delta t)|_{\widehat{\mathbf{I}}(p\Delta t)=\mathbf{e}_j, \forall 1 \le p \le k}$$

then we have

$$\begin{aligned} \sum_{k=1}^{q} v_j(k\Delta t) &= \sum_{k=1}^{q} \widehat{\mathbf{c}}_{j,k}^T \widehat{\mathbf{I}}\big((q+1-k)\Delta t\big) \\ &= \widehat{\mathbf{c}}_{j,1}^T \widehat{\mathbf{I}}(q\Delta t) + \widehat{\mathbf{c}}_{j,2}^T \widehat{\mathbf{I}}\big((q-1)\Delta t\big) + \cdots + \widehat{\mathbf{c}}_{j,q}^T \widehat{\mathbf{I}}(\Delta t). \end{aligned} \tag{13}$$

It is to be noted that $\widehat{\mathbf{c}}_{j,k}$ is the vector of voltage noises at $t = k\Delta t$ corresponding to a constant current excitation $\widehat{\mathbf{I}}(p\Delta t) = \mathbf{e}_j, \forall 1 \le p \le k$.

C. Problem Decomposition

Applying (12) to represent the voltage noise, we can decompose the optimization problem (6) into the following two subproblems. For each node $1 \le j \le n$

I: Compute $\mathbf{c}_{j,k} = \mathbf{v}(k\Delta t)|_{\widehat{\mathbf{I}}(\Delta t)=\mathbf{e}_j, \widehat{\mathbf{I}}(p\Delta t)=0, \forall 2 \le p \le k}$, (14)
$\forall 1 \le k \le N_{ts}$;

II: Maximize/Minimize

$$v_j(N_{ts}\Delta t) = \sum_{k=1}^{N_{ts}} \mathbf{c}_{j,k}^T \widehat{\mathbf{I}}\big((N_{ts}+1-k)\Delta t\big) \tag{15}$$

subject to: $0 \le \mathbf{I}(k\Delta t) \le \mathbf{I}_L$, $\mathbf{UI}(k\Delta t) \le \mathbf{I}_G$

$$\mathbf{EI}(k\Delta t) = 0, \sum_{k=1}^{N_{ts}} \mathbf{I}(k\Delta t) \le \mathbf{I}_T.$$

Moreover, the optimization problem (7) can also be decomposed similarly by using (13) as the objective function. For each node $1 \le j \le n$

I: Compute $\widehat{\mathbf{c}}_{j,k} = \mathbf{v}(k\Delta t)|_{\widehat{\mathbf{I}}(p\Delta t)=\mathbf{e}_j, \forall 1 \le p \le k}, \forall 1 \le k \le N_{ts}$; (16)

II: Maximize/Minimize

$$\sum_{k=1}^{N_{ts}} v_j(k\Delta t) = \sum_{k=1}^{N_{ts}} \widehat{\mathbf{c}}_{j,k}^T \widehat{\mathbf{I}}\big((N_{ts}+1-k)\Delta t\big) \tag{17}$$

subject to the same set of constraints as stated in (15).

Clearly, the subproblems (14) and (16) are power grid transient analysis problems with an impulse current excitation and a constant current excitation, respectively. Different from conventional power gird transient analysis with realistic current waveforms to evaluate voltage noises, we use impulse or constant current excitation for power grid simulation to characterize voltage noise responses. The subproblems (15) and (17) are still LP but they are much easier to solve compared to (6) and (7), because the objective functions are formulated as linear functions of current excitations. Note that without transient constraints, the LP problems (15) and (17) can be further divided into many smaller LP problems at each time step and solved independently. In comparison with the exact approach of [10], this problem decomposition largely simplifies the vectorless verification of RLC power grids.

In addition, it is to be noted that the proposed problem decomposition is a generic approach for vectorless verification. Although the proofs of fundamental Lemmas 1 and 2 are based on our nodal analysis equation (3) with trapezoidal rule, these lemmas are essential properties of the power grid as an LTI system, and are independent of specific discretization rules and system equations used. Therefore, $\mathbf{c}_{j,k}$ and $\widehat{\mathbf{c}}_{j,k}$ can be computed by any accurate power grid transient analysis algorithms.

D. Methodology

Based on the problem decomposition, we propose to verify each node of the power grid by two orthogonal phases:

1) transient simulation;
2) noise optimization.

We first perform transient simulation with impulse or constant current excitation to compute $\mathbf{c}_{j,k}$ or $\widehat{\mathbf{c}}_{j,k}$ depending on the objective, and then solve two LP problems to evaluate the worst-case voltage noises in both directions. The resultant vectorless verification algorithm is summarized in Fig. 7. As a byproduct of solving the LP problems, the corresponding

Algorithm Vectorless Verification

Input: power grid matrices $\mathbf{G}, \mathbf{L}, \mathbf{C}$, current constraints in (15), Δt, N_{ts}.

Output: The worst-case voltage noises at each node.

1 **for** each node $1 \leq j \leq n$ **do**
2 Perform transient simulation with impulse current vector $\widehat{\mathbf{I}}(\Delta t) = \mathbf{e}_j$ to compute $\mathbf{c}_{j,k}$ in (14)
3 Solve the LP problems (15) to obtain the worst-case voltage noises in both directions
4 **end for**

Fig. 7. Vectorless verification algorithm.

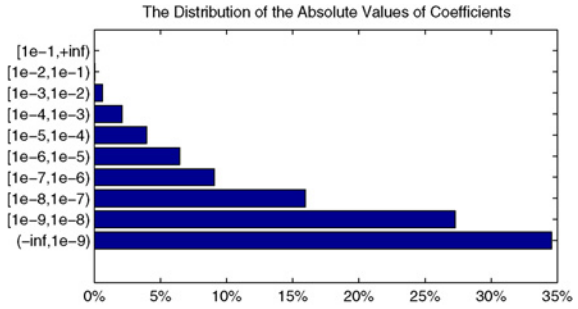

Fig. 8. Distribution of the absolute values of coefficients computed for verifying a random node in an RLC power grid with about 1.1 million nodes (Δt = 10 ps, N_{ts} = 100).

current waveforms leading to the worst-case voltage noises can also be obtained. Such current waveforms are important for designers as they serve as guidelines for grid modification. Therefore, the proposed methodology is capable of evaluating the worst-case voltage noises and identifying corresponding current waveforms.

The full-chip verification involves transient simulation and noise optimization for each node, thus being computationally expensive. However, compared to simulation-based approaches, which may need to enumerate infinite current excitations for theoretical guarantee, the proposed methodology verifies each node by performing transient simulation with a single current vector and solving LP problems. In practice, the proposed methodology can be applied to verify the risky regions of the power grid if full-chip verification is prohibitive.

More importantly, this methodology largely simplifies the vectorless verification problem, and relates power grid transient analysis to vectorless verification, so that existing power grid analysis algorithms can be leveraged. As the left-hand-side matrix of the system equation (3) is a symmetric **M**-matrix, it represents a resistor network, which can be obtained by converting the inductance and capacitance links into resistance branches accordingly. Then, the RLC power grid is reduced to a pure resistor network, which can be simulated very efficiently by using existing power grid analysis algorithms. In our implementation, we employ the preconditioned conjugate gradient (PCG) method [1], [27] with a random-walk based stochastic preconditioner [28] for fast power grid simulation. However, it is still very challenging to solve the LP problems for noise optimization, because practical power grids usually have a large number of current sources, and many time steps need to be evaluated for verification, resulting in prohibitively complicated LP problems.

V. Variable Reduction

To solve the LP problems efficiently, we propose to generate reduced-size LP problems with a user-specified error tolerance. The motivation and principles are introduced in Sections V-A and V-B, respectively. The algorithm details are presented in Section V-C.

A. Motivation

Since computing the magnitude of voltage noise is the mainstream technique for vectorless verification, we consider solving the LP problems (15) to evaluate the worst-case voltage noises in both directions through noise maximization and minimization. The discussion is limited to the noise maximization problem, because the minimization problem can be converted to a maximization problem (by multiplying the objective by -1) and solved accordingly.

Using the definition of $\widehat{\mathbf{I}}(t)$ in (1), we can re-write (15) as a function of $\mathbf{I}(t)$ with updated coefficient vectors. The zero-valued current sources should be dropped[1], so that the number of variables in (15) is equal to $N_{ts} \times N_{cs}$, where N_{cs} is the number of actual current sources. To simplify the notation, let $\mathbf{c}$ be the vector of all coefficients, $\mathbf{I}$ be the vector of current variables at all time steps, $\mathcal{I}_{\mathcal{F}}$ be the feasible set of current excitations defined by the constraints in (15). Then the noise maximization problem in (15) can be represented as

$$\text{Maximize } \mathbf{c}^T\mathbf{I}, \text{ subject to } \mathbf{I} \in \mathcal{I}_{\mathcal{F}}. \tag{18}$$

As this LP problem usually has a large amount of variables for practical power grids, solving it directly with standard LP algorithms often takes huge amount of runtime. It is critical to simplify the LP problem by reducing the number of variables for efficient computation.

Fortunately, the grid locality can be exploited for variable reduction. There are two kinds of locality: 1) spatial locality, i.e., the voltage noise of a node is mainly dependent on the current sources in its neighborhood; and 2) temporal locality, i.e., the voltage noise at a time point is mainly attributable to its recent current excitations. In practice, many coefficients have very small absolute values due to grid locality, so the corresponding current variables do not contribute much to the voltage noise. As shown by the example in Fig. 8, the absolute values of most coefficients are much smaller than 10^{-6}, removing the corresponding current variables from the objective function of the LP problem (18) would not introduce much error to the computed worst-case voltage noise, i.e., these current variables are insignificant for verification. However, simply ignoring such current variables during verification is not reliable, we need a conservative approach with accuracy guarantee for variable reduction.

[1]It is important to do so, because the runtime of standard LP solvers is typically dependent on the number of variables and constraints.

B. Principles

In (18), both $\mathbf{c}^T$ and $\mathbf{I}$ can be partitioned (and reordered if necessary) into two parts, such that

$$\mathbf{c}^T\mathbf{I} = \begin{bmatrix} \mathbf{c}_1 \\ \mathbf{c}_2 \end{bmatrix}^T \begin{bmatrix} \mathbf{I}_1 \\ \mathbf{I}_2 \end{bmatrix} = \mathbf{c}_1^T\mathbf{I}_1 + \mathbf{c}_2^T\mathbf{I}_2$$

where $\mathbf{I}_1$ is the vector of significant current variables, $\mathbf{I}_2$ is the vector of insignificant current variables to be removed, $\mathbf{c}_1$ and $\mathbf{c}_2$ are the corresponding coefficient vectors. Assume that there is no equality constraints relating the current variables of $\mathbf{I}_1$ and $\mathbf{I}_2$, and consider the following two LP problems:

$$\text{Maximize } \mathbf{c}_1^T\mathbf{I}_1, \text{ subject to } \begin{bmatrix} \mathbf{I}_1 \\ \mathbf{0} \end{bmatrix} \in \mathcal{I}_{\mathcal{F}}, \tag{19}$$

$$\text{Maximize } \mathbf{c}_2^T\mathbf{I}_2, \text{ subject to } \begin{bmatrix} \mathbf{0} \\ \mathbf{I}_2 \end{bmatrix} \in \mathcal{I}_{\mathcal{F}}. \tag{20}$$

We call (19) the reduced-size LP problem as it can be viewed as a reduced-size version of (18). Let $(\mathbf{I}^*, v^*)$ be the optimal solution and optimal value of (18), $(\mathbf{I}_1^*, v_1^*)$ and $(\mathbf{I}_2^*, v_2^*)$ be that of (19) and (20), respectively. Then the following lemma must hold:

Lemma 3: $v_1^* \le v^* \le v_1^* + v_2^*$.

Proof: Obviously, $v_1^* = \mathbf{c}_1^T\mathbf{I}_1^* = \mathbf{c}^T \begin{bmatrix} \mathbf{I}_1^* \\ \mathbf{0} \end{bmatrix} \le \mathbf{c}^T\mathbf{I}^* = v^*$. Moreover, since no equality constraints relates the current variables of $\mathbf{I}_1$ and $\mathbf{I}_2$, the optimal value of the following LP problem

$$\text{Maximize } \begin{bmatrix} \mathbf{c}_1 \\ \mathbf{0} \end{bmatrix}^T \mathbf{I}, \text{ subject to } \mathbf{I} = \begin{bmatrix} \mathbf{I}_1 \\ \mathbf{I}_2 \end{bmatrix} \in \mathcal{I}_{\mathcal{F}},$$

is equal to that of (19), so $\begin{bmatrix} \mathbf{c}_1 \\ \mathbf{0} \end{bmatrix}^T \mathbf{I}^* \le v_1^*$. Similarly, we have $\begin{bmatrix} \mathbf{0} \\ \mathbf{c}_2 \end{bmatrix}^T \mathbf{I}^* \le v_2^*$. Hence

$$v^* = \begin{bmatrix} \mathbf{c}_1 \\ \mathbf{0} \end{bmatrix}^T \mathbf{I}^* + \begin{bmatrix} \mathbf{0} \\ \mathbf{c}_2 \end{bmatrix}^T \mathbf{I}^* \le v_1^* + v_2^*.$$

■

Lemma 3 defines theoretical bounds of the maximum voltage noise. In practice, it is desired to identify the insignificant current variables $\mathbf{I}_2$, whose corresponding optimal value v_2^* is acceptably small, so that we can evaluate the worst-case voltage noise by solving the reduced-size LP problem (19) instead of the original LP problem (18).

We employ a user-specified error tolerance δ_{lp} to control the accuracy of the computed worst-case voltage noise, and try to solve the following variable reduction problem:

Consider the LP problem (18), find the maximum set of insignificant current variables $\mathbf{I}_2$, *such that* $v_2^* \le \delta_{lp}$.

Then, by solving the reduced-size LP problem (19) to compute v_1^*, we have

$$v_1^* \le v^* \le v_1^* + \delta_{\text{lp}} \tag{21}$$

where $v_1^* + \delta_{\text{lp}}$ is reported as the conservative bound over the maximum voltage noise.

C. Details

To solve the variable reduction problem, we need to check the condition $v_2^* \le \delta_{\text{lp}}$ for some $\mathbf{I}_2$. However, solving (20) to compute the exact v_2^* would be very challenging because of the large number of variables involved. In order to find a proper set of insignificant current variables efficiently, we choose to compute an upper bound of v_2^* heuristically, and make sure that the computed upper bound is no larger than δ_{lp}, so (21) still holds.

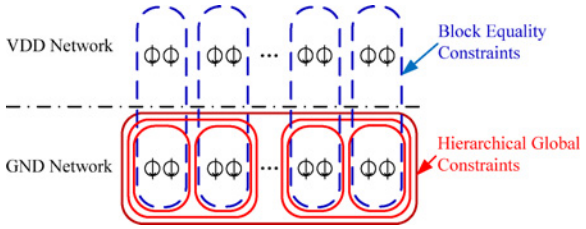

Fig. 9. Equality constraints and global constraints at each time step. Equality constraints relate the current sources in both VDD and GND networks, they are nonoverlapped and defined for individual circuit block. Global constraints are specified hierarchically in the GND network to bound the total current of circuit block(s).

We adopt nonoverlapped equality constraints and hierarchical global constraints shown in Fig. 9, as well as local constraints and transient constraints. It can be seen that equality constraints and global constraints naturally divide the current sources (i.e., the current variables at each time step) into groups. Let b and m be the number of equality constraints and global constraints at each time step, respectively. There are a total of $N_{ts} \times b$ equality constraints and $N_{ts} \times m$ global constraints. Recall that there are $N_{ts} \times N_{cs}$ current variables. Let I_p be the pth current variable. Define sets of indices $\mathcal{S}_k$ as

$$\mathcal{S}_k = \begin{cases} \{p | I_p \text{ is restricted by the } k\text{th equality constraint}\}, \\ 1 \le k \le N_{ts} \times b; \\ \{p | I_p \text{ is restricted by the } (k - N_{ts} \times b)\text{th global} \\ \text{constraint}\}, N_{ts} \times b + 1 \le k \le N_{ts} \times (b + m) \end{cases}$$

where $\mathcal{S}_k$, $N_{ts} \times b + 1 \le k \le N_{ts} \times (b+m)$ also includes indices of current variables of the VDD network, because the current sources in the VDD network are indirectly restricted by global constraints through equality constraints. Every $\mathcal{S}_k$ corresponds to a set of current variables, and no equality constraints relates the current variables of disjoint sets. For each $\mathcal{S}_k$, rewrite the corresponding LP problem (20) as

$$\text{Maximize } v_k = \sum_{p \in \mathcal{S}_k} c_p I_p, \tag{22}$$
$$\text{subject to } \mathbf{I}|_{I_p = 0, \forall p \notin \mathcal{S}_k} \in \mathcal{I}_{\mathcal{F}}$$

where v_k is the voltage noise caused by the corresponding set of current variables, c_p is the pth coefficient. The other current variables $I_p, \forall p \notin \mathcal{S}_k$ are set to 0, and then the constraints can be simplified by removing the zero-valued variables. Nevertheless, solving (22) for each $\mathcal{S}_k$ with standard LP solvers still takes long runtime, because there are $N_{ts} \times (b+m)$ LP problems with complicated constraints (i.e., local, global, equality, and transient constraints).

For fast estimation of the optimal value of (22), we compute its upper bound by solving simplified LP problems, which are obtained by removing equality constraints, transient constraints, and higher level global constraints. For each

$\mathcal{S}_k, 1 \le k \le N_{ts} \times b$

$$\text{Maximize } v_k = \sum_{p \in \mathcal{S}_k} c_p I_p, \quad \text{subject to local constraints only} \tag{23}$$

for each $\mathcal{S}_k, N_{ts} \times b + 1 \le k \le N_{ts} \times (b + m)$

$$\text{Maximize } v_k = \sum_{p \in \mathcal{S}_k} c_p I_p \tag{24}$$

subject to local constraints and hierarchical global constraints that only restrict the current variables I_p, $p \in \mathcal{S}_k$. The solution of (23) can be easily obtained by setting I_p to the maximum value defined by local constraints if $c_p > 0$, and 0 otherwise. Equation (24) can be efficiently solved by the sorting-deletion algorithm [18] as follows. Each I_p is set to 0 if $c_p \le 0$; the other I_ps with $c_p > 0$ are sorted, such that their corresponding c_ps are in nonincreasing order, and then they are set to the maximum feasible value defined by local constraints and hierarchical global constraints sequentially.

Let v_k^* be the optimal value of (22), $\widehat{v}_k$ be the optimal value of (23) and (24). For each set $\mathcal{S}_k$, define the average noise bound per variable

$$\overline{v}_k = \frac{\widehat{v}_k}{|\mathcal{S}_k|}. \tag{25}$$

Let $\mathcal{U}$ be the index set of insignificant current variables, $\widehat{v}_{\text{total}}$ be the aggregate noise bound of selected sets. The variable reduction algorithm can be summarized as shown in Fig. 10. In order to identify sets of insignificant current variables, it first computes $\widehat{v}_k$ and $\overline{v}_k$ for all sets $\mathcal{S}_k$, and then iteratively selects the set with the minimum $\overline{v}_k$ among all feasible candidate sets, so that the total number of identified insignificant current variables can be maximized. Note that the supersets of the selected set must be updated during each iteration to reflect the status change.

Lemma 4: The variable reduction algorithm identifies insignificant current variables with error tolerance δ_{lp}, and the resulting reduced-size LP problem satisfies (21).

Proof: According to Lemma 3 and (21), we only need to show that $v_2^* \le \delta_{\text{lp}}$. The identified set of insignificant current variables is a collection of pairwise disjoint sets of variables, which are chosen iteratively. According to the termination condition of the variable reduction procedure (i.e., line 8 of Fig. 10), these sets satisfy

$$\sum_{\forall \text{ identified sets } \mathcal{S}_k \subseteq \mathcal{U}} \widehat{v}_k \le \delta_{\text{lp}}$$

and can be viewed as a partition of insignificant current variables $\mathbf{I}_2$. By generalizing the proof of Lemma 3 for the partition of $\mathbf{I}_2$, it follows that

$$v_2^* \le \sum_{\forall \text{ identified sets } \mathcal{S}_k \subseteq \mathcal{U}} v_k^* \le \sum_{\forall \text{ identified sets } \mathcal{S}_k \subseteq \mathcal{U}} \widehat{v}_k \le \delta_{\text{lp}}.$$

■

Lemma 5: The time complexity for computing all $\widehat{v}_k$ and $\overline{v}_k$ is $O\big(N_{ts} \times N_{cs}(TotalLevel + \log N_{cs}) + N_{ts} \times (b + m)\big)$, where $TotalLevel$ is the total level of hierarchical global constraints. Each iteration for identifying sets of insignificant current variables takes $O\big(N_{ts} \times (b + m) + TotalLevel\big)$ time.

Algorithm Variable Reduction
Input: coefficients **c** in (18), constraints in (15), δ_{lp}.
Output: the index set of insignificant variables $\mathcal{U}$.

```
1  U ← ∅;
2  v̂_total ← 0;
3  // Compute v̂_k and v̄_k
4  Compute v̂_k, ∀1 ≤ k ≤ N_ts × b by solving (23);
5  Compute v̂_k, ∀N_ts × b + 1 ≤ k ≤ N_ts × (b + m) by
   solving (24) with the sorting-deletion algorithm;
6  Compute v̄_k, ∀1 ≤ k ≤ N_ts × (b + m);
7  // Identify sets of insignificant variables iteratively
8  while ∃ set(s) S_k ⊄ U and v̂_total + v̂_k ≤ δ_lp do
9    Find one such set S_k* with the minimum v̄_k*;
10   U ← U ∪ S_k*;
11   v̂_total ← v̂_total + v̂_k*;
12   // Update supersets of the selected set S_k*
13   for each S_k ⊃ S_k* do
14     S_k ← S_k \ S_k*;
15     v̂_k ← v̂_k − v̂_k*
16     Recompute v̄_k;
17   end for
18 end while
19 Return U;
```

Fig. 10. Variable reduction algorithm.

Proof: Solving (23) to compute $\widehat{v}_k, \forall 1 \le k \le N_{ts} \times b$ takes $O(N_{ts} \times N_{cs})$ time. The sorting-deletion algorithm [18] is employed to compute $\widehat{v}_k, \forall N_{ts} \times b + 1 \le k \le N_{ts} \times (b + m)$. It takes $O\big(N_{ts} \times N_{cs} \log N_{cs}\big)$ time to sort the current variables, and $O(N_{ts} \times N_{cs} \times TotalLevel)$ time to compute the optimal value of (24). Based on the precomputed $\widehat{v}_k$, $\overline{v}_k$ can be calculated in $O(N_{ts} \times (b + m))$ time. Hence, the complexity for computing $\widehat{v}_k$ and $\overline{v}_k$ follows.

There are a total of $N_{ts} \times (b + m)$ candidate sets $\mathcal{S}_k$, and each set has a maximum of $TotalLevel$ supersets. Therefore, in each iteration, it takes $O\big(N_{ts} \times (b + m)\big)$ time to identify a proper set $\mathcal{S}_{k^*}$, and $O(TotalLevel)$ time to update its supersets. Then Lemma 5 follows. ■

VI. Experimental Results

The proposed vectorless verification approach has been implemented in C++, and the LP problems are solved by MOSEK [29], a general optimization software. To evaluate the performance, we generate integrated RLC power grids with 4 metal layers, 1.2V VDD, and various C4 bumps/chip sizes/power consumptions. For each power grid, we extract local constraints from the grid description, generate transient constraints and equality constraints, each of which includes about 100 current sources in the GND network as well as the VDD network, and specify up to 10 global constraints hierarchically. All experiments are carried out on a 64-bit Linux server with 2.67 GHz Intel X5650 processor and 64 GB memory. Although the processor has multiple cores, only a single core is used for experiments.

We apply the proposed variable reduction algorithm with different error tolerances $\delta_{\text{lp}} = 5, 10, 20$ mV to verify synthetic

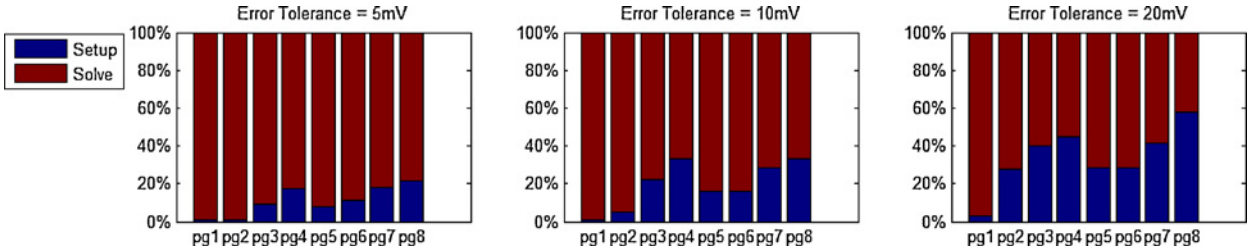

Fig. 11. Runtime break down of noise optimization using the proposed variable reduction algorithm. "Setup" denotes the runtime of the variable reduction procedure. "Solve" represents the runtime of solving the reduced-size LP problems.

TABLE I
AVERAGE RUNTIME PER NODE FOR VECTORLESS VERIFICATION

Power Grids			Simulation	Standard LP Solver	Proposed Variable Reduction Algorithm								
					Error Tolerance δ_{lp} = 5mV			Error Tolerance δ_{lp} = 10 mV			Error Tolerance δ_{lp} = 20 mV		
Name	Nodes	[1]N_{cs}	[2]Time (s)	[3]Time (s)	[4]Variables	[5]Time (s)	[6]×	[4]Variables	[5]Time (s)	[6]×	[4]Variables	[5]Time (s)	[6]×
pg1	3088	1352	0.12	12.41	43646	3.42	3.63	28852	2.63	4.72	10877	1.00	12.38
pg2	11 768	5202	0.46	105.21	84769	16.62	6.33	32130	3.02	34.89	9605	0.52	201.31
pg3	45 928	20 402	1.65	415.16	92093	7.66	54.19	44506	3.03	137.11	29758	1.70	244.12
pg4	71 408	31 752	2.66	612.32	143613	6.32	96.95	74467	3.37	181.87	48672	2.46	248.65
pg5	102 488	45 602	3.80	1064.45	200959	20.84	51.08	111273	10.57	100.71	72949	5.90	180.31
pg6	181 448	80 802	6.84	1846.32	346159	29.18	63.28	202114	20.46	90.24	130296	11.38	162.18
pg7	282 808	126 002	10.98	3455.03	576164	30.15	114.60	345809	19.25	179.48	213325	13.09	263.95
pg8	1 125 608	502 002	45.61	[7]NA	1857217	131.57	NA	1168304	86.40	NA	565071	48.07	NA

[1] the number of current sources;
[2] the runtime of power grid transient simulation;
[3] the runtime of noise optimization by solving the LP problem (15) directly with the standard LP solver (i.e., MOSEK);
[4] the average number of variables in the reduced-size LP problems;
[5] the runtime of noise optimization by using the proposed algorithm, including both variable reduction and solving the reduced-size LP problems;
[6] the speedup of the proposed algorithm relative to the standard LP solver (i.e., MOSEK) for noise optimization;
[7] MOSEK fails to solve the LP problem (15) for pg8.

TABLE II
WORST-CASE VOLTAGE NOISES OF A RANDOM NODE WITH AND WITHOUT TRANSIENT CONSTRAINTS

Power Grids	Node Type	Without Transient Constraints		With Transient Constraints		Overestimation	
		Overshot/ground bounce (mV)	Voltage drop/ undershot (mV)	Overshot/ground bounce (mV)	Voltage drop/ undershot (mV)	Overshot/ground bounce	Voltage drop/ undershot
pg1	ground	39.75	12.39	22.55	12.39	76.27%	0.02%
pg2	supply	18.28	30.63	18.20	21.86	0.45%	40.11%
pg3	ground	14.04	10.51	11.26	10.34	24.69%	1.67%
pg4	supply	10.46	13.65	10.31	11.1	1.39%	22.95%
pg5	ground	15.27	12.26	12.87	12.11	18.65%	1.17%
pg6	supply	17.45	19.98	17.3	17.95	0.82%	11.33%
pg7	ground	20.32	18.02	18.43	17.88	10.24%	0.82%
pg8	supply	21.17	23.13	NA	NA	NA	NA

power grids with time step Δt = 10 ps and the number of time steps N_{ts} = 100, i.e., we evaluate the worst-case voltage noises within 1 ns. For performance comparison, we also compute the exact worst-case voltage noises by solving the LP problem (15) directly with MOSEK. As MOSEK allows to choose between the simplex method and the interior point method to solve LP problems, we experiment with both options but only report the results using the interior point method as it is often faster.

Table I presents the average runtime per node, which is an estimation from solving 100 random nodes for each power gird because it is too time-consuming to verify all the nodes. The runtime can be generally partitioned into two parts: the runtime for power gird transient simulation, and the runtime for noise optimization. It can be seen that the power grid simulation time is very small as the random-walk based PCG method is fairly efficient, but solving the LP problem (15) directly with the standard LP solver (i.e., MOSEK) takes a large amount of runtime, thus being the performance bottleneck of vectorless verification. Fortunately, the proposed algorithm achieves significant speedups over the standard LP solver for noise optimization because of variable reduction, and the resulting runtime for noise optimization is close to the transient simulation time. In general, the proposed algorithm tends to become more effective as the grid size increases, because the grid locality can be better exploited in larger power grids. For each power grid, as the error tolerance increases, the proposed algorithm removes more insignificant current variables, and provides better performance. For example, the

LP problems (15) for verifying pg7 contains $N_{ts} \times N_{cs} = 100 \times 126\,002 \approx 12.6$M current variables. With 5 mV error tolerance, the reduced-size LP problems only have less than 0.6M current variables, achieving about 115× speedup. With 20 mV error tolerance, the variable count further decreases to about 0.2M, leading to 264× speedup.

Moreover, for each power grid, it is observed that the runtime of the variable reduction procedure with different error tolerance values are approximately the same, because most time complexity of variable reduction is due to the computation of $\widehat{v}_k$ as summarized in Lemma 5. Fig. 11 shows the runtime break down of noise optimization using the proposed algorithm. The runtime of variable reduction tends to become increasingly important as grid size increases. In fact, the variable reduction runtime increases monotonically as the grid size becomes larger. With larger error tolerance, its percentage increases because the reduced-size LP problems can be solved more efficiently due to less current variables. The runtime and speedup of noise optimization shown in Table I and Fig. 11 do not show a well-defined trend, because the runtime for solving the reduced-size LP problems varies case by case.

Compared with the approaches in [16] and [17], which compute bounds of voltage noises under DC current constraints, the proposed vectorless verification approach takes more runtime to calculate the exact worst-case voltage noises (with user-specified error margin) based on both DC and transient current constraints. This is due to the fact that our exact approach is more compute-intensive than computing bounds according to [16] and [17], especially with transient constraints. In comparison with the verification approaches with hierarchical power constraints in [18] and [19], the proposed approach takes similar runtime to setup the LP problems (by transient simulation), while it consumes more runtime to solve the LP problems, since our current constraints do not have strict hierarchical structure and the LP problems cannot be solved by the sorting-deletion algorithm. Hence, the variable reduction algorithm is proposed in order to solve the LP problems efficiently.

To demonstrate that omitting transient constraints may result in pessimistic voltage noise prediction, we perform experiments without transient constraints for comparison. Table II shows the worst-case voltage noises of a random node with and without transient constraints. Note that each node has two worst-case voltage noises, i.e., overshot/voltage drop of a supply node, and ground bounce/undershot of a ground node. An interesting phenomenon is that omitting transient constraints leads to significant percentage of overestimation for the voltage drop of a supply node and the ground bounce of a ground node, while it has minor impact on overshots and undershots. This phenomenon is attributable to the fact that the worst-case current waveforms for overshots and undershots nearly satisfy transient constraints over the verification time interval. Generally, with transient constraints, we can get more realistic voltage noise estimations, thus avoiding costly overdesigns of thepower grid.

In summary, the proposed variable reduction algorithm largely accelerates vectorless verification with transient current constraints, and can be applied for verifying practical RLC power grids. One might complain that the synthetic power grids are relatively small, and the per node runtime is large. However, our algorithm is important for at least three reasons. First, the size of the RLC power grid model is dependent on the level of model extraction. In practice, our algorithm can be applied either to parts of the power grid, or to the top-level network of the grid. Second, our algorithm can be easily parallelized since each node is verified independently. Third, as discussed in [18], one can choose to verify a few risky nodes of the grid, e.g., the nodes that are farthest from voltage sources. To take full advantage of the proposed algorithm for better performance, one can start with a large error tolerance value (e.g., 20 mV), and then switch to a smaller error tolerance (e.g., 5 mV) if higher solution accuracy is required. There would be a performance gain if only a small portion of nodes need to be verified with higher accuracy.

VII. Conclusion

In this paper, we studied the vectorless verification of power grids using an integrated RLC power grid model. Our study showed that the vectorless verification of RLC power grids can be divided into two phases: power grid transient simulation and noise optimization. We proposed novel transient constraints to restrict the waveform of each current source for sign-off verification, so that the worst-case voltage noise estimations can be more realistic. Moreover, to solve the noise optimization problem efficiently, we designed a variable reduction algorithm to generate reduced-size LP problems with a user-specified error tolerance. Results showed that our algorithm significantly sped up vectorless verification with transient current constraints, making the verification of large-scale RLC power grids possible.

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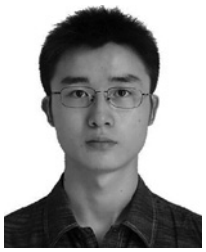

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