Versatile Three-Level FC-NPC Converter With High Fault-Tolerance Capabilities: Switch Fault Detection and Isolation and Safe Postfault Operation

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Abstract—**This paper deals with a hybrid fault-tolerant converter topology. It is performed through the connection of a classical three-phase three-level Neutral Point Clamped (3L-NPC) converter with a fourth three-level Flying Capacitor (3L-FC) leg. The 3L-FC leg actively balances the 3L-NPC neutral point voltage. For normal operation mode, this paper proposes a mathematical design of the filter needed to connect these two different topologies. Experimentally, and thanks to the already existing decoupling capacitors of the 3L-NPC converter, this filter requires the addition of only one low size inductance.**
When one fault of the power switch of the 3L-NPC occurs, the paper proposes hardware reconfiguration technique based on only two fuses and one thyristor per leg allows a safe post-fault operation recovery. This is achieved thanks to a simple fault-detection method and a new technique that combines fault leg isolation and corresponding phase post-fault connection to the neutral point. Also, a dedicated FPGA-based control of the reconfigured converter is synthetized to ensure power system availability under fault operation mode.
The converter fault-tolerant capabilities are addressed through simulation results and original overall experimental validations of the fault detection and isolation and the post-fault operation steps, carried out on a 15 kW prototype converter.

Index Terms—**Multilevel converter, Hybrid converter, Fault detection, Fault isolation, Fault tolerance.**

I. Introduction

During the last decades, multilevel converters have been one of the more worthwhile challenges in power electronic fields. They have enabled power systems to meet increasingly stringent grid and load requirements [1]–[8]. Nowadays, many industrial applications, especially for medium- and high-voltage systems, use multilevel topologies, particularly the Neutral Point Clamped (NPC) one, thanks to its inherent advantages such as high DC-bus voltage, reduced output voltage harmonics, low voltage stress on power switches, and low *dV/dt* ratings [9]–[13].

Recently, the reliability of power converters has become an important issue. In fact, for many applications using standalone converters or on-board systems, fault tolerance is crucial. This is the case in the transportation field (electric vehicles, hybrid electric vehicles, rail, and aerospace), where the power system redundancy has a financial cost and volume limitations and may be technically inappropriate [14]–[16]. In addition, in present-day renewable energy applications, fault tolerance considerations are mandatory since maintenance can be difficult and expensive as in offshore wind farms. Moreover, a large-scale energy production shutdown may cause serious network stability problems and lead to a risk of blackout [17],[18].

Fault tolerance considerations have to be introduced from the converter design step in order to synthesize robust, secure, and fault-tolerant systems that provide operation availability after failure occurrence[19],[20]. Furthermore, the state of the art of power system reliability shows the predominance of the power converter and, in particular, power devices as the origin of the overall system failures [21]–[25]. Several model-based Fault Detection and Isolation (FDI) methods were proposed in literature for linear [26] and nonlinear systems [27]. These methods generally assume that, the control would be able to preserve operation at the nominal equilibrium point until the post-fault mode is reached. This issue is crucial for practical cases such as power converter applications. To overcome this issue, a safe-parking framework was proposed for nonlinear systems [28] and more recently for switched nonlinear ones [29]. Although the distinction between sensor and actuator faults for nonlinear systems was considered [30], the needed FDI time is the main concern of such techniques when applied for power converters, especially for short circuit switch faults. Moreover, a global power converter fault tolerance has to consider technological aspects when dealing with the electric isolation of the faulty power switch and the reconfiguration of the post-fault system issues.

This paper focuses on a hybrid fault-tolerant converter able to detect a power switch fault, isolate the corresponding faulty leg, and recover safe post-fault operation.

In [31]–[33], the authors proposed a fault-tolerant hybrid three-level converter based on the connection of a three-level Flying Capacitor (FC) leg to a three-phase three-level NPC (3L-NPC) converter. Transition from normal mode to faulty mode was ensured by fuses and an additional semi-conductor. This post-fault reconfiguration depends on the faulty NPC IGBT and the fault type (open-circuit or short-circuit). However, fault detection and the method of blowing up fuses were not discussed and the practical implementation issues were not detailed. In [34], the authors show the FC IGBT's

dead time effect on the FC output voltage for this fault tolerant hybrid topology and claim to add an LC filter to overcome this issue.

In this paper, this fault-tolerant topology is sensitively improved. Four new features are proposed: First, a detailed mathematical design of the LC filter is performed. Second, a new and simple PWM control reconfiguration is developed. Third, a novel hardware reconfiguration technique based on fuses and one thyristor is experimentally tested. This new technique is based on an interesting NPC-intrinsic topology feature in order to adapt and simplify the set-up proposed by [33], where two different circuits are needed for a classical two-level converter reconfiguration. Finally, the whole of the fault-tolerance process, including fault detection, fault isolation, and post-fault hardware and control reconfiguration, is experimentally handled and validated.

The second section is dedicated to the hybrid feature of the proposed converter topology. The role of the FC leg is described and a detailed design methodology for the NPC-FC decoupling filter is presented. In the third section, the fault-tolerant FPGA-based PWM strategy is addressed. In the fourth section, a novel high-performance converter-reconfiguration technique is proposed. A comparison between two different fuse technologies is experimentally addressed. Then, the experimental results of post-fault operation mode are discussed. These results are obtained with an FPGA control board and a 15 kW laboratory test-bench. The fault-tolerant reconfiguration process improves the converter reliability and allows power system post-fault operation after the occurrence of an NPC switch fault.

II. Hybrid NPC-FC Converter: Issues and Proposed Solutions

The considered power converter solution consists of a classical three-phase 3L-NPC topology with an added fourth FC leg connected at the neutral point "O", as shown in Fig.1. Note that the proposed topology is equivalent to the connection at the neutral point of two power converters: a three-level FC-based DC/DC converter and a three-level NPC DC/AC converter. Moreover, the hybrid converter is open loop controlled since the close loop control would not affect the hybrid feature of the converter or its fault tolerant capabilities.

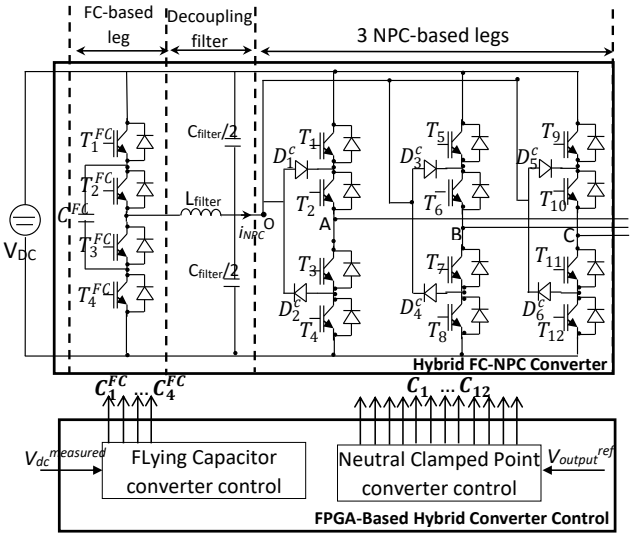


Fig.1. Hybrid FC-NPC converter: topology and control

A. Role of the FC Leg

Under normal operation, the FC leg's main function is to provide the NPC converter with an active neutral point. In fact, a two-cell/three-level FC leg with a 50% ratio leads to an output voltage equal to half of the DC bus value, theoretically with a zero-voltage ripple at the output [35]. This voltage can constitute an efficient active neutral point for the NPC legs. Active neutral point regulation techniques proposed in the literature [36] are interesting because they offer a considerable volume reduction and electrolytic capacitors are replaced by lower size and more reliable and safer film capacitors. However, they involve dedicated control strategies and consequently limit the degrees of freedom of the NPC converter. Fig.2 shows a comparison of the neutral point voltage when the FC leg is controlled with the active balance strategy described above (Fig. 2.b) and the case of a conventional NPC converter with two 600-µF DC bus capacitors s (Fig. 2.a). It proves the effectiveness of the proposed active balance. Furthermore, unlike NPC converters, the proposed hybrid converter allows a very low frequency operation (as for machine start-up cases) and even a multilevel DC/DC chopper operation may be possible by interlacing the NPC legs.

B. Connecting the FC leg to the NPC ones

For a practical implementation and because of mandatory dead-times, the duty cycle of the FC leg will never be precisely equal to 50%, and a low-size high-frequency filter, denoted (L_{filter}, C_{filter}) must be included, as shown in Fig.1. Qualitatively, this filter has two main functions, which are developed below:

- From the NPC leg mid-point to the FC leg: Only the NPC mid-point low-frequency current at three times the modulation frequency has to flow between the two converter parts. Indeed, the high frequency components of this current affect the FC voltage balance especially in the case of identical (or an integer multiple/sub-multiple) switching frequencies of the NPC and FC legs.
- From the FC leg to the NPC leg mid-point: this second-order filter acts on the residual pulse-width voltages of the FC output voltage that are caused by the IGBTs' dead-times.

The hybrid topology converter needs a precise sizing of the LC filter elements, which is developed in the next paragraph.

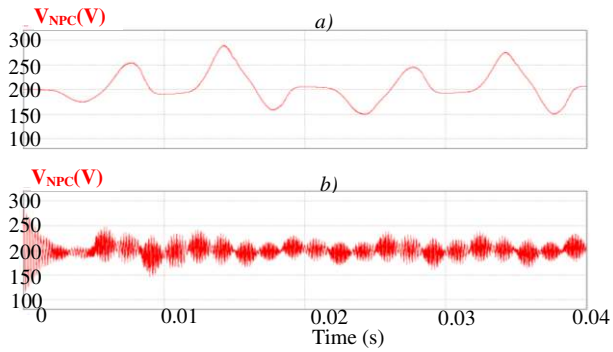


Fig.2. Neutral point voltage V_{DC} = 400 V, load R = 1 Ω, L = 10 mH: a) Conventional three-level NPC converter, b) Proposed three-level hybrid converter with active neutral point balance

C. Sizing Methodology of the Proposed Filter

Three criteria families are fundamental for the LC filter sizing: spectral properties, state variables' ripples, and system behaviour after sudden load disconnection.

i) Spectral constraints: The filter cut-off frequency, F_{filter}, must be chosen to properly filter the residual pulse-width voltages at the FC leg output. The filter cut-off frequency maximum value, denoted F_{filter_max}, has to be equal to the minimum of the NPC leg's frequency, denoted F_{sw_NPC}, and the FC leg's apparent frequency, denoted F_{sw_FC}. Besides, the minimum value of the filter cut-off frequency, denoted F_{filter_min}, is equal to one decade lower than F_{filter_max}, as expressed by Eqs. (1) and (2).

$$F_{filter\_min} = \frac{1}{2.\pi.\sqrt{\left(L_{filter}.C_{filter}\right)_{max}}} \qquad F_{filter\_min} = \frac{Min(F_{SW\_NPC}, F_{SW\_FC})}{10} \tag{1}$$

$$F_{filter\_max} = \frac{1}{2.\pi.\sqrt{\left(L_{filter}.C_{filter}\right)_{min}}} \qquad F_{filter\_max} = Min(F_{SW\_NPC}, F_{SW\_FC}) \tag{2}$$

ii) NPC neutral point voltage and FC output current ripples. First, the neutral point voltage ripple, denoted δV_{NPC}, is generated by the I_{NPC} current (see Fig. 1) and particularly its high frequency components (@ F_{sw_NPC}) when it flows through C_{filter}. Second, the dead-times of the FC leg lead to glitches in its output voltage. These glitches excite the inductance and cause L_{filter} current ripple, which corresponds to the FC output current ripple, denoted δI_{FC}.

The NPC mid-point voltage ripple and the FC output current ripple must be set to admissible values through a smart choice of C_{filter} and L_{filter} values. To perform a precise calculation of δV_{NPC} and δI_{FC}, an analysis of the filter operation is detailed below. In fact, Fig.3 gives a simplified scheme of the principle of the filter.

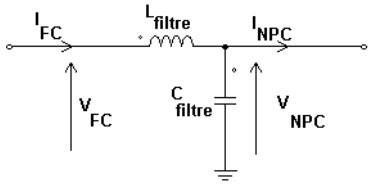


Fig.3. Simplified scheme of the LC filter

The high-frequency component of V_{NPC}, denoted $(V_{NPC})_{HF}$, can be expressed by:

$$(V_{NPC})_{HF} = (I_{NPC})_{HF} \,.\, Z_{C_{filter}} \tag{3}$$

where:

$(I_{NPC})_{HF}$ is the high frequency component at F_{sw_NPC} of current I_{NPC},

and $Z_{C_{filtre}}$ is the C_{filter} impedance, expressed by:

$$Z_{C_{filter}} = \frac{1}{2.\pi.F_{sw\_NPC}.C_{filter}} \tag{4}$$

Consequently, $(V_{NPC})_{HF}$ can be expressed by:

$$(V_{NPC})_{HF} = \frac{(I_{NPC})_{HF}}{2.\pi.F_{sw\_NPC}.C_{filter}} \tag{5}$$

and the maximum admissible ripple of V_{NPC} is then:

$$\delta V_{NPC\_max} = \frac{(I_{NPC})_{HF}}{2.\pi.F_{sw\_NPC}.C_{filter\_min}} \tag{6}$$

where C_{filter_min} is the C_{filter} minimum value corresponding to the maximum ripple of V_{NPC}. The expression for C_{filter_min} is then given by (7):

$$C_{filter\_min} = \frac{(I_{NPC})_{HF}}{2.\pi.F_{sw\_NPC}.\delta V_{NPC\_max}} \tag{7}$$

The FC output current ripple depends on the voltage across L_{filter}, denoted $V_{L_{filter}}$ as expressed by Eq. (8).

$$V_{L_{filter}} = L_{filter}.\frac{dI_{FC}}{dt} \tag{8}$$

Since the amplitude and duration of $V_{L_{filter}}$ ripple are respectively $V_{DC}/2$ and T_d, where T_d is the dead time of the FC leg IGBTs, δI_{FC} can be deduced by (9).

$$\delta I_{FC} = T_d.\frac{V_{DC}}{2.L_{filter}} \tag{9}$$

The minimal value of L_{filter} that enables the I_{FC} ripple to be within its admissible interval is expressed by (10).

$$L_{filter\_min} = T_d.\frac{V_{DC}}{2.\delta I_{FC\_max}} \tag{10}$$

iii) Finally, the inductance and capacitance have to be in a range that guarantees protection against NPC mid-point over-voltages caused by an instantaneous load disconnection or the turning-off of all power devices.

Fig.4 gives a simplified scheme to analyse the V_{NPC} ripple in the case of a brutal load disconnection. L and C do model the LC filter components, E models the V_{FC} voltage, and switch K is used to instantaneously disconnect the load modelled by R. The capacitor voltage V_c, which emulates the neutral point voltage, is constant as long as the load is connected. Once switch K is off, emulating a sudden load disconnection, the system becomes oscillatory and the V_c voltage undergoes an unavoidable over-voltage. This over-voltage depends on the values of L and C. In fact, initially, the system is described by Eq. (11), and when switch K is turned off, it verifies Eqs. (12) and (13).

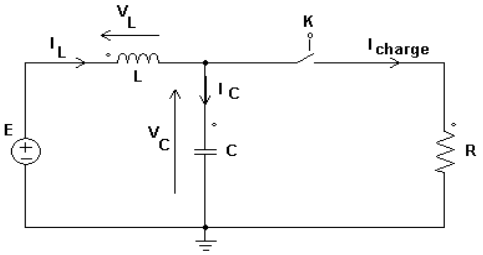


Fig.4. Simplified model of the filter behaviour after an instantaneous load disconnection

$$V_C(t=0) = E, V_L(t=0) = 0, i_L(t=0) = \frac{E}{R} \tag{11}$$

$$V_C(t) = E - V_L(t) \tag{12}$$

$$V_L(t) = L.\frac{di_L}{dt} \tag{13}$$

The current i_L can be written as in Eq. (14):

$$i_L(t) = \frac{E}{R}.\cos(\omega t) \tag{14}$$

where :

$$\omega = \frac{1}{\sqrt{L.C}} \tag{15}$$

Consequently the over-voltage of the capacitor, C, is equal to that of the inductor, L; it is easily derived from (12)–(14) and is given by Eq. (16).

$$\delta V_C = \sqrt{\frac{L}{C}}.\frac{E}{R} \tag{16}$$

Analogously, for the case of instantaneous load disconnection from the proposed hybrid converter, the load current can be approximated by its RMS value and the neutral point voltage, V_{NPC}, would be subject to an over-voltage given by (17).

$$\delta V_{NPC} = \sqrt{\frac{L_{filter}}{C_{filter}}}.I_{load} \tag{17}$$

Imposing a maximum admissible ripple of V_{NPC} in the case of instantaneous load disconnection can be performed if the LC filter components are chosen with respect to Eq. (18).

$$L_{filter\_max} = \frac{(\delta V_{NPC})^2}{(I_{load})^2}.C_{filter} \tag{18}$$

Fig.5, which has a two-dimensional coordinate system, describes the considered LC filter sizing criteria and summarizes graphically the proposed design methodology.

The hatched zone corresponds to the values of L_{filter} and C_{filter} that satisfy Eqs. (1), (2), (7), (10), and (18) and can consequently cope with the three above-mentioned requirements.

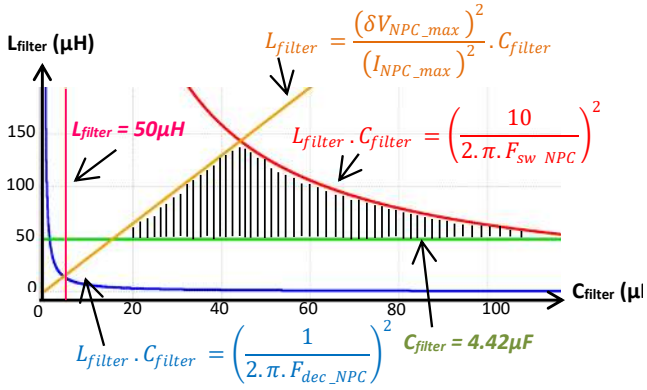


Fig.5. NPC filter sizing methodology: Application for the proposed converter: The hatched zone correspond to values L_{filter} and C_{filter} that meet the three considered criteria @V_{DC} = 600 V, I_{load}= 10 A, F_{sw_NPC} = F_{sw_FC} = 20 kHz , δV_{NPC_max}= 6%, δI_{FC_max} = 6 A, T_d = 1 µs.

It should be mentioned that C_{filter} is "naturally" available in the power converter. It is composed of the already existing decoupling capacitors (taken as equal to 3.3 µF in the experimental setup) in parallel with each half leg of the NPC inverter. This leads to C_{filter}= 19.8 µF. L_{filter} has been chosen as 50 µH regarding the above described methodology.

C. Experimental Validation of the Hybrid Converter Operation under Normal Condition Mode

In order to verify the effectiveness of the proposed filter, it was tested experimentally as shown in Fig.6. The developed power converter uses INFINEON™ F3L150R07W2E3_B11 three-level IGBT modules for the NPC legs and two IXYS™ FII40-06D modules for the commutation cells of the FC leg. Under normal conditions, the proposed FC-NPC power converter was tested with a three-phase RL load and an open-loop FPGA-based control. Under this healthy mode, called (3,3,3) mode, the control board generates three-level PWM signals for the 12 IGBT modules of the three NPC legs. The FC leg, which acts as a DC/DC converter with a constant duty cycle equal to 50%, is controlled to generate an output voltage equal to $V_{DC}/2$. The flying capacitor is actively balanced by using the algorithm proposed in [35].

Fig.7 gives the experimental validation of the proposed converter topology and control, that is, the three-phase NPC converter connected through the LC filter to the FC leg, feeding a three-phase 10-A RL load. The obtained output voltages and currents prove the efficient global operation as shown on Fig.7.a and Fig.7.b. It should be mentioned that the neutral point voltage ripple does not exceed 10% without using any capacitor bank (Fig7.c.). This is achieved thanks to the active neutral point control and the FC filter described above. As expected, the FC leg output current I_{FC} low frequency component (150 Hz) is three times the reference frequency (50 Hz). This low frequency component, which is also observable on the neutral point voltage, is due to non-negligible impedance of the LC filter inductance. The three output voltages, V_{AO}, V_{BO}, and V_{CO}, are quasi-perfectly three-level modulated (0, $+V_{DC}/2$, and $-V_{DC}/2$). The dead time clearly affects the V_{FC} voltage involving $2*F_{sw\_FC}$ frequency glitches. These glitches, which also affect the V_{NPC} voltage, are completely filtered by L_{filter}. As expected, the spectral analysis of I_{NPC} current flowing between the two converter parts given in Fig.7.d shows the two first frequency components at F_{sw_NPC} (20 kHz) and $2*F_{sw\_FC}$ (40 kHz). Moreover, the V_{NPC} voltage ripple and the I_{FC} current one have their values inside the expected ranges.

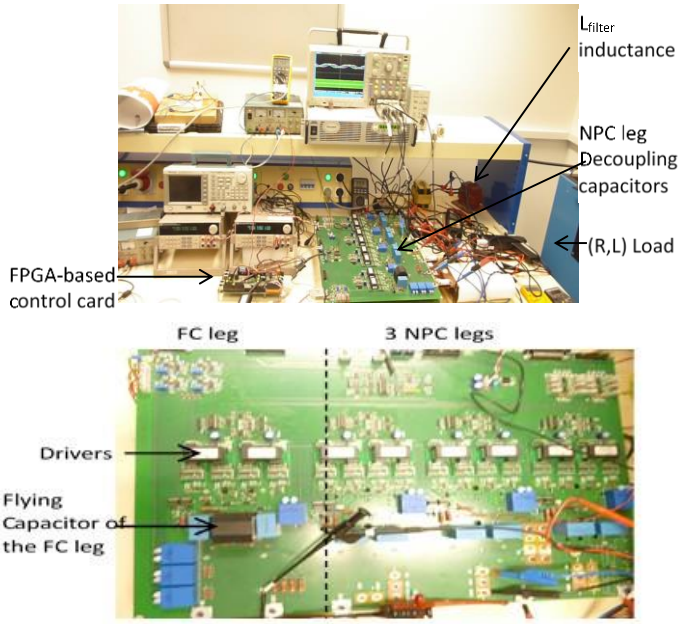


Fig.6. Experimental test bed for LC filter validation: The FC leg is connected to one NPC leg through a 50 µH filter inductance (L_{filter}.)

III. Simple Fault-Tolerant PWM Strategy for the Hybrid FC-NPC Converter

As described in Section II.D, during normal mode, an open-loop FPGA-based three-level PWM strategy is used to control NPC legs. When an NPC IGBT breaks down, the corresponding leg is partially isolated and the phase is

connected to the FC leg output. In this section, a fault-tolerant PWM strategy is described. It consists of developing a PWM reference system for the degraded mode. Fault detection, leg isolation, and post-fault connection are detailed in the next section. It should be noted that in the following, phase *A* refers to the damaged converter leg. Analogous analyses are obviously valid if the failure occurs in phase *B* or phase *C*.

A. Description of the proposed FPGA-based PWM scheme under faulty conditions

During faulty mode, the FC leg continues feeding the active midpoint voltage to the neutral point of the two healthy NPC legs. Thus, phase *A* permanently has just one level "$V_{DC}/2$", while the two other phases have three levels (V_{DC}, $V_{DC}/2$, and 0), as in normal mode operation. This faulty mode is then referred to as (1,3,3) mode. Only phases *B* and *C* are modulated and their power switches have to be controlled. It should be mentioned that, under fault condition (1,3,3) mode, the power converter delivers only eight active voltage vectors and one zero voltage vector and that its maximum modulation depth (M_{max}) is reduced by 50% when compared to normal conditions. Even if this limitation affects the power delivered to the converter load, it avoids system breakdown and corresponds to a transient operation mode before corrective maintenance. The fault tolerant SVM-based strategy described in [35] involves complicated mathematical development and is not compatible with rapid and high-performance FPGA-based controls.

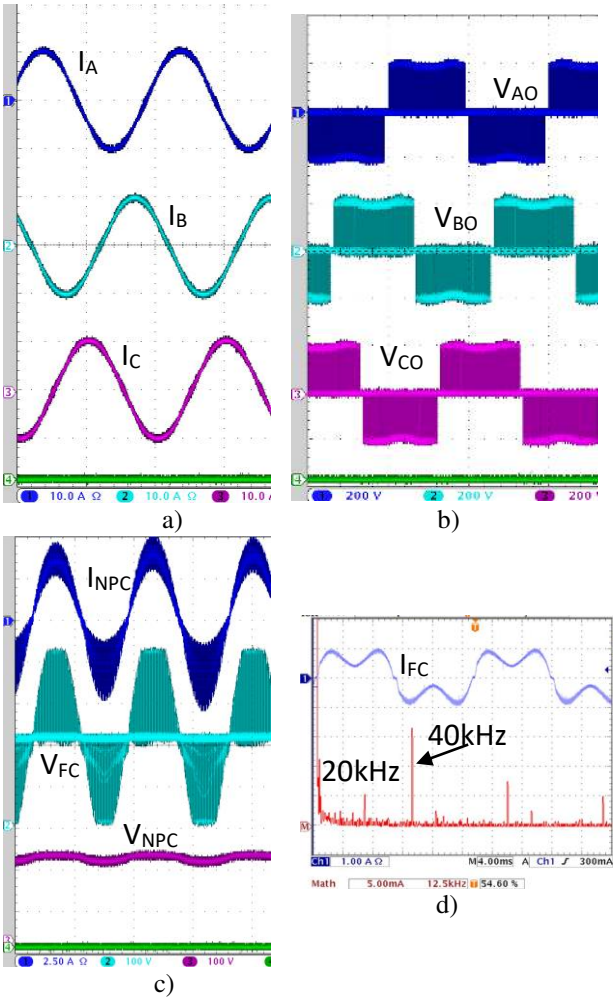


Fig.7. Proposed FC-NPC converter topology and control under normal conditions. Experimental validation @ V_{DC} = *100-V / 10-A* RL load, F_{sw_FC} = *20 kHz*, F_{sw_NPC} = *20 kHz*, dead time T_d = *1 µs*: a) Phase currents I_A, I_B, and I_C *(10 ms/div, 10 A/div)*; b) Output voltages V_{AO}, V_{BO}, and V_{CO} *(10 ms/div, 200 V/div)*; c) NPC input current I_{NPC} *(4 ms/div, 2.5 A/div)*, FC output voltage V_{FC} *(4 ms/div, 100 V/div)*, and NPC neutral point voltage V_{NPC} *(4 ms/div, 100 V/div)*; d) Time *(4ms/div, 1A/div)* and spectral *(12.5 kHz/div, 5 mA/div)* analysis of FC output current I_{FC}

This post-fault reconfiguration implies a modification of the PWM reference system. In fact, in [37], it has been demonstrated that when one of the converter phases is not modulated, shifting the two remaining ones by 30° as depicted in Fig.8.a leads to a system that is able to operate in a balanced way regarding the phase-to-phase voltages.

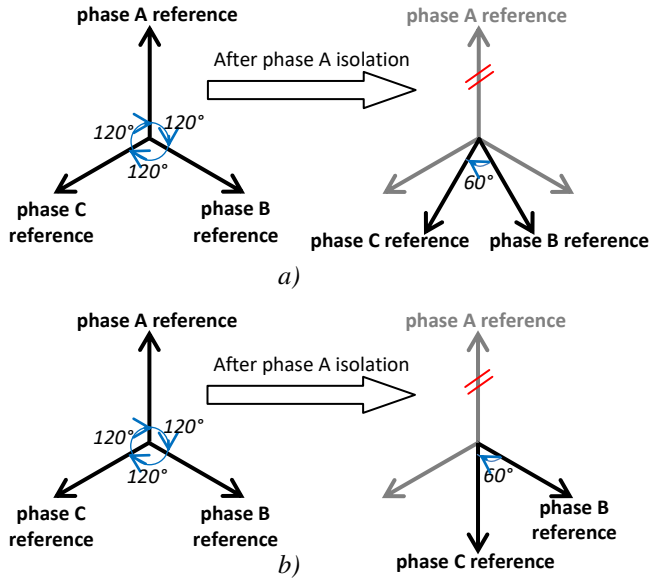


Fig.8. Voltage reference system modification after the loss of phase *A* leg: a) Classical modification [37]; b) Proposed modification

In this paper, this solution is improved. In order to simplify the control reconfiguration from the normal mode to the faulty one, the PWM reference system presented in Fig.8.b is proposed. With this technique, the phase *B* reference is not changed during faulty mode, and the phase *C* reference can be easily deduced from the phase *A* one. In fact, after the occurrence of a fault, the phase *C* reference is the opposite of the phase *A* one during normal mode.

B. Experimental Results

Validation tests of the proposed control reconfiguration were carried out on the experimental test bench described above. Fig.9 gives some of the experimental results obtained with various DC bus voltage and RL-load current configurations. Under normal conditions, the three NPC converter phases deliver three-level voltage outputs. When a fault occurs, the power converter reconfiguration ensures the connection of the faulty leg (taken as phase *A* under the current tests) output to the NPC neutral point and the V_{AO} voltage is then null (Fig.9.a). During faulty mode, and according to the proposed reconfiguration scheme described in the previous paragraph, the V_{CO} voltage is equal to the opposite of the V_{AO} one if the fault wouldn't have occurred; as illustrated in Fig.9.a. The V_{BO} and V_{CO} voltages continue to be three-level modulated after the occurrence of the fault (Fig. 9.b): They are shifted by *60°*, enabling the load currents to form a balanced three-phase system with a *50%* amplitude reduction: Fig. 9.c emulates the converter recovery since the power system switches from the (1,3,3) mode to normal mode operation.

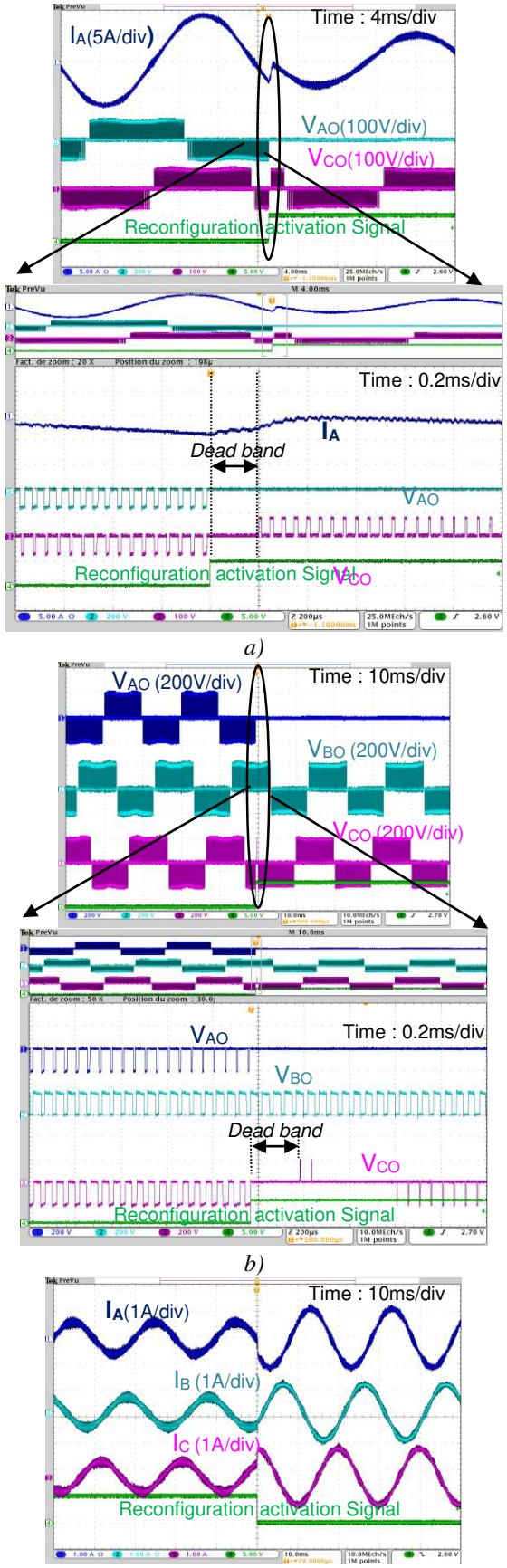


Fig.9. Fault-tolerant hybrid FC-NPC converter and control validation: Transition between normal condition mode and (1,3,3) post-fault mode with a security dead-band and a *50%* reduction in output current @ *20 kHz* switching frequency, and *1 µs* dead time: a) phase A current, I_A and Output voltages V_{AO}, V_{CO}; b) Output voltages V_{AO}, V_{BO} *and* V_{CO}; c) Load currents I_A, I_B, and I_C

It is to be noted that for safe transition from normal mode to faulty mode, a 200us dead band is introduced between these two modes: During this dead band, phase C control signal is OFF and its output voltage is then null. The magnified Fig. 9.a and Fig.9.b prove that the transition from normal condition mode to post-fault mode does not involve any transient or undesirable system interruption.

IV. Novel Fault Isolation and Post- Fault Reconfiguration Techniques for the Hybrid FC-NPC Converter

In order to reach fault tolerant capabilities, three steps are mandatory for the considered FC-NPC converter: first, the converter has to detect the fault that would affect the power switch, second, isolate it, and third, enable the reconfiguration of the post-fault topology. In the following, an interesting technique combining both isolation and post-fault reconfiguration is proposed.

A. Fault Detection

NPC IGBT faults lead to discordance between the control signal delivered by the PWM module and the corresponding leg output voltage. The developed fault-detection principle is to compare an adaptation of the control signals with the voltages across the converter IGBTs. Under normal conditions, they comply; otherwise, the fault detection module indicates an error.Fig.10 shows the adopted fault detection for the 3L-NPC converter. The output *Vopt1* of optocoupler *Opt. 1* is:

- "ON" if the converter output *Voutput1* is equal to $V_{DC}/2$,
- "OFF" otherwise.

The output *Vopt2* of opto-coupler *Opt. 2* is:

- "ON" if *Voutput1* is equal to $-V_{DC}/2$,
- "OFF" otherwise.

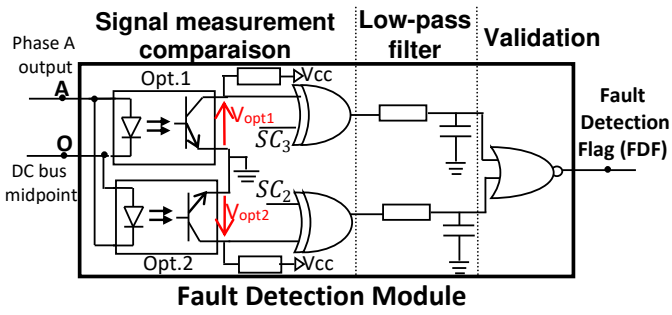


Fig.10. Fault detection module. Under normal conditions, the "fault detection flag" is ON. It turns to OFF when a fault occurs on one of the four power switches T_1,...,T_4

It should be mentioned that the two RC-based low-pass filters aim to filter the output comparison signal and avoid inadvertent activation caused by an imperfect compensation of the dead time and driver's propagation delays. Typically, the optimal compensation of the delays is tuned at the nominal operation. To validate the fault detection step, experimental tests on one NPC converter leg were carried out. An FPGA-based control board delivers the power switch control signals. The NPC leg is connected to a *100-V* DC bus and the neutral point "*0*" is passively balanced. The fault is created through an external push button that inhibits the four control signals of phase by means of a blocking signal, named BLS. An open-circuit fault is then emulated. Fig.11 gives the

power switch blocking signal BLS, the IGBT T_1 output voltage ($V_{CE}(T_1)$), and the fault detection flag (FDF) after the occurrence of a fault.

The power switch fault is effectively detected only *33 µs* after it begins to occur, which is less than the switching period of the NPC part . This delay is due to the two RC-based low-pass filters and has to be taken into account in order to propose adapted fault isolation and power converter reconfiguration procedures.

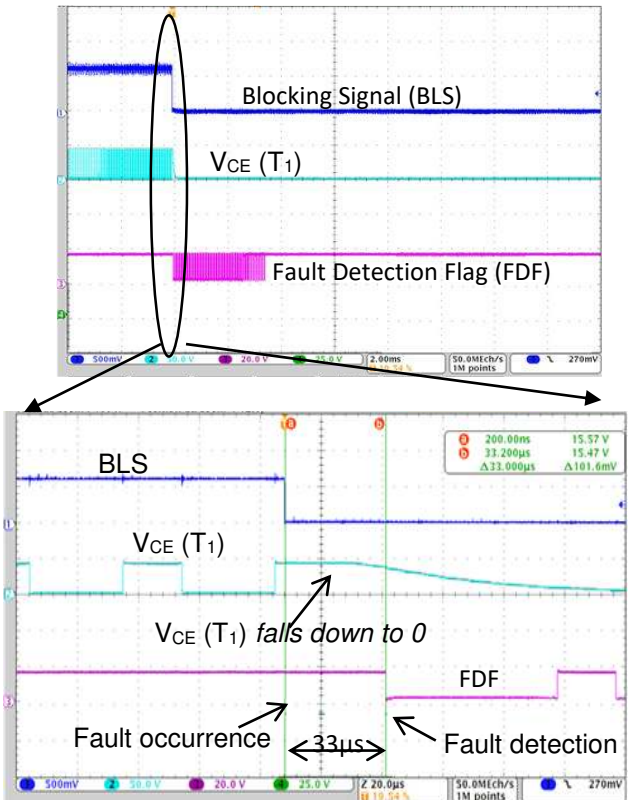


Fig.11. Power switch fault detection: a) Blocking Signal *BLS (0,5V/div)*, IGBT T_1 output voltage $V_{CE}(T_1)$ *(50V/div)*, and Fault Detection Flag, *FDF (20V/div)*, Time : *2ms/div;* b) zoom: *20µs/div*

B. Fault Isolation and Power Converter Reconfiguration

In [38], the authors proposed an interesting fault isolation and hardware reconfiguration technique for two-level converters and [35] adopted it for multilevel applications. Since it requires the addition of only one power switch (thyristor) and two fast fuses per phase, its principle is now integrated in the studied power converter topology. The proposed symmetrical isolation technique consists of "high-side" and "low-side" fuse-blowing through the DC bus short circuit using thyristor Th_x in series with snubber inductance Ls_x. The post-fault connection between the damaged phase and the active neutral point is also ensured by this thyristor, and no additional semiconductors are necessary for this connection; as depicted. In fact, phase current flows from the load to the FC leg output (or vice versa) through the parallel diodes of the fault leg IGBT modules and the thyristor Th_x as shown in Fig.12. In this figure, the fault-tolerant three-level hybrid power converter reconfiguration after the occurrence of a fault on the phase *A* leg is presented. This new technique has two main advantages. First, isolation and post-fault reconfiguration are ensured by the same additional component, that is, the thyristor Th_x. Second, this technique is applicable regardless of the faulty IGBT and the fault type (open circuit or short circuit). Parallel diodes are connected within the transistor chips.

The power converter reconfiguration needs a fast fuse reaction during pre-arc phase (low I^2Tp value), low *di/dt* value during post-arc phase, a low leakage current and short operation time in order to prevent converter power switch damage and to ensure acceptable post-blowing isolation performance. Many experimental tests are carried out in order to indicate the recommended fuse technology and PCB compatible technology for the considered application.Fig.13 shows the system topology used for the isolation

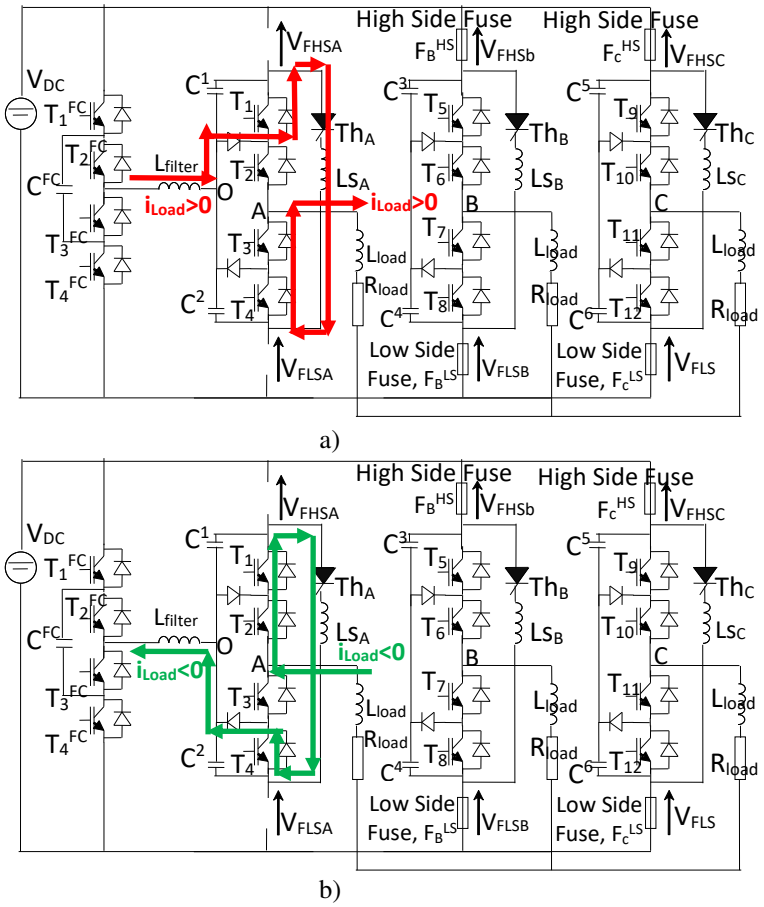


Fig.12. Hybrid FC-NPC converter: power switch fault-tolerance capability thanks to a simple reconfiguration control and an effective addition of three thyristors (Th_a,Th_b,and Th_c) and six fast fuses ($F_X{}^{HS}$ and $F_X{}^{LS}$, where $X = A$, B, and C). *a)Case of positive load current b) Case of negative load current*

technique test. The two fuse technologies presented in Fig.15 are tested: Surface Mounted Devices (SMD, *125 V / 10 A*, *2 × 2 matrix*) and a classical cartridge one (*250 V / 32 A*) screwed on the bus bar power PCB. Three parameters are considered to compare the two fuse types:

- the time needed by the thyristor current, I_{TH}, to reach the value that blows up the High Side and Low side fuses;
- the time needed by I_{TH} to fall down to zero after fuses blowing up. In fact, in the considered fault-tolerant power converter application, the discharge time of the snubber inductance is an important issue: the converter reconfiguration step cannot begin before the post-arc phase ends definitively. The choice of isolation fuse influences the waiting time that the converter control board has to have between normal and fault operation modes.

- and voltages across the two fuses V_{FHS} and V_{FLS}. In fact, once the fault leg is isolated, it is important to consider the voltages across the high- and low-side fuses. Theoretically, these two voltages are balanced and equal to $V_{DC}/2$. Otherwise, the converter output voltage *Voutput* would be floating and would lead to additional and undesirable load current components caused by the fuse leakage current.

Fig.16 shows the experimental results during the fault leg isolation. As expected, the first phase during the fault isolation operation corresponds to the snubber inductance charging with I_{TH} current. Once the fuse I^2T_p rating value is reached, the fuses blow and the *Ls* current discharges through the power switch freewheeling diodes: this is the second phase of the isolation process. During this phase, after the post-arc phenomena, fuses become high impedance, allowing isolation of the fault leg.

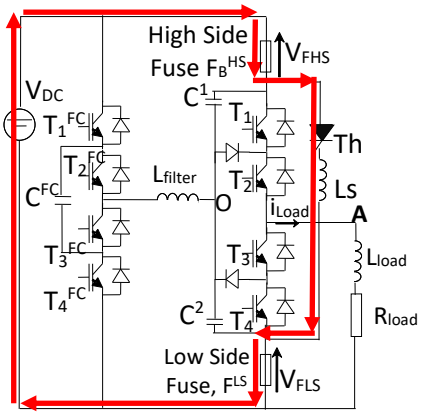
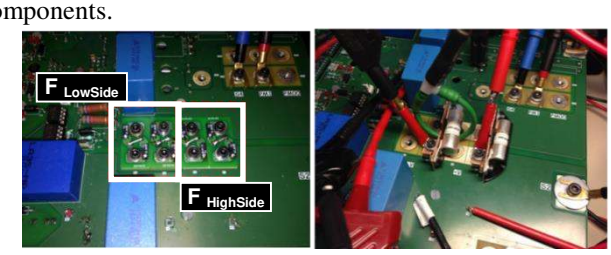


Fig.13. Fault isolation technique test setup: Two fuses (F_{HS} and F_{LS}), one thyristor (*Th*), and a snubber inductance *Ls* are added to the original 3L-NPC leg

Fig.14. .

As shown in Fig.16, the two fuse types have approximately the same speed: For the cartridge type, the current I_{TH} reaches *2500A* after *25* μs and for the SMD one, the current I_{TH} reaches *1800A* after *20* μs. The two fuse types have approximately the same performances considering this first criteria. However, the post-arc phase requires *60%* more time when using the cartridge fuses (*80* μs) compared to the SMD ones (*50* μs). Then, the second fuse technology leads a lower overvoltage at the DC bus than the first one, and it clearly provides a better safe isolation process regarding all parallel components.



a) *b)*

Fig.15. Fuses used for experimental tests: a) SMD fuses: Schurter 125 V / 10 A; b) Cartridge fuses: Mersen BS88 32 A / 250 V

Moreover, Fig.16.a shows that with the cartridge fuses, the unbalance between the voltages at the "high-side" and "low-side" fuses reaches *250 V* (V_{HFS_max}=*250V and* V_{FLS_min}=*0V)*, that is, *150%*, whereas it does not exceed *150V* with SMD technology, as shown in Fig.16.b.

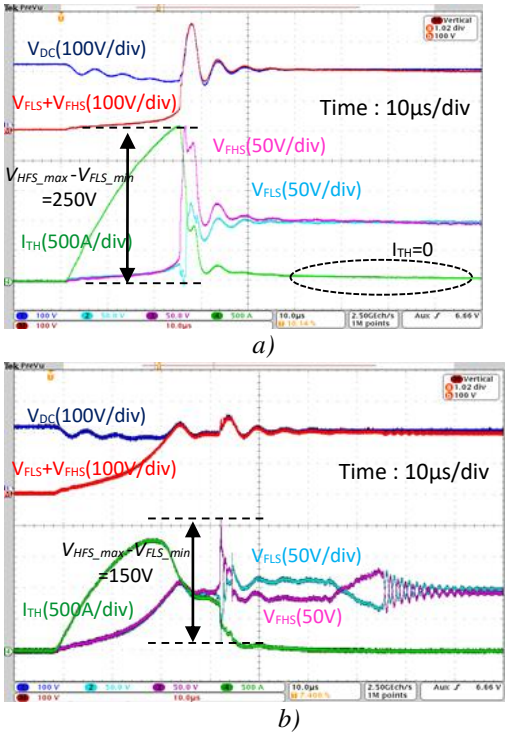


Fig.16. Comparison of the behaviour of two fuses of different technologies during power converter fault leg isolation, V_{DC} = *200 V*: a) Classical cartridge; b) surface mounted devices: high- and low-side fuse voltages V_{FHS} *(50 V/div)*,V_{FLS} *(50 V/div)*, fuse current I_{TH} *(500 A/div)*

The above described isolation technique tests led to the conclusion that the SMD fuses are, today, the most suitable ones for the fault-tolerant power converter studied. It should be mentioned that, during the arc phase, a very low energy is generated, which corresponds only to the energy stored in the "DC bus-NPC leg" mesh and does not involve the energy stored in the load phase that spontaneously flows through the clamp diodes and the FC leg.. Moreover, the energy stored in the snubber inductance is not considered because this inductance is freewheeling. All these properties are important because fuses that have low break energy (and consequently low cost and volume) are able to meet the considered application requirements. However, these fuses must have undergone very low manufacturing dispersion in order to have quasi-similar behaviour during the fault isolation process. Consequently, this effective fault isolation solution does not entail a significant converter efficiency, price and volume increase.

C. Experimental Validation

In this paragraph, the whole of the fault-tolerance process, including fault creation, fault detection, leg isolation, and control reconfiguration, is experimentally validated. The fault is created using an external switch, which produces an open circuit of one of the NPC power switches.

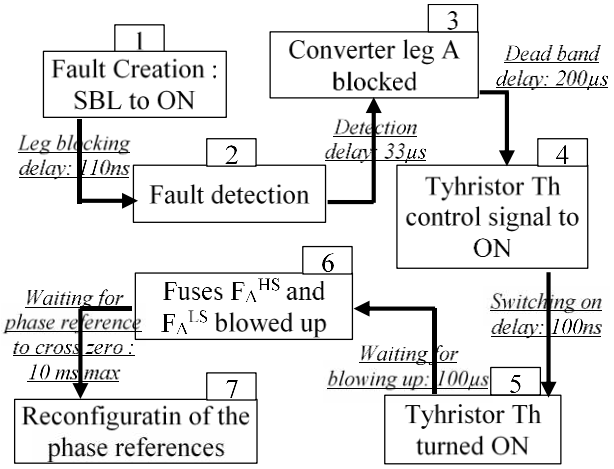
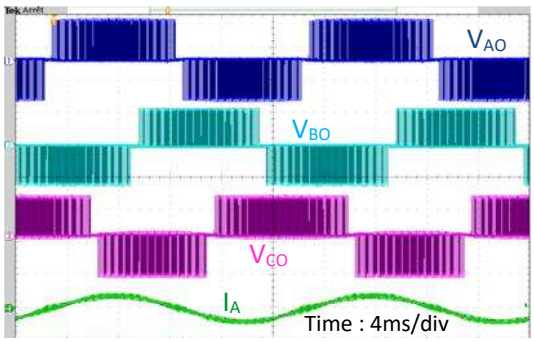
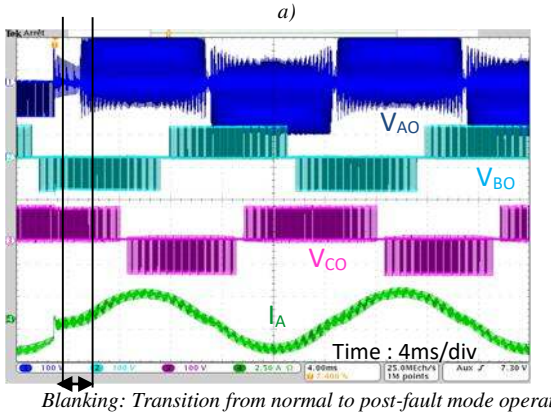


Fig.17. Fault-tolerance process

For safe transition from normal mode to faulty mode, two actions are taken. First, a dead band is considered after fault detection and before thyristor activation. Second, control reconfiguration is done when the phase *A* reference is equal to zero, in order to avoid the risk of over-current. Fig.17 shows all the delays included in the fault-tolerance process.In this test, the focus is given to the transition from normal to faulty operation. In order to dissociate the numerous issues of the designed hybrid converter (neutral point regulation, filter behaviour, post-fault operation, hardware reconfiguration), the midpoint of the NPC legs is connected to a capacitive neutral point voltage composed of two electrolytic capacitors. During faulty mode, the FC leg replaces the faulty NPC one. Fig.18 demonstrates the effectiveness of the proposed fault-tolerance process.

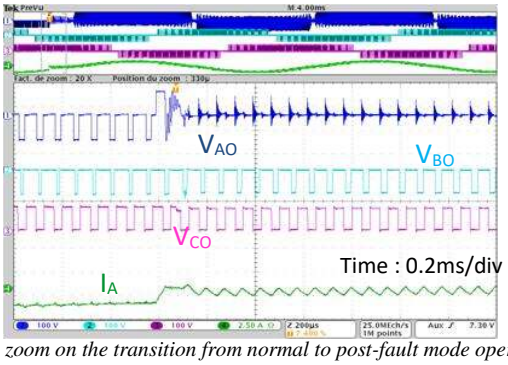


a)



Blanking: Transition from normal to post-fault mode operation

b)



c) zoom on the transition from normal to post-fault mode operation

Fig.18. Experimental validation of the fault-tolerance process: NPC leg output voltages V_{AO}, V_{BO}, and V_{CO} (100V/div) and NPC leg A output current I_A (2.5A/div). a) normal mode operation, b) post-fault mode operation, c) zoom on the transition from normal to post-fault mode operation

Indeed, the availability of the converter after an NPC IGBT breakdown is ensured. In this test, the open-circuit failure occurs when the phase *A* reference is close to zero, which results in reduced blanking time (2 ms) before the FC leg starts to modulate. During this blanking time, phase *A* is isolated from the DC bus, connected to the inactive FC leg and its load current is cancelled, while phases *B* and *C* remain active with a 120° phase shift. Voltages V_{BO} and V_{CO} do not undergo any degradation during faulty mode. However, due to the resonance between the flying capacitor C^{FC} and filter inductance L_{filter} (already mounted on the test bench), the mid-level of voltage V_{AO} is not perfectly null. Phase current I_A is still perfectly sinusoidal in faulty mode with the same amplitude. Fig.19 shows the fuses' voltage and snubber current during the isolation process. The triggering of the thyristor causes the charge of $L_{snubber}$ inductance, resulting in a strong current surge with a peak at 1800 A: it is the first isolation phase. When i²t is reached, the fuses blow up and the snubber current flows in the freewheeling diode until it is cancelled. The voltage across each fuse increases gradually, because of the plasma fluctuation and then fuse's internal resistance. This internal resistance is first constant and then suddenly increases during the arc phase. The DC voltage is divided between the two fuses: It confirms the effectiveness of the leg isolation.

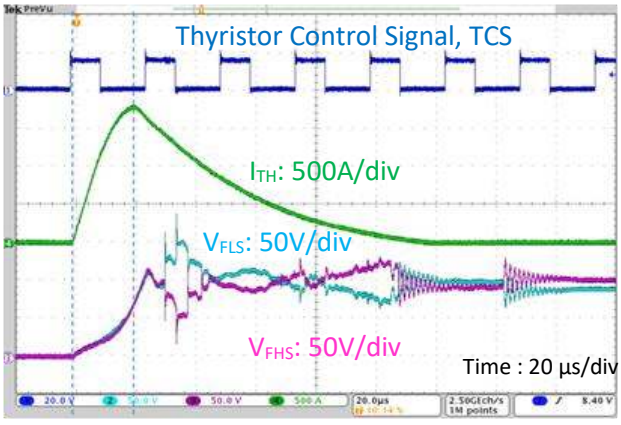


Fig.19. Experimental validation of the fault-tolerance process: Thyristor control signal, $L_{snubber}$ current I_{TH}(500A/div), fuse voltages V_{FHS} (50V/div) and V_{FLS} (50V/div)

V. Conclusion

This paper investigates a three-level fault-tolerant hybrid converter that hat combines two main topologies: three identical three-level NPC-based legs and a three-level FC-based one. The aim of this FC leg is to provide an actively balanced neutral point to the NPC ones and to replace the conventional high-capacitance electrochemical capacitors by simple polypropylene ones.

Connection of the FC leg to the three NPC ones needs an LC filter design to ensure decoupling of the mandatory two topologies. The precise filter sizing is described in detail. It takes into account three criteria: spectral constraints, admissible neutral point voltage and current ripples, and protection against NPC neutral point overvoltage in the case of instantaneous load disconnection.

Under fault conditions, a post-fault mode named (1,3,3) is analysed: the damaged leg is disconnected and the corresponding phase is connected to the active midpoint generated by the FC leg. Converter availability is ensured, but with an output power penalty of *50%*. A simple FPGA-based reconfiguration control for post-fault (1,3,3) mode was proposed and experimentally validated.In order to tolerate power switch faults, in both open- and short-circuit modes, the authors enhanced the hybrid FC-NPC topology by adding the required fault-tolerance features needed to detect the switch fault, isolate the corresponding damaged leg, reconfigure the converter, and ensure its safe post-fault operation. For each of the three NPC legs, dual-fuses and one thyristor are added to isolate the switch fault. This thyristor also ensures an original reconfiguration of the hybrid converter after the occurrence of the fault. Two fuse technologies were tested and their performances were shown, proving that the SMD one is currently more suitable for fault-tolerant converter applications.

This paper is a novel research investigation in the field of fault-tolerant multilevel converters since all the needed fault-tolerance functionalities were simultaneously tested and validated. The experimental results were carried out with a 15 kW converter test-bench that the authors designed according to the abovementioned considerations. The proposed functionalities imply increases in converter cost and volume, but they remain relatively low. Indeed, the designed converter has attractive solutions considering the fault-tolerance improvement it offers. The developed test-bench could be used as an original experimental benchmark to evaluate the whole of the fault-tolerance process and to verify the effectiveness of the dependable capabilities of the power system when a switch failure occurs.

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