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Vertical Nanowire Gate-All-Around *p*-type Tunneling Field-Effect Transistor With $Si_{0.8}Ge_{0.2}$/Si Heterojunction

Arvind Soundarapandian [1, 2], Ramanathan Gandhi [1, 2], Zhixian Chen [1], Xiang Li [1], Navab Singh [1] and Sungjoo Lee [2]

[1] Institute of Microelectronics, A*STAR (Agency for Science, Technology and Research), Singapore
[2] Department of Electrical and Computer Engineering, National University of Singapore, Singapore

Abstract. We present a CMOS compatible *p*-type gate-all-around (GAA) vertical silicon nanowire tunneling field effect transistor (TFET) featuring $Si_{0.8}Ge_{0.2}$ source with silicon channel. Besides heterojunction on source side, the highly abrupt doping profile at source-to-channel junction is achieved by low temperature dopant segregation. The fabricated devices display subthreshold slope (SS) as low as 30mV/dec over one decade of drain current, which remains below 60 mV/dec over 3 decades. In addition, our TFET showed reasonable I_{on}/I_{off} ratio of (10^4) and low drain induced barrier lowering (DIBL) of 40 mV/V.

Keywords: Tunnel Field Effect Transistor (TFET), Subthreshold Slope (SS), Dopant Segregation.

1. Introduction

Scaling of MOSFET to improve device performance and increase device density faces enormous challenges due to excessive increase in passive power. Subthreshold leakage (OFF state) current is the major leakage contributor in nanoscale MOSFET devices and is also highly temperature dependent. It increases with device scaling owing to non-scalability of subthreshold slope (SS) and continuous reduction in the supply voltage (V_{dd}), which requires reduction of the threshold voltage (V_{th}) to maintain essential device performance. The $SS=[d(\log I_d)/dV_g]^{-1}$ of MOSFETs is governed by thermal diffusion of carriers over a potential barrier and has theoretical lower limit of 60 mV/decade at room temperature. To overcome this issue, alternative transistor designs are needed for energy efficient devices. One such device is the Tunneling Field-Effect Transistor (TFET) [1-9]. Although there are few novel devices such as carbon nanotube based FETs [10], impact ionization MOSFETs [11-13] and NEMS based FETs [14-15] which show potential sub-60 mV/dec operation, TFET has the advantage of CMOS process compatibility and possesses extremely low OFF state current. Other devices have the disadvantage in terms of its fabrication process and high voltage requirements for its operation as well as reliability concern [1].

The TFET structure consists of gated *p*+/*i*/*n*+ structure as shown in Fig. 1. The carrier injection happens via band to band tunneling (BTBT) at the reverse biased source channel junction. Unlike MOSFET, which utilizes thermionic injection-carrier diffusion, TFET uses tunneling as the carrier injection mechanism. Therefore, it is possible for TFETs to achieve low OFF state current as well as SS below the ideal limit of 60 mV/decade of MOSFET at room temperature.

However, the ON state current of a Si TFET is several magnitudes lower than that of conventional Si MOSFETs due to the fact that Si has relatively larger bandgap and effective tunneling mass [1]. Therefore, devices with novel geometry and different source material are necessary to substantially increase the device drive current. One such technique is to introduce lower bandgap material such as SiGe at source to enhance the tunneling current [7]. Such a technique, which is easy to integrate in vertical format, when coupled with vertical gate-all-around GAA nanowire structure gives excellent results due to better electrostatic control of

channel by the gate compared to planar device [16]. Moreover, the vertical nanowire provides high density of integration which leads to more number of devices per unit area [17].

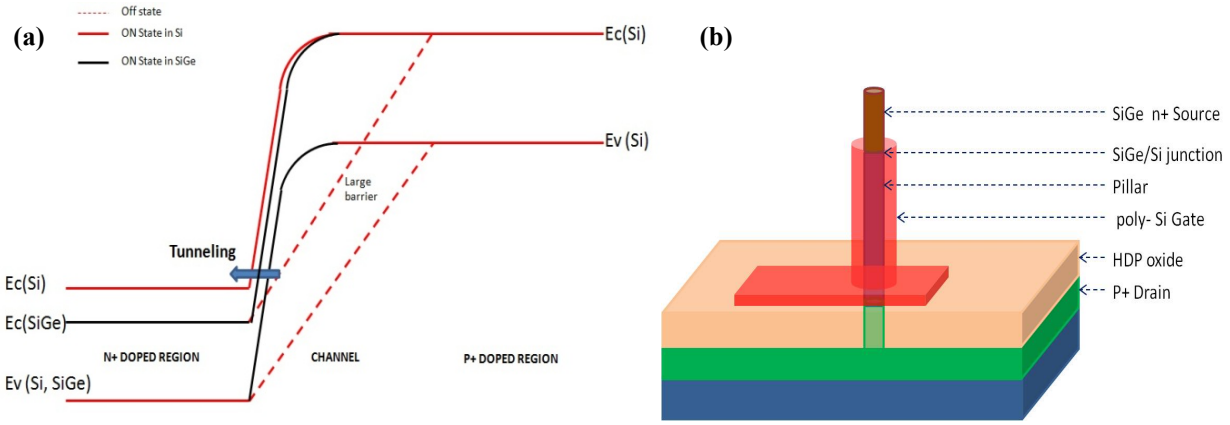

Fig. 1: (a) Band diagram showing the mechanism of tunneling that happens in TFETs with gated *p*+/*i*/*n*+ structure. (b) 3D schematic of the heterojunction vertical nanowire GAA TFET.

In this paper, we demonstrate *p*-TFET fabricated on GAA vertical nanowire platform integrated with SiGe source coupled with a novel dopant segregated silicidation technique to achieve steep source dopant profile that leads to reduction of SS. Our device has a reduced ambipolar behaviour due to independently tuned source/drain profiles (sharp on source side and graded on drain side) with SS as low as 30 mV/decade, with $I_{on}/I_{off} \sim 10^4$ and drain induced barrier lowering (DIBL) of 40 mV/V.

2. Device Fabrication

The methodology used here to fabricate GAA SiGe source nanowire TFET is a top down approach [5-6] as shown in Fig. 2. The scanning electron micrographs for the device process flow are shown in Fig. 3. We started off with an 8-inch Si substrate and performed RCA pre-clean before 50 nm $Si_{0.8}Ge_{0.2}$ was grown epitaxially in ultrahigh vacuum [Fig. 2(a)]. Thereafter, Si_3N_4 hard mask was deposited and lithographically patterned using 248 nm KrF laser source [Fig. 2(b)]. Nanowires with height of 300 nm and diameter ~ 70nm were formed via anisotropic etching, and followed by sacrificial oxidation and removal of grown oxide in diluted hydrofluoric acid (DHF) as shown in Fig. 2(c) and Fig. 3(a). The process of resist trimming and sacrificial oxidation are the key to achieve such a small diameter wire. In order to define the drain region BF_2 implantation ($10^{15}cm^{-2}$/10keV/0°tilt) and activation (1000°C/10s) was performed [Fig. 2(d)]. SiO_2 was then deposited non-conformally using high density plasma process and partial etched back using DHF to obtain 70 nm isolation oxide. After that, gate oxide of 4.5 nm was thermally grown followed by 50 nm amorphous-Si gate material deposition using low pressure chemical vapour deposition [Fig. 2(e)].

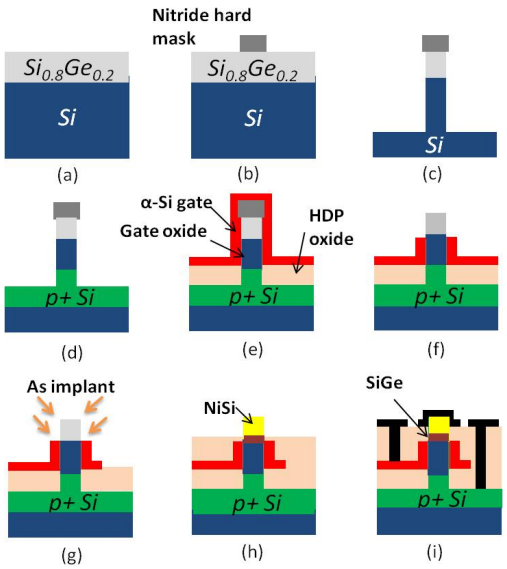

Fig. 2: Device Process flow.

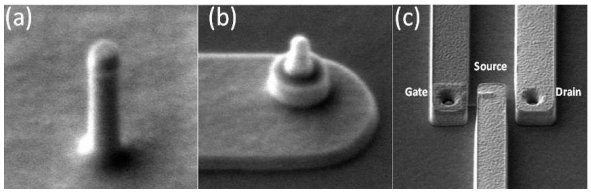

Fig. 3: Scanning electron micrographs of the fabricated device with a nanowire diameter of ~70 nm.

Gate material was implanted vertically by using phosphorus ($10^{15}cm^{-2}$/10keV) and activated at 1000ºC for 5s. Then, a sacrificial oxide layer defining the gate length is formed similar to isolation oxide and followed by isotropic etch of gate material to expose the top of the nanowire [Fig. 2(f) and Fig 3(b)]. The sacrificial oxide layer was then removed in DHF. The gate edge was aligned with the SiGe/Si heterojunction based on height measurements. After gate patterning, implantation of arsenic ($10^{15}cm^{-2}$/5keV) was done from four directions - 90° apart at a tilt angle of 60° to form the *n*+ source region [Fig. 2(g)]. In order to protect the gate from being shorted to source from the forthcoming silicidation step, another isolation HDP oxide was deposited and etched back to just expose the source for silicidation process [Fig. 2(h)].

Silicidation process includes deposition of Ni (15 nm) by sputtering, followed by a two-step rapid thermal annealing (RTA) at 220ºC/30s and 440ºC/30s in N_2 ambient. Unreacted Ni was selectively removed after first RTA in H_2SO_4:H_2O_2:H_2O solution. Silicidation was done to segregate arsenic dopants at the silicide-SiGe interface which is also source-to-channel junction [5-6]. Finally, Al metallization was done followed by sintering at 420ºC for 30min [Fig. 2(i) and Fig 3(c)].

3. Results and Discussion

The characterisation of SiGe *p*-TFETs was done using the HP4156A parameter analyzer. The I_d-V_g and I_d-V_d characteristics for the device with nanowire diameter of 70 nm and gate length of 150 nm are shown in Fig. 3. The SS was found to be ~30 mV/dec for a decade (10^{-14} - 10^{-13} A) and <60 mV/dec for a little over 3 decades of drain current (10^{-14} - 10^{-11} A). The SS increase with drain current can be clearly seen in Fig. 4(a). I_{on}/I_{off} ratio of 10^4 and DIBL of 40 mV/V is achieved in our work showing the excellent gate control of the GAA device.

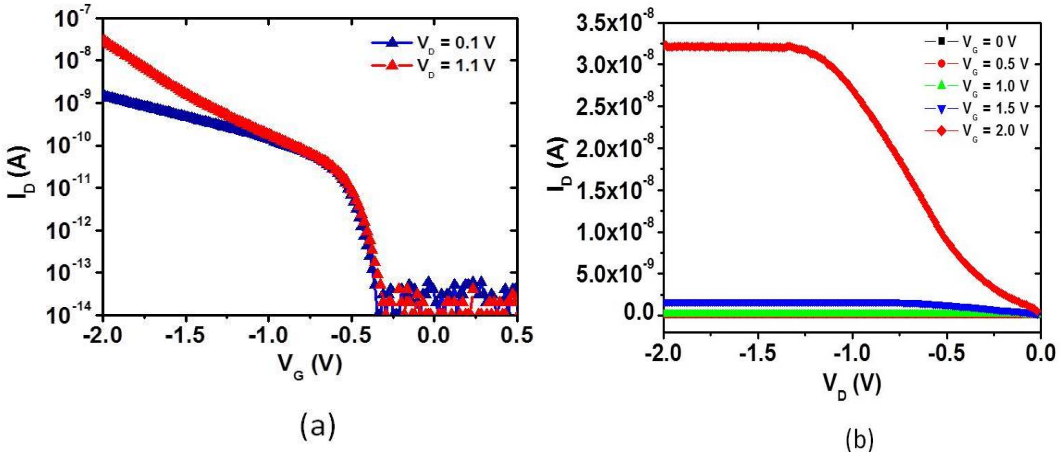

Fig. 3: (a) I_d–V_g characteristic of a heterostructure SiGe source nanowire p-TFET device with low SS values of 30 and 60 mV/decade over a decade of drain current (10^{-14} – 10^{-13} A) and over 3 decades of drain current (10^{-14} – 10^{-10} A), respectively, and (b) corresponding I_d–V_d.

Heterojunction based TFETs which utilizes lower bandgap material at source side such as SiGe should provide higher ON current due to the fact that tunneling current exponentially depends on tunnelling barrier. However, in our work, enhancement of ON current is not as expected, which might be due to poorly formed Si-SiGe interface, where high amount of interface traps lead to decrease in tunneling current. In order to improve Si-SiGe interface properties, a much better epitaxial process such as molecular beam epitaxy (MBE) [18] is recommended. MBE has an excellent atomic level deposition capability with controllable deposition rate which could reduce the number of traps formed in Si-SiGe interface. Thus, with better Si-SiGe interface,

enhancement of ON current is possible. There is also a possibility of marginal misalignment between SiGe layer and the edge of gate which in-turn could hamper the gate controllability on tunnelling junction, leading to low ON current.

It should be noted that our TFET device exhibits suppressed ambipolar behaviour in comparison to other experimental based TFETs in literature [8-9]. The doping gradient in source junction is more abrupt due to the source side being enhanced by dopant segregation method [19]. Because of large thermal budget applied after vertical implant, the doping density in drain channel junction at the bottom of the nanowire is graded. Hence, we observe a much wider depletion region at the bottom of the tunnelling which in turn leads to reduction in ambipolar behaviour. On the whole, the ambipolar effect is suppressed due to the natural asymmetry of the vertical design which led to manipulation of source and drain doping levels independently. In addition, our asymmetric TFET design which has low bandgap SiGe (small tunnel barrier) only at source also adds to suppression of ambipolar behaviour.

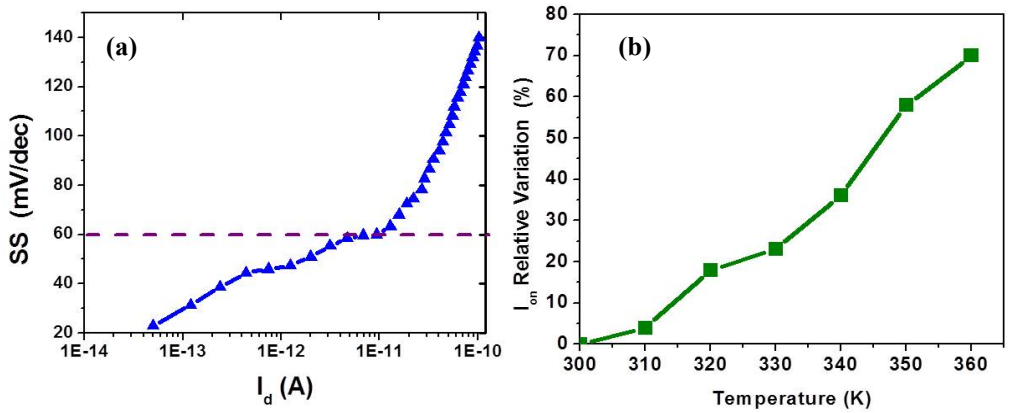

Fig. 4: (a) SS vs. I_d plot showing the typical TFET behaviour with sub 30 mV/decade for 1 decade and sub 60 mV/decade SS for three decades of drain current (10^{-14}–10^{-11} A). (b) I_{on} versus temperature showing the effect of increasing the temperature beyond room temperature.

Fig. 4(b) shows the effect of temperature with ON current of the device. Unlike MOSFETs where the ON current decreases when temperature increases, TFETs show a reverse phenomenon where the ON current increases as temperature increases due to temperature induced bandgap reduction. The expression for bandgap, E_g is given by

$$E_g = E_g(0) - \frac{\alpha T}{T + \beta}$$

Where $E_g(0)$, α and β are material constants. In turn, the bandgap dependence of the tunneling current can be quantitatively described using Kane's BTBT model [4, 13] as follows:

$$I_d \propto A\xi^2 E_g^{-\frac{1}{2}} exp\left(-B\frac{E_g^{\frac{3}{2}}}{\xi}\right)$$

Where ξ is the electric field and A, B are functions of carrier effective mass and the tunnelling barrier. So The reduction in E_g from the increase in temperature results in higher current. On the other hand, for MOSFETs, the drive current decreases as temperature increases due to carrier mobility reduction mainly because of the reduction of carrier scattering caused by thermal vibrations of the semiconductor crystal lattice [20].

4. Conclusion

In summary, we have demonstrated SiGe/Si heterojunction *p*-type TFET devices based on vertical nanowire GAA with SS as low as ~ 30 mV/decade for a decade and sub-60 mV/decade for 3 decades of drain current. This work projects TFETs as a promising successor of MOSFETs and for future energy-efficient green electronics. High quality Si-SiGe tunnel interface at source along with high-k gate dielectric material are expected to further enhance device ON current.

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