Review Article

Vertical Silicon Nanowire Platform for Low Power Electronics and Clean Energy Applications

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This paper reviews the progress of the vertical top-down nanowire technology platform developed to explore novel device architectures and integration schemes for green electronics and clean energy applications. Under electronics domain, besides having ultimate scaling potential, the vertical wire offers (1) CMOS circuits with much smaller foot print as compared to planar transistor at the same technology node, (2) a natural platform for tunneling FETs, and (3) a route to fabricate stacked nonvolatile memory cells. Under clean energy harvesting area, vertical wires could provide (1) cost reduction in photovoltaic energy conversion through enhanced light trapping and (2) a fully CMOS compatible thermoelectric engine converting waste-heat into electricity. In addition to progress review, we discuss the challenges and future prospects with vertical nanowires platform.

1. Introduction

Since late 1990s, the nanowire has become a buzz word in nanoscience and nanotechnology domain with many promises, demonstrations and surprises in the technologically important and application-rich areas. For example, nanowire devices, especially in Gate-All-Around (GAA) architecture, have emerged as the front-runner for pushing Complementary Metal-Oxide-Semiconductor (CMOS) scaling beyond the roadmap. These devices offer unique advantages over their planar counterparts and other contenders, which make them feasible as an option for 15 nm and beyond technology nodes with sub-10 nm channel length devices already demonstrated through simulations [1] and experiments [2]. Indeed, the cylindrical geometry gives inverse logarithmic dependence of the gate capacitance on the channel diameter, and thus the gate length in these devices can be scaled with wire diameter without reducing the gate dielectric thickness aggressively. With the same principle, it also makes the GAA nanowire architecture an excellent candidate for Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) type nonvolatile memory applications where the gate dielectric has to

be necessarily thicker. Chemical and biological sensing has been another important area where large surface to volume ratio enhances detection limit and make nanowire sensors as potential candidates [3, 4]. The giant piezo-resistive coefficient and reduced low frequency noise make the nanowires suitable for transducer world [5]. Nanowires have also shown excellent potential in the area of photonics [6], solar energy harvesting [7, 8], and energy storage [9]. Fundamentally, the improved properties of nanowire devices are a result of a combination of shape, density, and strong confinement of photon, phonon and electrons and their relative changes in reference to planar bulk structure.

The fabrication technology of nanowire can be broadly categorized into two groups: (i) the bottom-up and (ii) the top-down. The bottom-up approaches involving synthesis of nanowires have been extensively reviewed in the literature [10–12] and are not discussed in further detail here.

The top-down approach starts with pattern definition, mainly using conventional lithography, followed by pattern transfer and then trimming to reduce the diameter of the wire to nanoscale. Although isotropic wet etch can be used to trim the wire diameter, self-limiting oxidation process
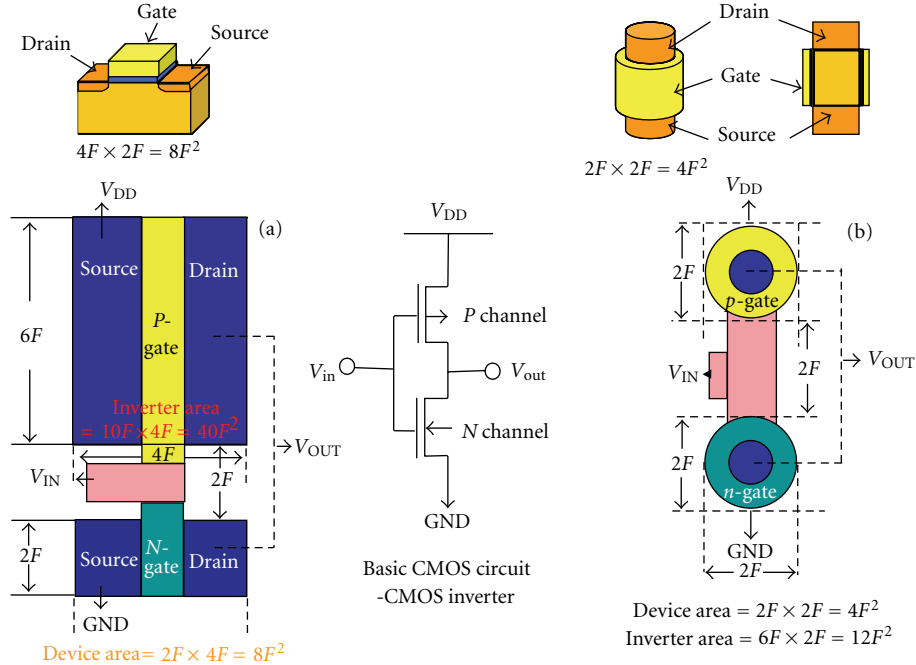
FIGURE 1: Schematic illustration of the footprint of (a) lateral and (b) vertical GAA nanowire MOSFET and corresponding CMOS inverters.

is generally used for better process control and has been extensively exploited at our institute [13].

In this paper, we review the progress of our top-down vertical nanowire technology platform from low power electronics and clean energy applications view point. A review of lateral nanowire platform focusing logic, nonvolatile memory, and biosensing applications has been published recently [13] and therefore will not be included here. The vertical platform resolves most of the fabrication-related challenges of lateral nanowires, for example, gate definition under the wire, gate etching on the wire, lithography, free gate length control and provides CMOS circuits with much smaller foot print as compared to any lateral (including planar, Fin, nanowire) MOS transistor at the same technology node. Being vertical, it decouples source/drain (S/D) implant processes and therefore acts as a natural platform for tunneling FETs—allowing independent tuning of S/D junctions and implant type for achieving low subthreshold slope (SS) and suppressing ambipolar behavior. Nonvolatile memory devices on vertical wires have the potential to be stacked vertically along the wire length in addition to footprint benefit similar to the CMOS. Under the green electronics title, Section 2 discusses the scaling through vertical approach followed by our progress on three electronic devices, namely, Metal-Oxide-Semiconductor field effect transistor (MOSFET), Tunneling field effect transistor (TFET), and SONOS nonvolatile memory (NVM); all fabricated in GAA format. In Section 3, we discuss clean energy harvesting, where results on solar cell showing performance improvement through enhanced light trapping and absorption, and a fully CMOS compatible thermoelectric engine converting waste heat into electricity, are presented. The challenges and future

prospects with vertical nanowires are discussed in Section 4. Finally, Section 5 summarizes the paper.

2. Low Power Electronics

2.1. Scaling Through Vertical Approach. Vertical nanowire devices, having source, drain, and gate terminals on top of each other, occupy much less area than planar as described in Figure 1. In terms of half-pitch "F", generally the minimum lithographic printable feature size, a planar transistor occupies $8F^2$ while a vertical transistor can be designed in $4F^2$ thus reducing the foot print by 50% for a given technology node. When connected together to fabricate circuits, the impact is even more, for example, a CMOS inverter which uses $40F^2$ of area with planar devices can be fabricated in $12F^2$ using vertical nanowires, resulting in an area saving of about 70%. The area saving directly relates to improvement in speed and saving in power consumption through resistance "R" and capacitances "C", both of which scale directly with area. The circuit speed being inversely proportional to "RC"-constant increases by $\sim 6.1 \times$ (e.g., simply Speed $\propto 1/RC \propto (\text{Area})^{-3/2}$). The power consumption, being proportional to CV^2, reduces to 30% of the planar (e.g., Power $\propto CV^2 \propto (\text{Area})$). A summary of the area, speed, and power advantages with vertical nanowires devices as compared to planar and lateral nanowire is provided in Table 1. Worth mentioning here that these back-of-the envelop calculations do not take into account any parasitic.

Despite the same scaling potential from gate control perspective as for lateral wire, the vertical wire device takes lead over lateral wire in foot print scaling followed by speed and power advantage. Indeed the lateral wire device foot
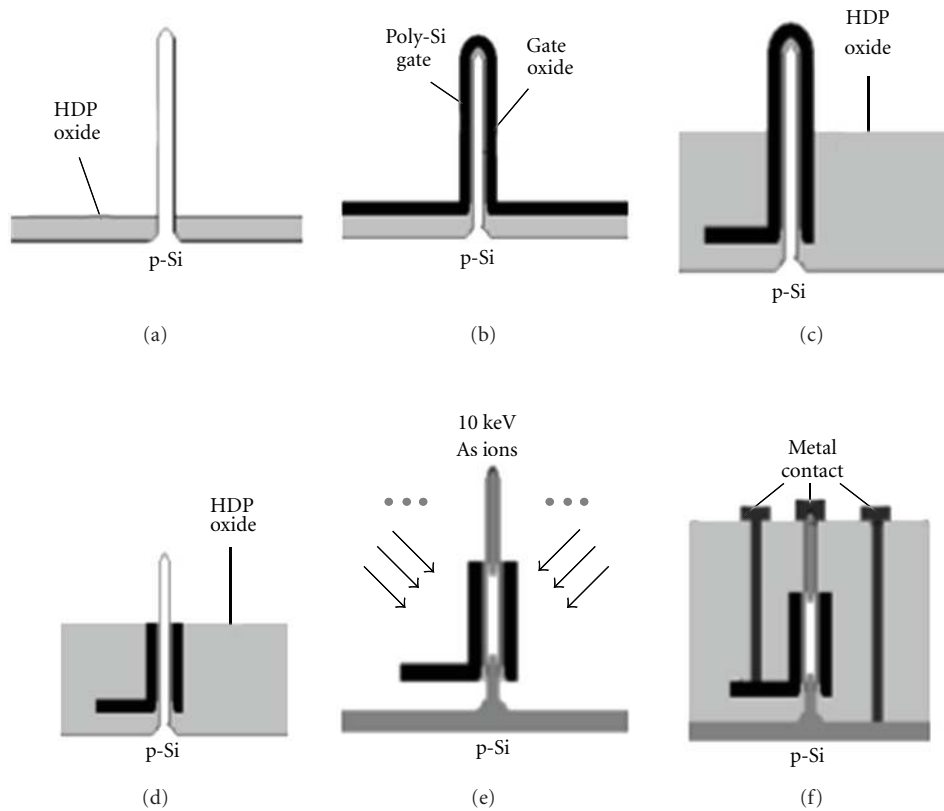
FIGURE 2: (a) Single silicon nanowire with bottom isolation, (b) after gate stack deposition, (c) after gate extension pad definition and HDP oxide deposition followed by etch back defining gate length, (d) after poly-silicon end cap removal, (e) removal of oxide followed by S/D and gate implant (single implant for all three electrodes), (f) final device after metalization. (Reprinted with permission from [15]. [2008] IEEE.)

print remains $8F^2$, the same as planar device. At circuit level, however, lateral nanowire can do little better than planar device as it can allow current matching with stacking of lateral wires, for example, forming two wires out of a Fin [14] and using both as channel for PMOS but only one for NMOS. In contrast, the current matching in vertical devices is possible with gate-length scaling without penalty on foot print. Further, the vertical approach is a route to resolve design and fabrication issues related to lateral nanowires. For example, defining uniform gate is a challenge as the shadowing effects in plasma etching may not allow clearing the gate material beneath the lateral nongated regions. Vertical GAA nanowire transistors are anticipated to be promising candidates as there is no shadowing effect issue and the gate length can be defined by the film deposition and etch back rather than lithography.

2.2. Integration Feasibility. We used GAA vertical nanowire CMOS transistors as test vehicle to develop vertical platform on 8″ silicon wafers [15]. The fabrication process steps of which are illustrated in Figure 2. Shown in Figure 3 are scanning electron microscopy (SEM) images taken as

TABLE 1: Benchmarking of lateral and vertical nanowire devices with planar.

	planar	NW (lateral)	NW (vertical)
Device circuit Areas (A)	$8F^2$, $40F^2$	$8F^2$, $24F^2$ Shrink ~40%	$4F^2$, $12F^2$ Shrink ~70%
Speed $\alpha 1/t$ α $(RC)^{-1}$ α $(A)^{-3/2}$	1	~ 2.2×	~ 6.1×
Power α CV^2 α $(A)^1$	1	~ 0.6×	~ 0.3×

various fabrication stages. Circular resist dots of different diameters (from 160 nm to 600 nm) were patterned using deep ultraviolet (DUV) lithography followed by 1 μm deep Si etch with SF_6 chemistry under resist mask. The etch depth can be tuned depending upon the device design. Si pillars were then oxidized at 1150°C to be converted into nanowires. High temperature was used to decrease the viscosity of grown oxide, ensuring smooth cylindrical Si core at the center of the pillar. The oxidation rate at the bottom of the pillar was low due to increased stress at high curvature [16, 17]. The
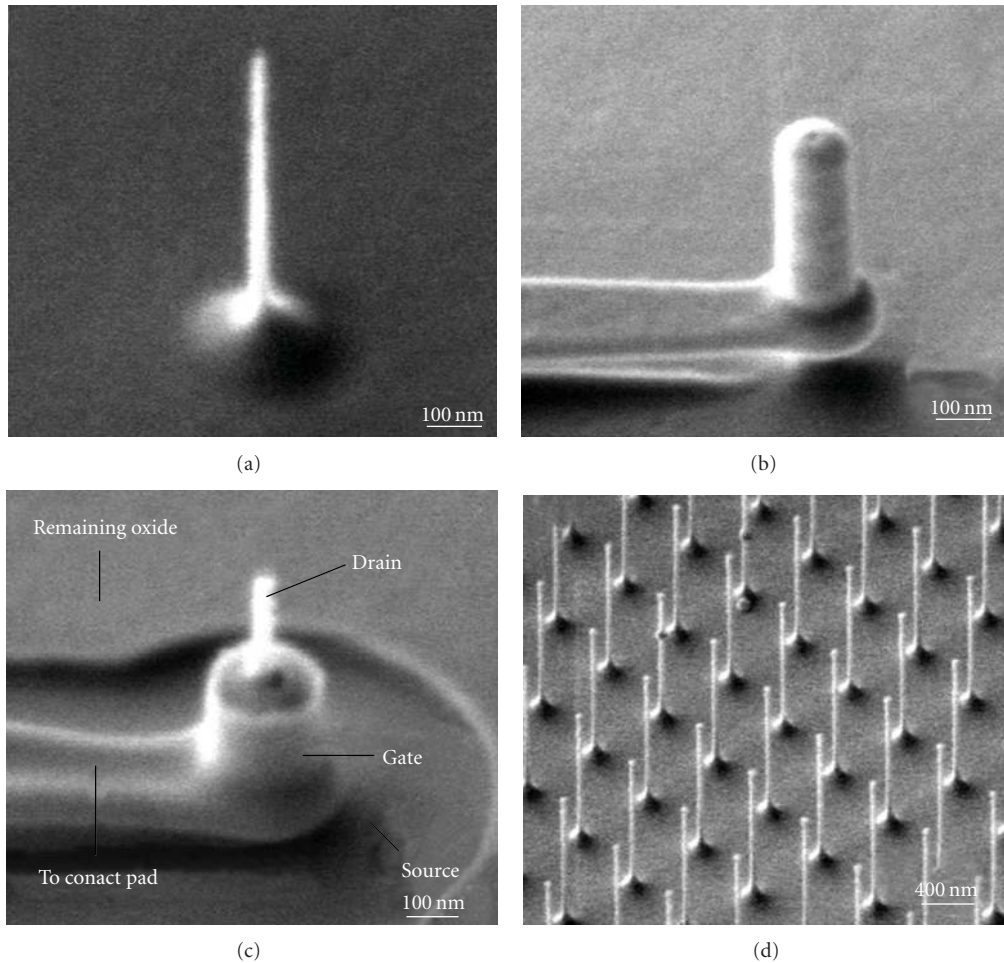
(a)

(b)

(c)

(d)

FIGURE 3: SEM pictures at different stages of device fabrication. (a) Vertical nanowire with diameter ~20 nm; (b) after gate patterning by lithography but before exposing the drain (the tip of the pillar) of the transistor; (c) after the drain (pillar tip) is exposed, ready for taking metal contacts, (d) vertical nanowire arrays with pitch of 500 nm. Nanowires are 1 μm tall with a diameter of ~20 nm. (Reprinted with permission from [15]. [2008] IEEE.)

grown oxide was then stripped in diluted HF (DHF). The SEM images of nanowire thus fabricated are shown in Figures 3(a) and 3(d).

Vertical nanowire formation was followed by a 250 nm thick layer of high density plasma (HDP) oxide deposition and wet etch-back using DHF (1 : 25). The HDP deposition resulted in thicker oxide on the bottom surface and thinner oxide along the nanowire sidewalls due to the nonconformal deposition. After wet etch-back ~150 nm, thick oxide remained to cover the footing of the vertical standing wire. This technique separates the gate electrode from the source extension pad and thus reduces the gate to source fringing capacitance. Gate oxide of ~5 nm was then thermally grown on the exposed wire surface, followed by deposition of 30 nm poly-Si, which serves as the gate electrode (Figure 3(b)). Gate pad was then patterned and etched under resist mask which covers the nanowire and provide a poly extension for gate contact. After gate pad etching, the process of HDP oxide deposition followed by wet etch back was repeated to access the poly on top of nanowire while protecting the gate

pad defined earlier. The exposed poly-Si was then isotropically etched by low RF power SF_6 plasma. Alternatively, this cap could be removed in wet Tetramethylammonium Hydroxide (TMAH) solution. The oxide on the wafer was then completely stripped in DHF (Figure 3(c)), and As (1 × 10^{15} cm^{-2}/10 keV) was implanted four times from four directions, 90 degrees apart, with large tilt angle (45 degree) It was followed by a rapid thermal annealing and standard metallization process.

Figure 4 shows typical characteristics from NMOS of channel diameter ~20 nm and PMOS of channel diameter ~40 nm, both having channel length of 150 nm. The device displayed very good performance with steep turn-on (SS~75 to 100 mV/dec), strong gate electrostatic control (extremely low Drain induced barrier lowering (DIBL) (10 to 50 mV/V)), and high I_{on}/I_{off} ratio (~10^7). However, the threshold voltage V_{th}, with poly-Si gate is much lower than required to integrate these devices into circuits [18–21].

Due to the small channel volume, conventional channel doping proves difficult with nanowires and may result in
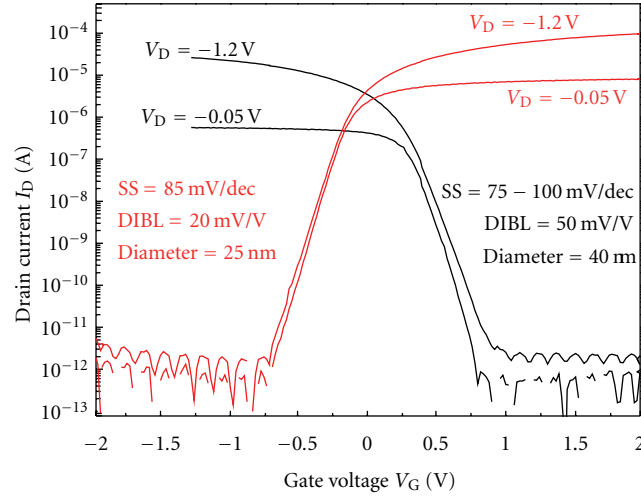
FIGURE 4: Transfer characteristics of GAA n- and p-FETs showing near ideal subthreshold swing indicating the excellent electrostatic control.
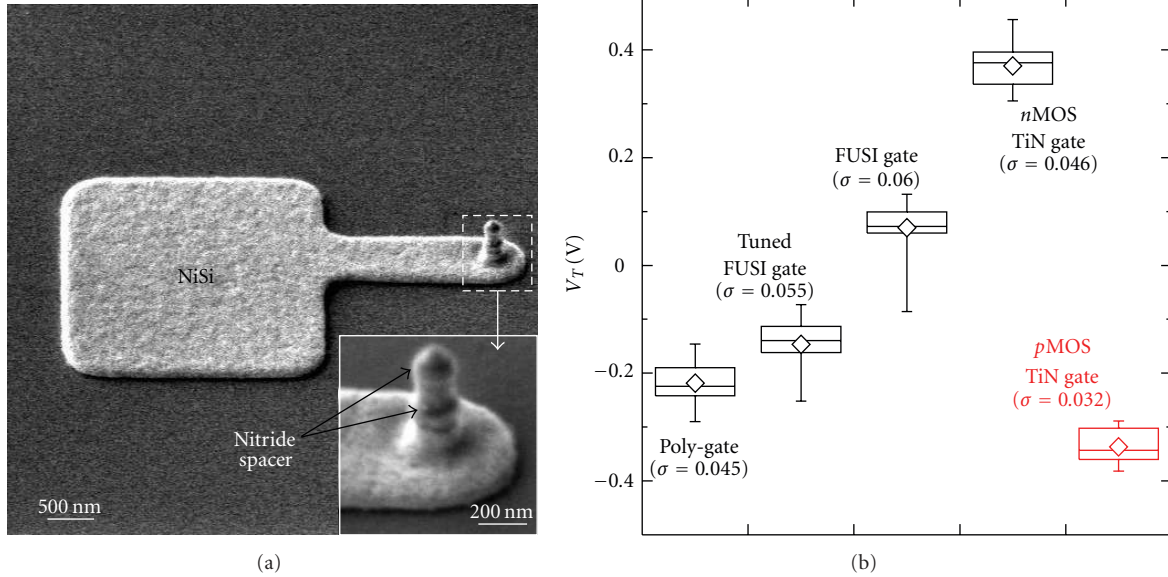

(a)

(b)

FIGURE 5: (a) A scanning electron microscope (SEM) image of an FUSI gate device after silicidation (440°C, 30 s) and removal of unreacted Ni in $H_2SO_4:H_2O_2:H_2O$ solution. (b) Box plots of the V_{th} distribution of measured devices for each split. V_{th} extraction using linear extrapolation was done for over 10 devices in each split.

significant V_{th} fluctuation due to dopant fluctuations in addition to mobility degradation. A better method of V_{th} adjustment is through gate work function tuning. We have implemented NiSi fully silicided (FUSI) and TiN gates, both with undoped nanowire channel. TiN is found to provide better symmetry for N and P devices, however, on the other hand, FUSI gate showed tenability with implant in gate poly-Si. Figure 5 presents SEM image of FUSI gate device and V_{th} values of both the TiN and FUSI gate devices.

The V_{th}-adjusted devices show distinct V_{th} shifts (ΔV_{th}) relative to each other as can be seen in Figure 5(b). The TiN PMOS and poly-gate NMOS have the lowest V_{th} (~ -0.38 V and -0.22 V), followed by the tuned FUSI gate device (~ -0.15 V) and the FUSI gate device (~ 0.07 V), while TiN NMOS has the highest V_{th} (~ 0.42 V). The TiN gate shows great potential in adjusting V_{th} for vertical SiNW MOSFETs to allow them to be integrated into low standby power circuits.

2.3. Turning MOSFET into Tunneling FET. Scaling of MOSFET to improve device performance and increase device density faces enormous challenges beyond the 22 nm node due to excessive increase in passive power. This arises due to the nonscalability of the SS that limits further reduction in MOSFET threshold voltage, V_{th}, and hence supply voltage, V_{dd}. To overcome this problem and to design more

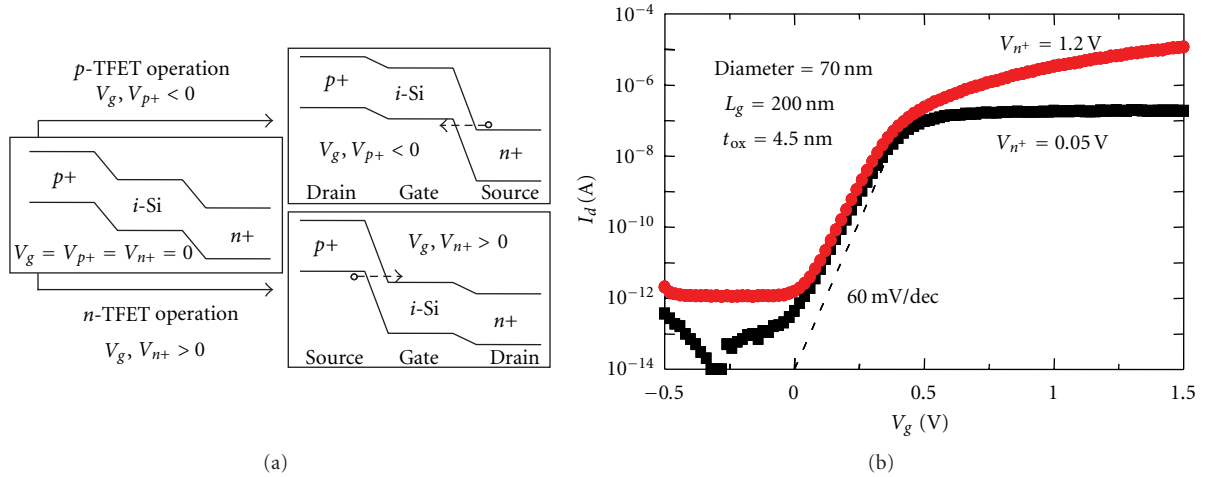(a)   (b)

Figure 6: (a) Band diagram of TFET showing tunneling junction, (b) I_d-V_g and characteristics of a vertical SiNW TFET with diameter 70 nm, gate length 200 nm and gate oxide thickness 4.5 nm. (Reprinted with permission from [28]. [2009] IEEE.)

energy-efficient devices, alternative transistor designs with low SS are needed. One of such devices is the TFET [22–28]. Unlike the MOSFET, which utilizes thermionic injection of carriers, TFET uses tunneling as the carrier injection mechanism. Therefore, it is possible for TFET to achieve low OFF state current as well as SS below the theoretical limit of 60 mV/decade for MOSFETs at room temperature. TFETs are essentially gated p+ −i −n+ diodes working under reverse bias and can operate as n- or p-TFETs. By controlling the i region with a gate, a tunneling barrier can be created either at the p+ −i (n-TFET, $V_G > 0$) or n+ −i (p-TFET, $V_G < 0$) junctions where carriers are able to tunnel through as shown in Figure 6(a) using band structure [27]. The reverse-biased p–i–n diode gives the TFET the low OFF-state diffusion current.

Leveraging on our vertical nanowire platform, tunneling FETs are fabricated similar to MOSFET using the same mask sets but with opposite type of source/drain doping. We used nitride hard mask to protect the wire top while implanting the bottom electrode. Shown in Figure 6(b) is the n-TFET I_d-V_g curves obtained from a device with diameter ∼ 70 nm, gate oxide thickness 4.5 nm, and gate length 200 nm. Excellent I_{on}/I_{off} ratio at V_{n+} = 1.2 V is observed (∼10^7), with an I_{off} (at V_g = 0 V) of ∼7 pA/µm and I_{on} (at V_g = 1.2 V) of ∼53 µA/µm (normalised with the wire circumference). The resulting record high I_{on} and low DIBL (∼17 mV/V) for this Si TFET is a result of the excellent gate control of the GAA nanowire structure. However, the obtained SS of 70 mV/dec is beyond the limit of kT/q (≈60 mV/dec), likely due to the tunneling junction ($p + −i$) not being perfectly abrupt.

To achieve SS < KT/q limit, we improve the abruptness of tunneling junction through a novel silicidation induced dopant segregation process [29] depicted in Figure 7. To demonstrate this experimentally, we used nanowires with height of 400 nm and diameter ranging from 30 to 200 nm. Afterwards, the bottom part of the nanowire was vertically implanted with BF$_2$ for pTFETs and with As for nTFETs to

form the drain regions of the TFETs. Isolation and gate stack was formed similar to presented for MOSFET. Then Source was implanted with As for pTFETs and BF$_2$ for nTFETs and thereafter followed by silicidation, which segregated the dopants to form abrupt source/channel junction. Finally, contact metallization was done.

The transmission electron microscopy (TEM) image showing vertical section of the fabricated p-TFET device is presented in Figure 8.

Figure 9 shows the I_d-V_g characteristics for both pTFET and nTFET, respectively. SS of 30 mV/decade averaged over a decade of drain current is obtained for both pTFET and nTFET devices. Improvement is due to the sharp doping profile at the source side as a result of dopant segregated silicidation, which causes dopants to pile up at the silicide edge [30, 31]. Suppression of ambipolar conduction is also achieved because of natural asymmetry of the vertical nanowire platform, which facilitates independent tuning of source and drain.

SS distribution with drain current is presented in Figure 10(a). SS below 60 mV/decade is achieved for 3 decades of drain current for pTFET and for more than 2 decades in the case of nTFET. The difference in SS behavior of pTFET and nTFET may arise because of the difference in the dopant segregation between As and BF$_2$ and wafer to wafer process variations. The impact on nanowire diameter on SS is presented in Figure 10(b); SS degrades with the increase of channel diameter. When channel gets wider, the gate electrostatic control on the channel region gets weaker or behaves more like a planar device. Moreover, for larger wires, the encroachment of NiSi into the wire is reduced, therefore, dopant gradient at the source-channel interface is less steep, and hence the SS degrades.

By using higher permittivity (high-κ) gate dielectric and low-bandgap materials at tunneling interface, ON current can be further enhanced [32, 33]. We also noted the difference in ON current between our pTFET and nTFET devices, that is because of the difference in the gate-drain underlap
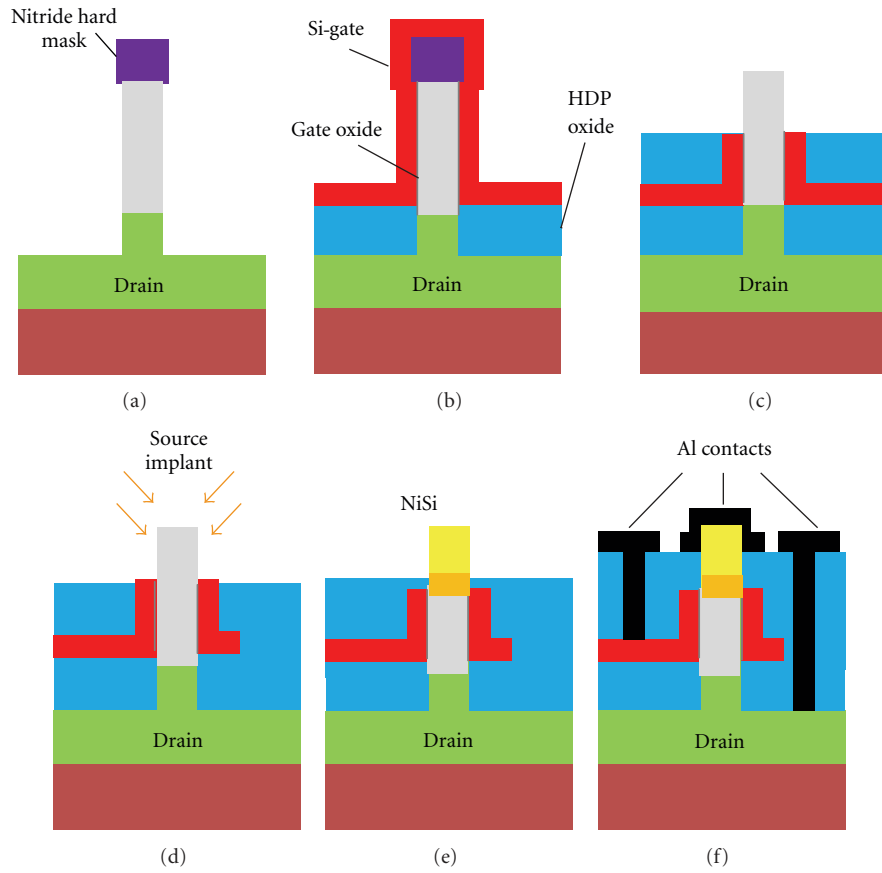
FIGURE 7: Vertical Silicon nanowire TFET process flow schematic. (a) Vertical pillar etch and As implantation to form the drain region, (b) isolation oxide deposition and gate stack formation, (c) the top amorphous-Si etched to expose source side of TFET, (d) source implanted with BF_2, (e) dopant segregated Ni silicidation, (f) contact opening and Al metallization. (Reprinted with permission from [29] [2011] IEEE.)
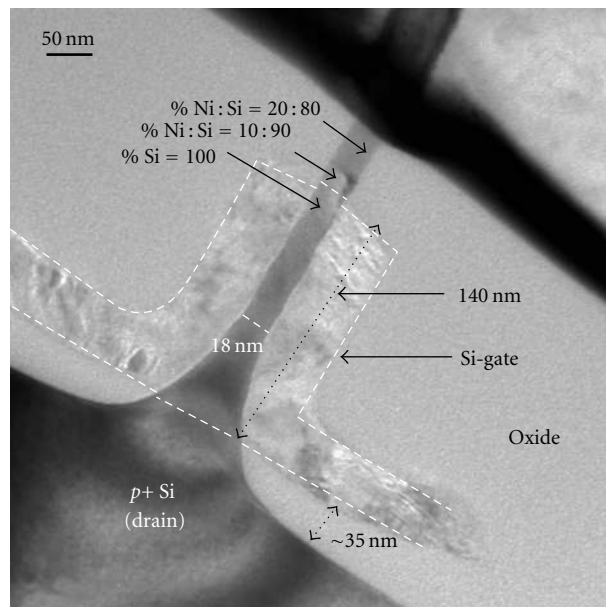

FIGURE 8: Cross-sectional TEM of pTFET showing a very narrow uniform wire surrounded with gate and silicide at top.
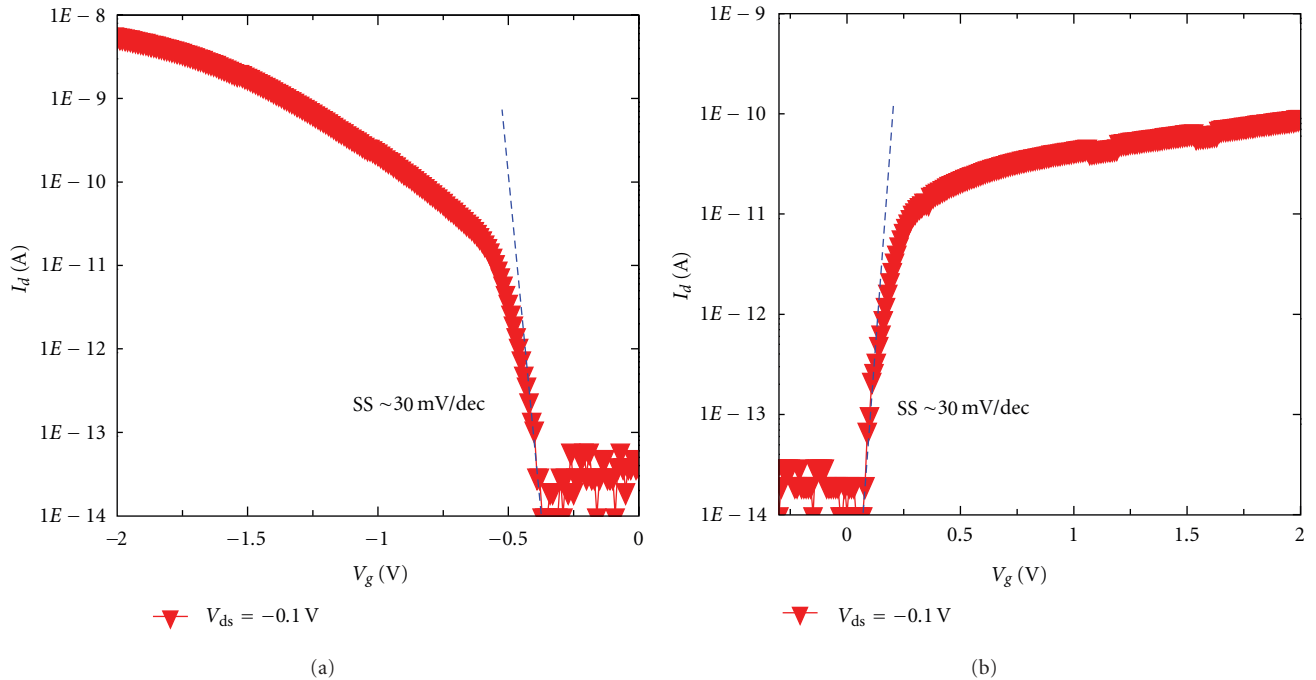
(a)

(b)

FIGURE 9: (a) Measured I_d-V_g characteristics of (a) p-TFET and (b) n-TFET with SS = 30 mV/decade averaged over a decade.
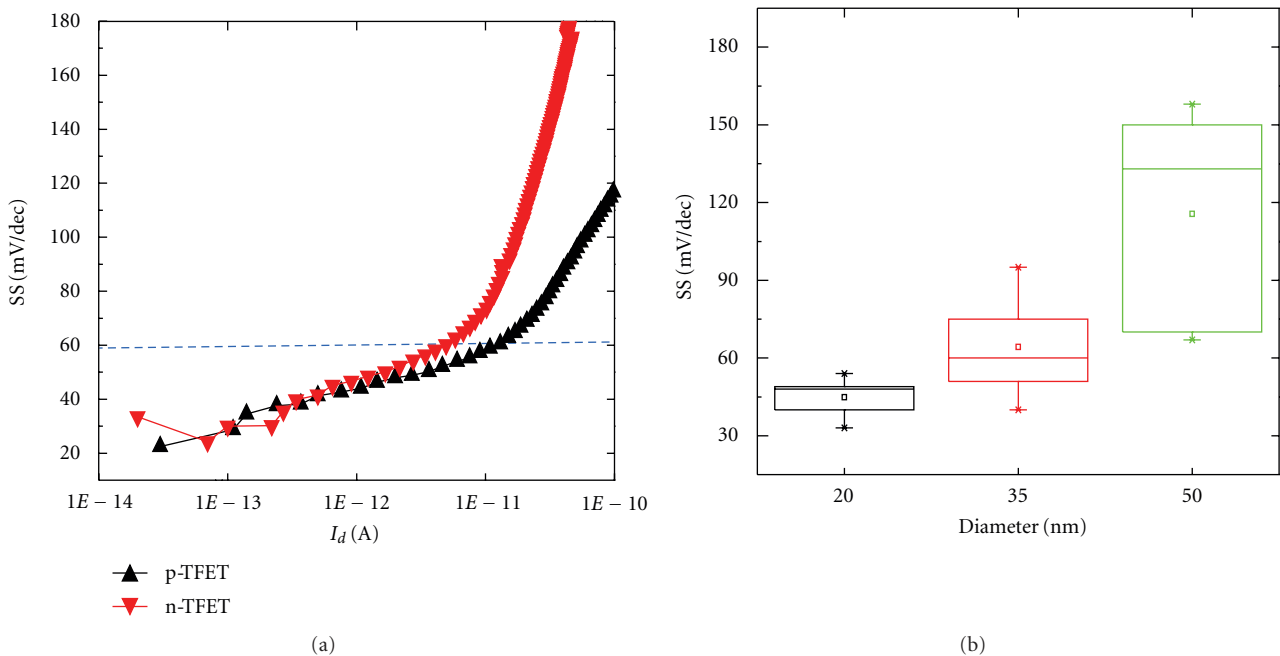

(a)

(b)

FIGURE 10: (a) SS versus I_d for TFETs. p-TFET exhibits sub-60 mV/decade swing for 3 decades of I_d, while n-TFET maintained sub-60 mV/decade for more than 2 decades of I_d (V_{ds} = 0.1 V). (b) SS variations on nanowire diameter of p-TFETs. SS increases as NW diameter gets wider.

thickness, pTFET has underlap of ~35 nm while nTFET has large underlap of ~100 nm. Large underlap on drain side seems to be one of the reasons suppressing the ON current of nTFET. Optimum gate-drain underlap is required to further suppress ambipolar conduction as well as to maximize ON current.

2.4. *Vertical Nanowire-Based Nonvolatile Memory.* Market of the nonvolatile memory has been booming persistently due to increasing demand of the portable electronic devices. It is currently dominated by flash memory having poly-silicon floating gate as the charge storage material. The floating gate memory, however, is facing rigorous challenges
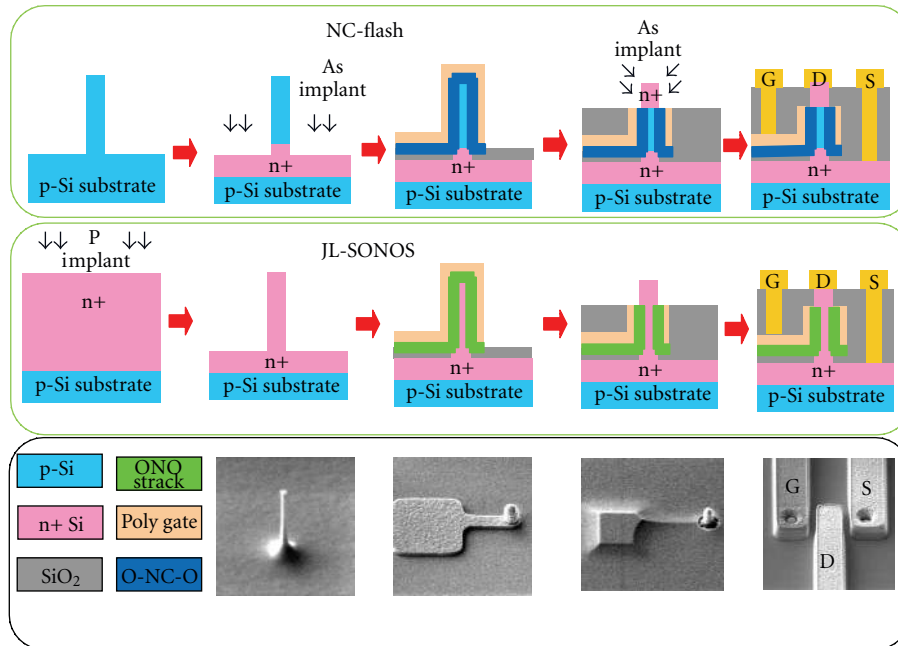
FIGURE 11: (a) Process integration flow of vertical SiNW junction-based NC-Flash: (a-1) vertical SiNW formation; (a-2) As is implanted to form the source; (a-3) gate stack deposition (O-N-O or O-NC-O for SONOS and NC-flash, resp.) and gate pad definition; (a-4) tip poly and O-NC-O removal, followed by drain implant; (a-5) metallization; (b) process integration flow of vertical JL-SONOS: (b-1) bulk implant and annealing; (b-2) vertical SiNW formation; (b-3) gate stack deposition and gate pad definition; (b-4) tip poly and ONO removal; (b-5) metallization; (c) tilted top view SEM image of SONOS/JL-SONOS fabrication during key process steps (left to right): vertical SiNW formation; gate pad definition; tip poly and ONO removal; metallization. (Reprinted with permission from [45]. [2011] IEEE.)

in the course of scaling beyond the 22 nm technology node because of significantly reduced coupling ratio and increased gate interference [34]. To overcome the scaling issues, the discrete charge trapped devices are being investigated widely. These devices use charge trapping materials such as silicon nitride, high-κ dielectric, and metal/silicon nanocrystals in place of conductive poly-Si floating gate and have simple fabrication process, lower programming voltage, and robust tolerances to defects in the thin tunnel oxide [35–40]. However, in discrete charge trap devices the gate dielectric thickness, for example, oxide-nitride-oxide (ONO) in case of silicon nitride as trap layer, is hard to scale due to the data retention concerns, and therefore it is difficult to avoid concomitant problems of severe short channel effects with scaling.

From transistor structure view point, the cylindrical architecture relaxes the requirement for ultrathin gate oxide and therefore is promising for SONOS-type nonvolatile memory, where thicker tunnel/block oxide is favored for longer retention time [41]. Apart from the superior gate control and electric field enhancement at tunnel oxide to channel interface, observed from the lateral- nanowire-based GAA SONOS cell [42], memory cell fabricated on vertical nanowires platform has more implication due to its small foot print and potential for 3D multilevel integration [43].

In our recent work, we fabricated a gate-all-around (GAA) SONOS flash memory on a vertical Si nanowire (SiNW) of diameter of 20 nm as the channel and presented excellent program/erase (P/E), retention, and endurance

characteristics [44]. The performance was further improved by replacing the charge trap layer with silicon nanocrystals (NC). The fabricated cells were an important building-block towards three-dimensional (3D) multilevel integration for ultrahigh density application. Though looks simple, vertical stacking of memory cells could be very challenging in forming junctions on nanowires between the cells. To overcome the junction formation issue, we also designed and fabricated a novel junction-less vertical SiNW-based SONOS cell. Being free of doped junctions, the junction-less (JL) memory device makes vertical SiNW a suitable platform for vertical stacking of memory cells to achieve ultra-high density application. The fabrication steps of our memory cells are sketched in Figure 11 and their detail are available in [45]. Just to highlight here, the JL-SONOS process was started with phosphorus implantation in p-type Si wafer followed by furnace annealing to create a uniform doping profile with different concentrations in the upper portion of the substrates. After that it follows the process flow of conventional junction-based vertical SiNW SONOS to form the wire channel and p-type doped poly-Si gate without S/D implantation, as shown in Figure 11(b). The absence of junctions on wire allows easy stacking of multiple cells on a nanowire.

Shown in Figure 12(a) is a cross-sectional TEM image of a vertical SiNW GAA JL-SONOS with wire diameter equals to 20 nm and gate length of ~120 nm. Figure 12(b) shows the cross-sectional TEM image of the gate stack with ONO thickness 5/7/7 nm. An atomic force microscopy

(a)

(b)

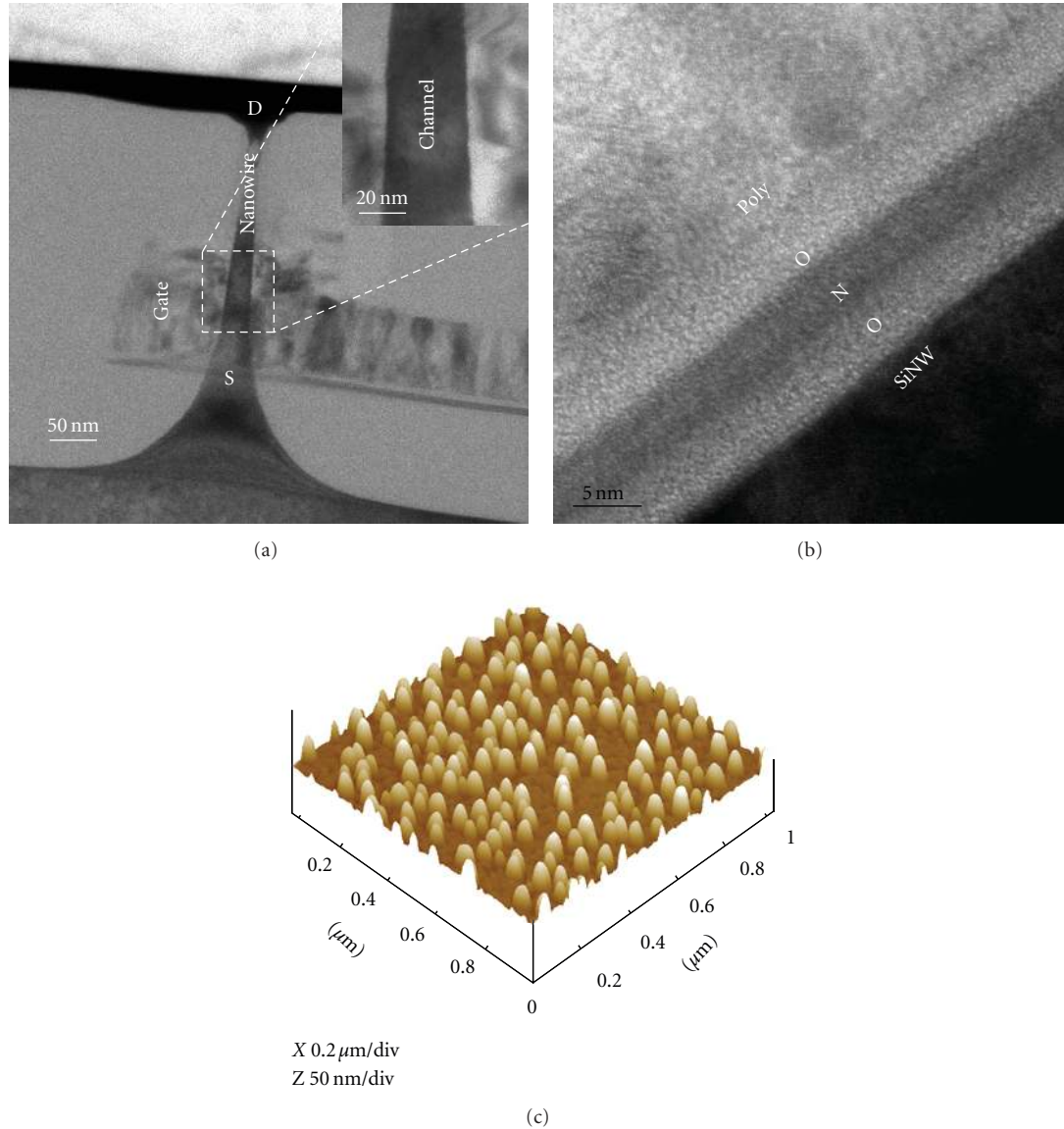X 0.2 μm/div
Z 50 nm/div

(c)

FIGURE 12: (a) Cross-sectional TEM image of vertical SiNW GAA JL-SONOS: diameter of wire is 20 nm and gate length 120 nm, (b) Cross-sectional TEM image of gate stack showing ONO thickness 5/7/7 nm. (c) AFM image scanned on $1 \times 1\,\mu$m^2 surface area that reveals the formation of Si-NC with a density of 7.5×10^{10}/cm^{-2}. (Reprinted with permission from [45]. [2011] IEEE.)

(AFM) image over $1\,\mu$m $\times$ $1\,\mu$m area of the nanocrystals deposited on tunnel oxide (in case of NC-flash) is shown in Figure 12(c). It reveals good uniformity and isolation between Si-NCs, although the size is big ($\sim$30 $\pm$ 10 nm in diameter) and density is low (around 7.5×10^{10}/cm^{-2}), indicating lot of room for further improvement. The effect of embedding SiNCs as trapping layer is illustrated in Figure 13(a) by comparing the P/E speed of NC-SOncOS with the control SiN-SONOS cell, both on 50 nm thick wire. The NC-SOncOS shows larger ΔV_{th} for the same P/E time period, indicating a better charge storage capability. The results indicate that the trapping centers in devices using silicon nanocrystals as charge trapping medium are superior than that of SiN, which enhances the trapping efficiency of the devices.

As can be seen in Figure 13(b), a partial window closure ($\sim$30% projected after 10 years) is observed for SiN-SONOS after 10^5 seconds 85°C retention for which the devices were programmed at 15 V for 100 μs and erased at -18 V for 1 ms. Incorporating SiNCs into the trap layer can significantly improve the charge loss by forming isolated energy wells due to conduction band offset [46] between Si and dielectrics. As shown in Figure 13(b), after SiNCs incorporation, the retention characteristics show great improvement and negligible memory loss was observed after 10^5 seconds retention at 85°C. Excellent endurance properties have been obtained for both SiN-SONOS and NC-Flash devices.

The characteristics of junction-less cells are presented next. Figure 14 illustrates the P/E characteristics of JL-SONOS with channel doping of 1×10^{17} cm^{-3} and
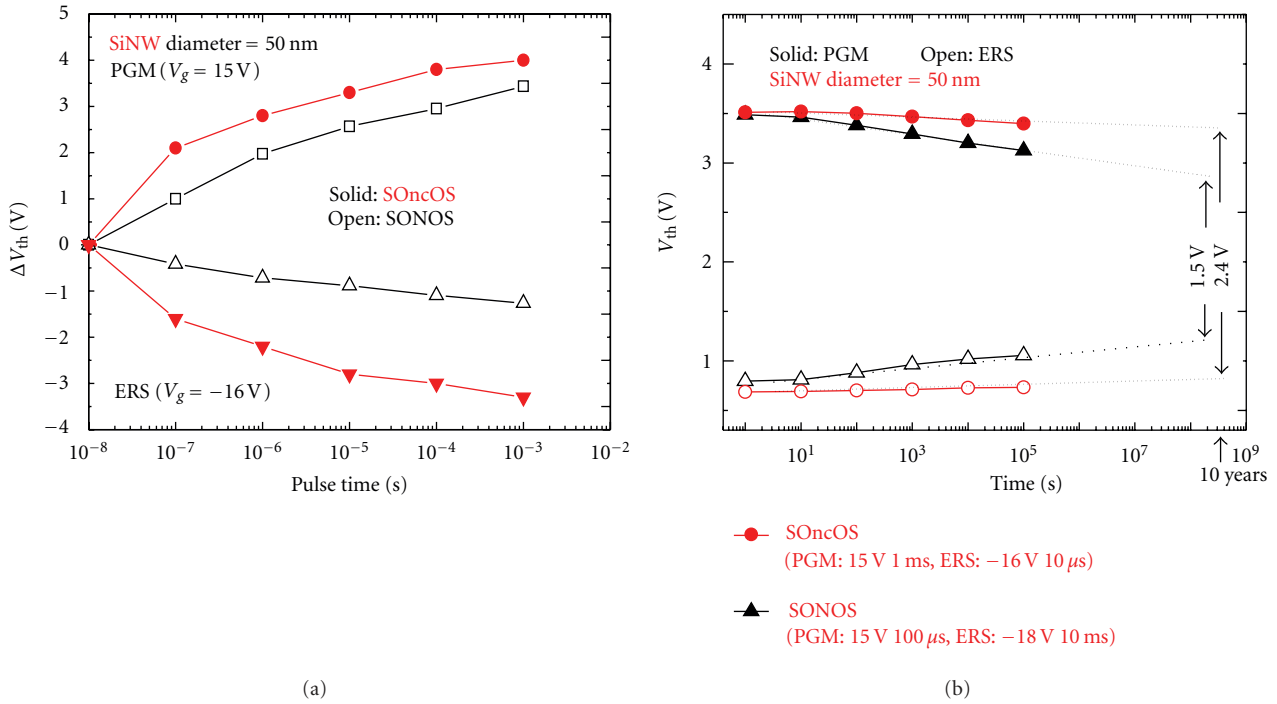
(a)

(b)

Figure 13: (a) Comparison of P/E speed between vertical SiNW-based NC-SOncOS and SiN-SONOS, with gate length of 150 nm and wire diameter of 50 nm. (b) Retention characteristics at 85°C for vertical SiNW-based GAA SONOS and NC-SOncOS. (Reprinted with permission from [45]. [2011] IEEE.)
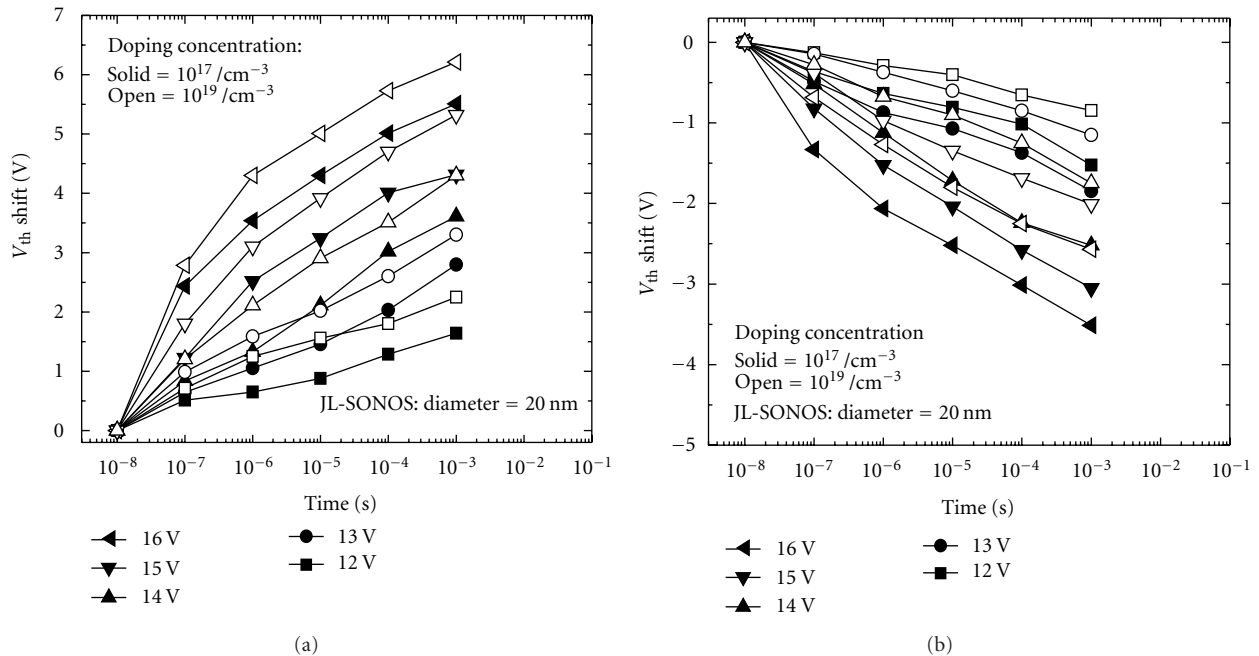

(a)

(b)

Figure 14: (a) Programming and (b) erasing characteristics using FN tunneling of vertical SiNW-based GAA JL-SONOS memory device with channel doping of 1×10^{17} cm^{-3} and 1×10^{19} cm^{-3}. (Reprinted with permission from [45]. [2011] IEEE.)

1×10^{19} cm^{-3}, respectively, for a fixed wire diameter of 20 nm. For both the doping concentrations, the memory window is nearly same, more precisely, 3.2 V for low doped (1×10^{17} cm^{-3}) and 2.7 V for moderately doped ($1 \times$ 10^{19} cm^{-3}), when a P/E time of 1 ms was used at +15 V/ −16 V, respectively.

Shown in Figure 15 is the feasibility on the multibit programming for the JL-SONOS measured on cell with
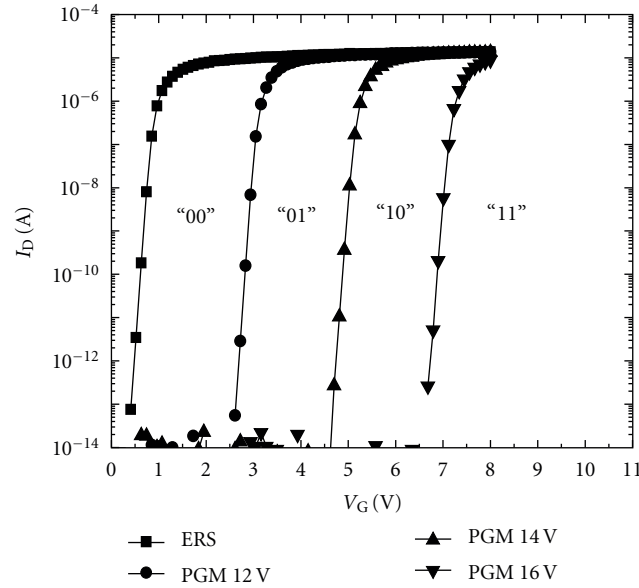
FIGURE 15: Multibit programming characteristics of JL-SONOS memory with a gate biases of 12, 14, and 16 V for 1 ms. Wire diameter = 20 nm, channel doping = $1 \times 10^{19}/\text{cm}^{-3}$. (Reprinted with permission from [45]. [2011] IEEE.)
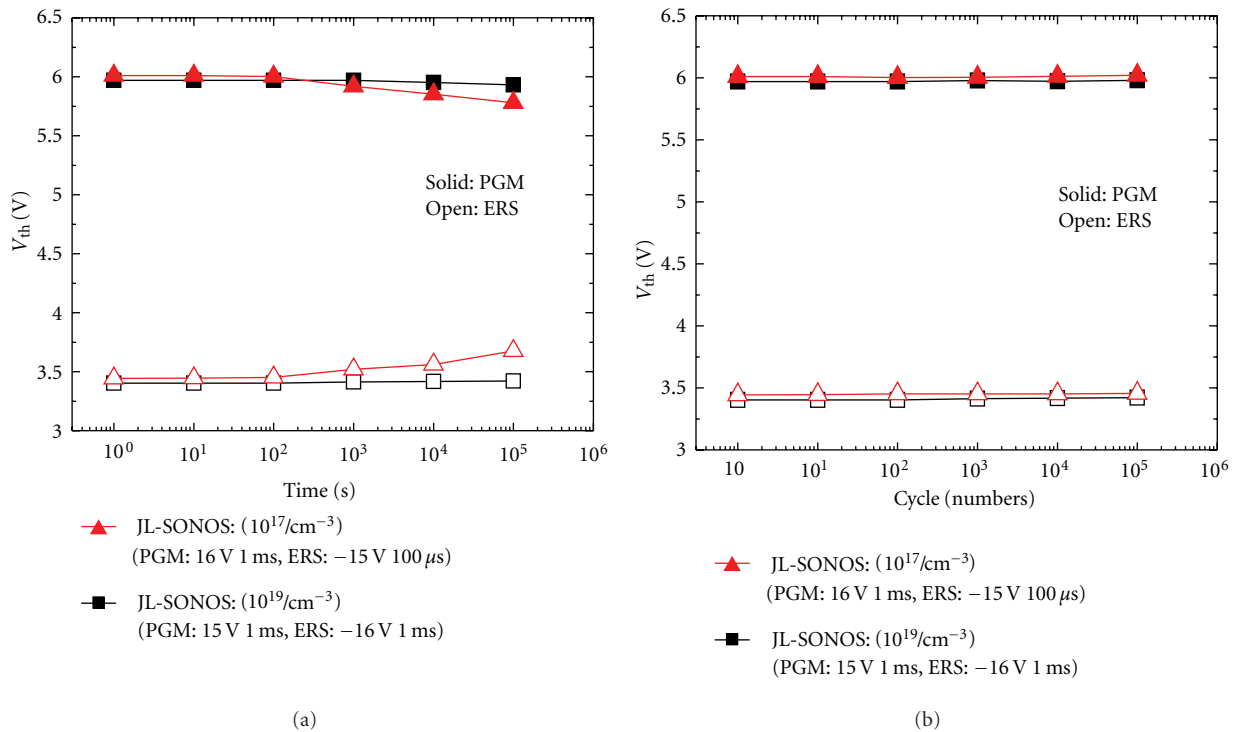

(a)

(b)

FIGURE 16: (a) Retention characteristic at 85°C for JL-SONOS memory device with channel doping of 1×10^{17} cm^{-3}.and 1×10^{19} cm^{-3}. (b) Endurance characteristic at 85°C for JL-SONOS memory device with channel doping of 1×10^{17} cm^{-3}.and 1×10^{19} cm^{-3}. (Reprinted with permission from [45]. [2011] IEEE.)

doping 1×10^{19} cm^{-3}. As obvious from the figure, the memory cell is able to store 2 bits per cell using four states "00", "01", "10", and "11" with each state defined a different V_{th} of >1 V.

The high temperature retention characteristic at 85°C for JL-SONOS is shown in Figure 16(a). The JL-SONOS

with high channel doping (1×10^{19} cm^{-3}) exhibits less V_{th} degradation as compared to lightly doped JL-SONOS (1×10^{17} cm^{-3}), and its memory window can be well maintained up to 10^{5} sec. Under retention conditions, direct trap-to-band (TB) tunneling from a nitride traps to the channel conduction band is the main discharge mechanism. With
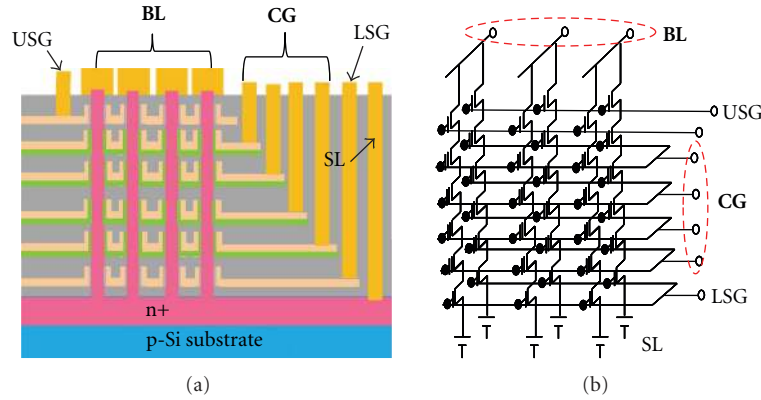
(a) (b)

FIGURE 17: Schematic of 3D multilevel stacked NAND using JL-SONOS as building blocks.

increased channel doping, the energy states close to the channel conduction band are more likely to be occupied by electrons. This reduces the probability of further electron injection from the trap layer, and thus more reliable charge storage can be expected [47]. The endurance characteristic of JL-SONOS is shown Figure 16(b), in which all devices can maintain the P/E window after 10^5 cycles at 85°C.

A possible 3D memory cell circuit design based on vertical SiNW JL-SONOS is illustrated in Figure 17. Without using junction for both selection gate transistors and memory cell, the integration process would be significantly simplified.

3. Clean Energy

3.1. Vertical Nanowire-Based Solar Cell. Si thin film solar cell is considered for the next generation of solar cell as it provides a viable pathway towards low material and production cost [48]. Nonetheless, the thickness of Si thin film is much lower than the optical thickness to absorb 90% or more of the above-band-gap-photons [49], limiting the total power conversion efficiency (PCE). One of the possible approaches to enhance the light absorption is the integration of Si nanostructure on thin film. In addition to many other optical phenomenons, diffraction of light plays a key role with nanostructured surface making poorly absorbed red light to enter at higher angle into the film, thus improving the chances of absorption. Although, the exploitation of Si nanowire or nanopillar (SiNP) in solar cell application [49–53] has been widely studied over the past decade due to its excellent optical [53–56] and electrical properties [49, 52], there was not much systematic analysis that could guide design of high efficiency solar cells. Our group did a very through simulation-based study [7] and followed that by experimental verification [8]. We found the optimized pillar diameter (D) is $0.20\,\mu$m, at diameter/periodicity (D/P) ratio of 0.5 (i.e., periodicity $0.4\,\mu$m) and height (H) $1\,\mu$m [7, 56], the SEM image of which is shown in Figure 18(a).

We comprehensively study the electrical characteristics of the optically optimized structure for both the axial and radial *p-n* junctions using simulations. Our simulations incorporate optical properties of the device studied by using 3D Finite Element Method (FEM). The light is assumed to be incident normally to the SiNP array, under AM 1.5 G 100 mW cm^{-2} spectrum. The electric field ($\vec{E}$) at each coordinate of the 3D simulation grid is calculated and exported to the Cogenda Genius Simulation Manager [57] for electrical solving the current continuity equation and Poisson's equation self-consistently. The calculations of the current-voltage (J-V) characteristic of the SiNP solar cell follow the description in [58]. Drift-diffusion model is implemented for carrier transport within the device. Shockly-Reed-Hall (SRH) and Auger recombination are also taken into consideration.

We discuss only axial junction (device in Figure 18(b)) here. Shown in Figure 19(a) is the effect of minority carrier diffusion length on short circuit current I_{sc} and open circuit voltage V_{oc}. Inset shows the PCE comparison with planar reference device. It can be observed that a diffusion length as poor as $0.6\,\mu$m is tolerable with our design, showing the possibility of exploitation of low-grade Si in photovoltaic application to lower the production cost [59]. Indeed a PCE of 17.4%, assuming surface recombination velocity "S" = 0 cm-s^{-1}, is predicted with small minority carrier diffusion length for electron ($L_n \geq 0.6\,\mu$m). Figure 19(b) shows the photo-generated carrier concentration with a clear concentration effect inside the wire. Designing the junction location inside this highly concentrated area is the key of getting high performance. Further, it is worth mentioning that though bulk recombination is lowered in thin film solar cell, and the Auger and surface recombination may increase due to higher carrier densities near the surface. It would have a negative impact on the short circuit current density (J_{sc}) and open circuit voltage (V_{oc}) [60], especially for nanopillar solar cell due to the increased surface area and absorption near the surface. We found a decrease in PCE from 17.4% to 15.5% with S increased from 0 cm-s^{-1} to 1000 cm-s^{-1}, indicating its detrimental impact [7].

Next we present our experimental results of axial junction nanopillar solar cells, the fabrication details of which are available in [8]. Owing to the significantly enhanced light absorption of the optimized SiNP array texturing,
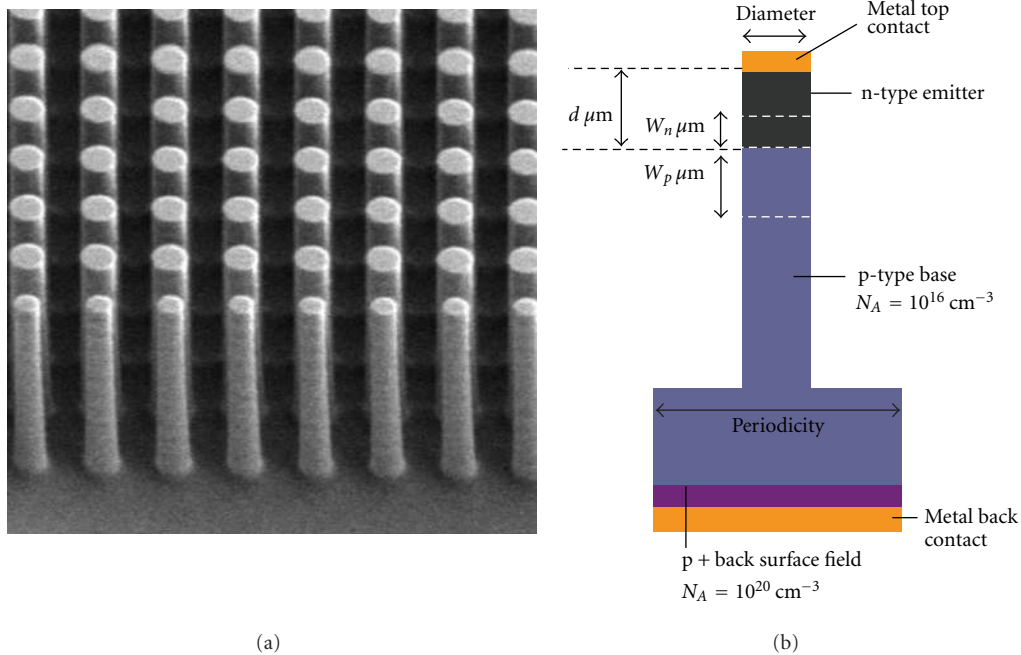
(a)

(b)

FIGURE 18: (a) SEM image of a Si nanopillar pattern used for simulating PCE analysis. Pillar parameters are diameter = 200 nm, pitch = 400 nm, and height = 1000 nm; (b) crossectional schematic of axial junction. (Reprinted with permission from [8]. [2010] IEEE.)

(a)

(b)

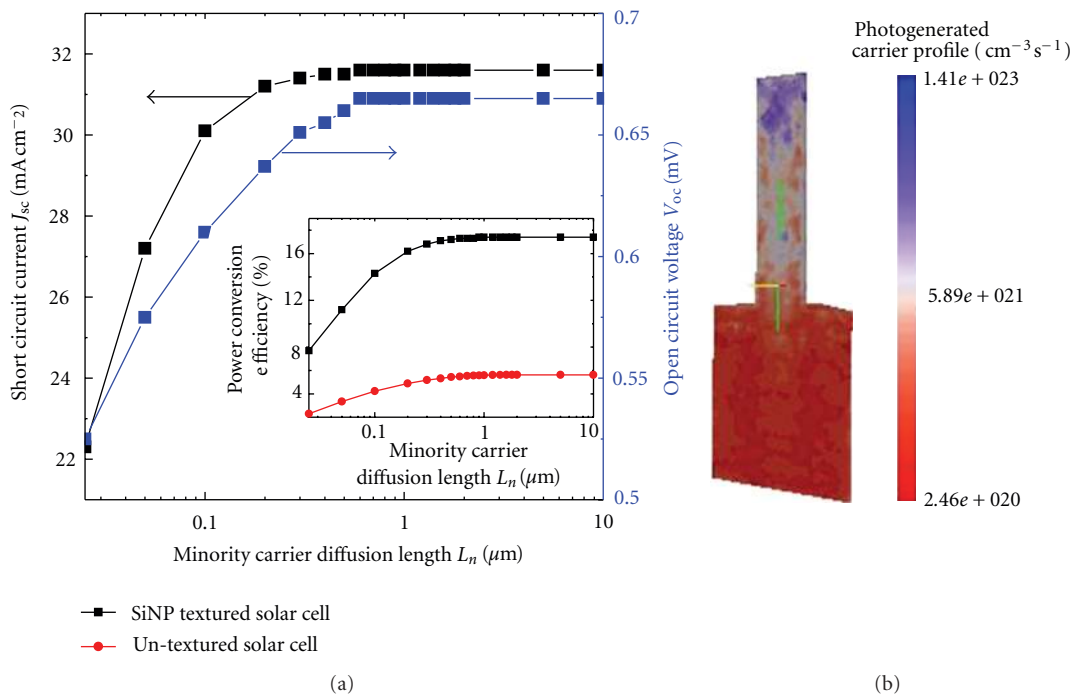FIGURE 19: (a) Short circuit current and open circuit voltage of the SiNP textured solar cell at various L_n. Inset is the efficiency of the SiNP textured and untextured solar cell; (b) photo-generated carrier profile G in a Si nanopillar textured thin film solar cell at $L_n = 0.6\,\mu$m. (Reprinted with permission from [59]. [2010] IEEE.)

a short circuit current density (J_{sc}) of 34.3 mA/cm^2 is realized on axial p-n junction inside SiNP surface textured solar cell, which is the highest to date among reported Si nanowire (SiNW)/SiNP-based solar cells. This is in distinct comparison to J_{sc} of 18.1 mA/cm^2 demonstrated on the solar cell without SiNP.

Shown in Figures 20(a) and 20(b) are the microscope images of the nanopillar-based and planar solar cells,
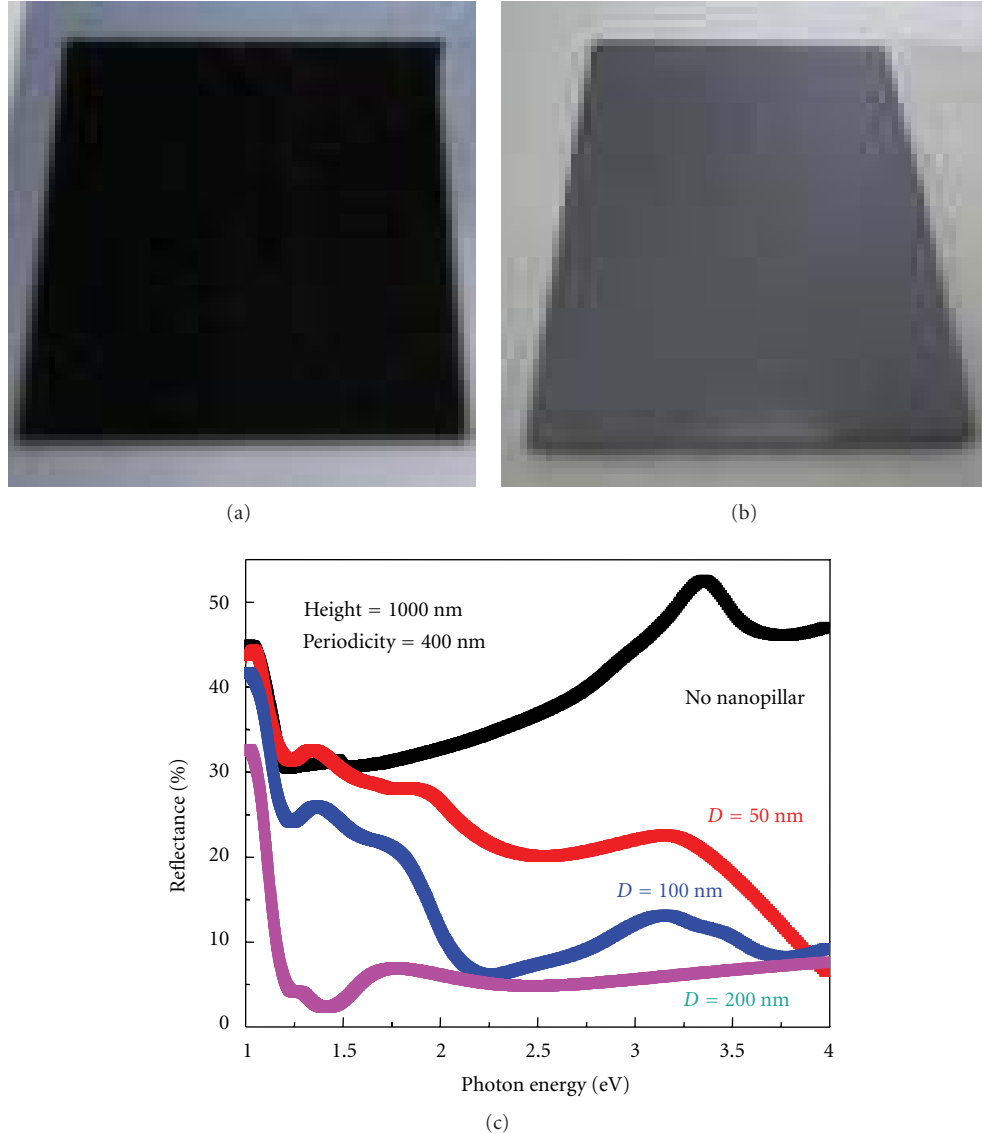
(a)

(b)

(c)

FIGURE 20: Photographs of (a) SiNP textured and (b) untextured solar cell (without top TCO layer). (c) Reflectance spectra with varying parameters. (Reprinted with permission from [8]. [2010] IEEE.)

respectively. It is clearly observed that the textured solar cell appears darker than the untextured one due to its superb antireflection properties. In align with our previous theoretical prediction, the lowest reflection is achieved when the SiNP diameter is 200 nm as shown in Figure 20(c) (e.g., D/P is 0.5) [7, 56].

The external quantum efficiency (EQE) was measured to investigate efficiency of the light absorption and carrier separation/carrier collection for the device (Figure 21). The doping concentration of the emitter (with junction depth of 250 nm) and back surface is 10^{20} cm^{-3}, and the doping level of base is 10^{16} cm^{-3} in the devices. The illuminated condition is AM 1.5G, that is, 100 mW cm^{-2}. Figure 21 depicts the EQE in the main energy range of solar spectrum as a function of SiNP diameter. The EQE of SiNP array textured devices is much higher than that of untextured one, indicating that the

photons are more efficiently absorbed. The device textured by the SiNP array with D of 200 nm (or D/P of 0.5) and H of 1000 nm has the best EQE (>200% of the untextured one), implying the excellent light trapping and carrier extraction capability for the sample with optimized surface texturing. The results are also well matched with the aforementioned reflection measurement and simulation result [7].

The short circuit current "J_{sc}" measured under AM 1.5 G 100 mW cm^{-2} illumination for nanopillar devices with various diameter is shown in Figure 22(a) along with simulated current-voltage graphs in Figure 22(b). The measured J_{sc} increases with increasing D/P ratio, and the trend is in good agreement with the simulation results and EQE data.

The J_{sc} of SiNP surface textured device is boosted to a maximum of ~31.4 mA/cm^2 with pillar D of 200 nm, which is ~1.7 times larger than that of the untextured device
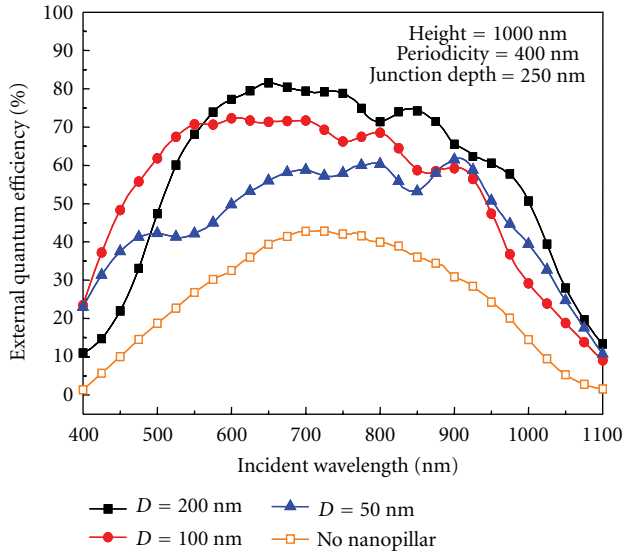
FIGURE 21: External quantum efficiency for various pillar diameter showing best result for 200 nm pillar diameter under AM 1.5 G 100 mWcm^{-2} illumination. (Reprinted with permission from [8]. [2010] IEEE.)

(18.1 mA/cm^2). To the best of our knowledge, the device in our work achieved the highest J_{sc} using the nanopillar p-n junction.

In brief, nanowires are shown to have high potential for improving solar cell performance through improvement in reflection /absorption behaviour. With proper design, poor quality silicon is shown to be acceptable and does not deteriorate performance till diffusion length is as low as $0.6\,\mu$m. High short circuit current is demonstrated experimentally with an improvement of $1.7\times$ in comparison to planar cell.

3.2. Vertical Nanowire-Based Thermoelectric Cooling/Thermoelectric Generation. With the aggravation in the high heat flux fields like 3D electronics, implantable bioanalytical devices, and semiconductor lasers, the thermal map of general electronics has become extremely uneven and detrimental to the devices' performance [61]. Besides a growing need to cool down the local hot spots generated, there is an even more attractive opportunity to harvest the surplus heat. However, chip level harvesting has not been feasible due to the low thermoelectric conversion efficiency of current bulk materials and also due to a lack of proper CMOS compatible material.

The basic principles of thermoelectric cooling/thermoelectric generation (TEC/TEG) are based on Peltier or Seebeck effects where all electric current is accompanied by heat current and vice versa. A thermoelectric device can alternate between being a power generator via heat to electrical current conversion or a cooler via electrical current carrying away the heat [62]. The efficiency of the thermoelectric modules is dictated by the dimensionless figure-of-merit ZT, that is, $S^2\sigma T/\kappa$, where S, σ, k, T, are Seebeck coefficient, electrical conductivity, thermal conductivity, and absolute

temperature, respectively. Commercial state-of-art thermoelectric materials-alloys of Bi, Te, Sb, and Se have ZT $\geq$ 1 at room temperature [62]. However, these materials are difficult to handle and process like silicon technology, which is widely used in the semiconductor industry. Although thermoelectric materials have their performance limited in their bulk form, their low-dimensional nanostructures seem to outperform expectations [63]. Silicon, which was never considered for thermoelectric applications in its bulk form, has become a potential contender at the nanoscale. Studies show that the thermal conductivity of a 50 nm wide SiNW is reduced by 2 orders (to a k of 1.6 W/mK) resulting in an improvement in the ZT value to 1 from the bulk material of 0.01. The tremendous reduction of κ is attributed to the effect of phonon boundary scattering at nanoscale [64–69]. This significant discovery opens up a window for chip-level thermoelectric energy harvesting with potential to be integrated into conventional electronic circuitry. With Silicon as the TEG material, the use of Bi$_2$Te$_3$-based materials can be avoided.

We recently reported a top-down CMOS compatible integration technology for SiNW-based TEG [70], the schematic flow of which along with SEM images is shown in Figure 23. The P and N SiNW elements are connected at the top by Aluminum and at the bottom through metal-silicide formed by selective silicidation. This SiNW-based TEG is highly scalable and appropriate for chip level cooling and power generation due to the ease of integration with other CMOS ICs. The microscope image of the completed device is shown in Figure 24(a) with stack details during measurement in Figure 24(b). It had a total surface area of 5 mm × 5 mm (60% filled with doped wires) and consisted of 162 thermocouples.

The power generation of the device was characterized by heating one side using a copper heater designed and fabricated on separate wafer and attached to device under test. The heater die also had temperature measurement devices. Shown in Figure 25(a) is the open circuit voltage, V_{oc} across the TEG with different temperatures generated across the device "dT". As expected, an increase in V_{oc} is observed with an increase in dT. A V_{oc} of 1.5 mV was measured under an overall applied dT of 70 K across the whole experimental setup (0.12 K across the SiNW). A linear relationship across all data points is due to S = dV/dT relationship. With the thermal resistance values presented in Figure 24(b) and using S = dV/(NdT) on the largest V_{oc} measured across setup (dT = 70 K), the effective Seebeck coefficient of the TEG was extracted to be 39 μV/K. The extracted value is lower than reported SiNW value at comparable doping level [64]. However, it can be pointed out that each layer in the experimental setup has its own interfacial thermal resistances which will lower significantly the actual dT across the TEG. As it is a first demonstration, there is a room to improve interfacial thermal resistances and thus improve the dT across the nanowire. Indeed, the idea of an ultrathin thermoelectric device is envisioned to be directly integrated onto chips for direct energy harvesting. In this way, the interfacial thermal resistance associated with the experimental setup can be eliminated. Hence, the effective dT across the SiNW can
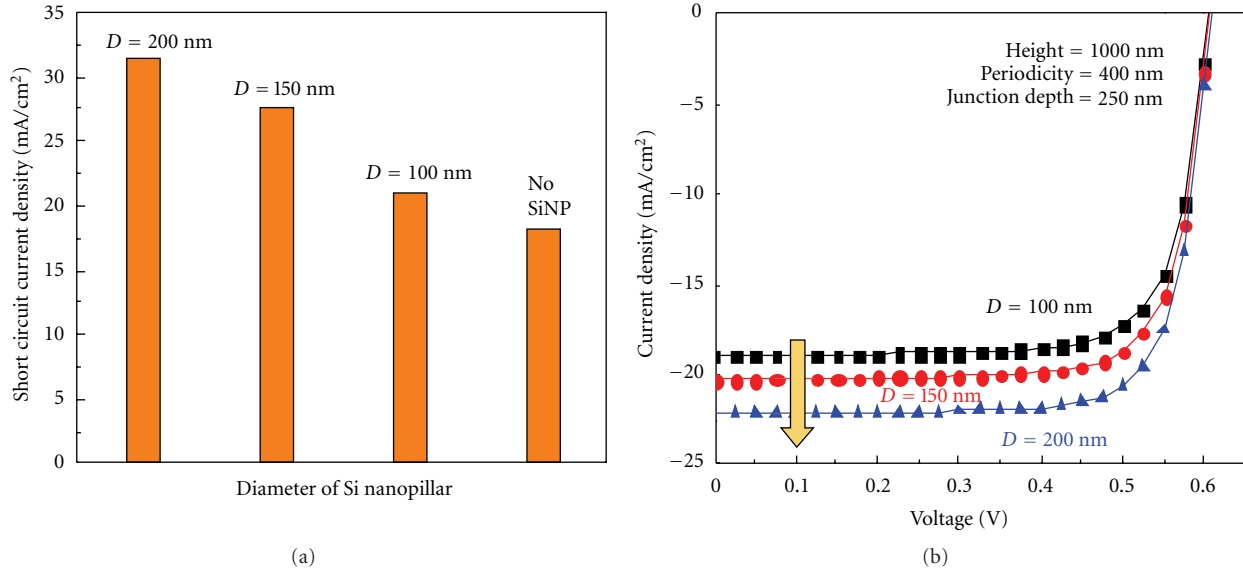
(a)

(b)

FIGURE 22: (a) Measured J_{sc} as a function of Si nanopillar diameter under AM 1.5 G 100 mWcm^{-2} illumination (b) Simulated J-V characteristic of Si nanopillar thin film solar cell (with underlying Si thin film of ~800 nm). (Reprinted with permission from [8]. [2010] IEEE.)

be increased. In Figure 25(b), the generated voltage/power is plotted as a function of current at a total dT of 70 K across the experimental setup. A maximum power output of 1.5 nW is realized under a voltage and current of 0.75 mV and 2 μA, respectively. In our device, if we could extend the dT across the wire to 1 K, a power density of 1.2 μW/cm^2 can be harvested. However, the ability to maintain a large dT across the SiNW to generate a larger power is another important aspect that needs to be considered and optimized.

In brief, SiNW TEG was fabricated using CMOS compatible top-down processes. Seebeck effect was demonstrated and power generation was measured. With further improvements in top metallization and low thermal conductivity material filling between nanowires, such as polyimide, excellent nanoscale thermoelectric energy harvesters can be realized. Such SiNW TEG can be cost-effective, scalable and possibly easier to be integrated. By potential integration of these TEG beneath (wafer backside) traditional high heat flux circuitry, these nanoscaled generators can provide location specific thermal harvesting and pave way to ultra low powered IC's and self-powered circuits.

4. Challenges and Opportunities

There has been significant progress in fabrication technology and in understanding of the electrostatics and transport in the GAA nanowire devices; huge challenges remain to be met before this new device architecture reaches the level of manufacturing. The first challenge is large device parameter variability in the threshold voltage and I_{on} as reported in [10]. This variability is mainly attributed to possible variation of nanowire shape, size/diameter, roughness and variation in interface quality. Tight control of the starting pillar dimensions with advanced lithography and surface

smoothing using H_2 annealing [71] may help in reducing this variation. Indeed, being controlled from all sides the sensitivity of device parameters to nanowire diameter, which is defined by lithography and generally has ±5% variation, is large. Poor lithographic process window for pillar pattern is one the main contribution of critical dimension variation across the wafer. However, one of the solutions for this problem is the change of pattern polarity using hard mask scheme. Use of variability-specific designs, such as eight transistor SRAM [72] or probabilistic circuit design techniques, such as neuromorphic designs [73], could form part of the solution for successful implementation of GAA nanowire devices into manufacturable circuits.

The second challenge pertains to the tuning of the threshold voltage. Due to very limited volume of channel body, the doping of the channel for V_{th} adjustment is not feasible. Due to cylindrical architecture, the impact of gate oxide thickness on V_{th} is also expected to be significantly diminished. The feasible solutions lie only with the tuning of the gate electrode work function and the wire diameters.

The third challenge, specific to vertical nanowire devices, is inherent asymmetry between source and drain resistance, and also in channel diameter if profile is not controlled well. These asymmetries have to be taken care of in circuit designs and therefore provide an opportunity to designers to come up with novel design solutions. Further, the vertical wire is shown as natural platform for TFET; the challenge with circuit design which could be huge as TFET will not work as pass transistor in both directions. Designing hybrid circuits with MOSFETS and TFETS could be one of the solutions to resolve this issue.

The issues which are a challenge in electronics domain have either little or no impact on energy harvesting or could even be favorable. For example, critical dimension
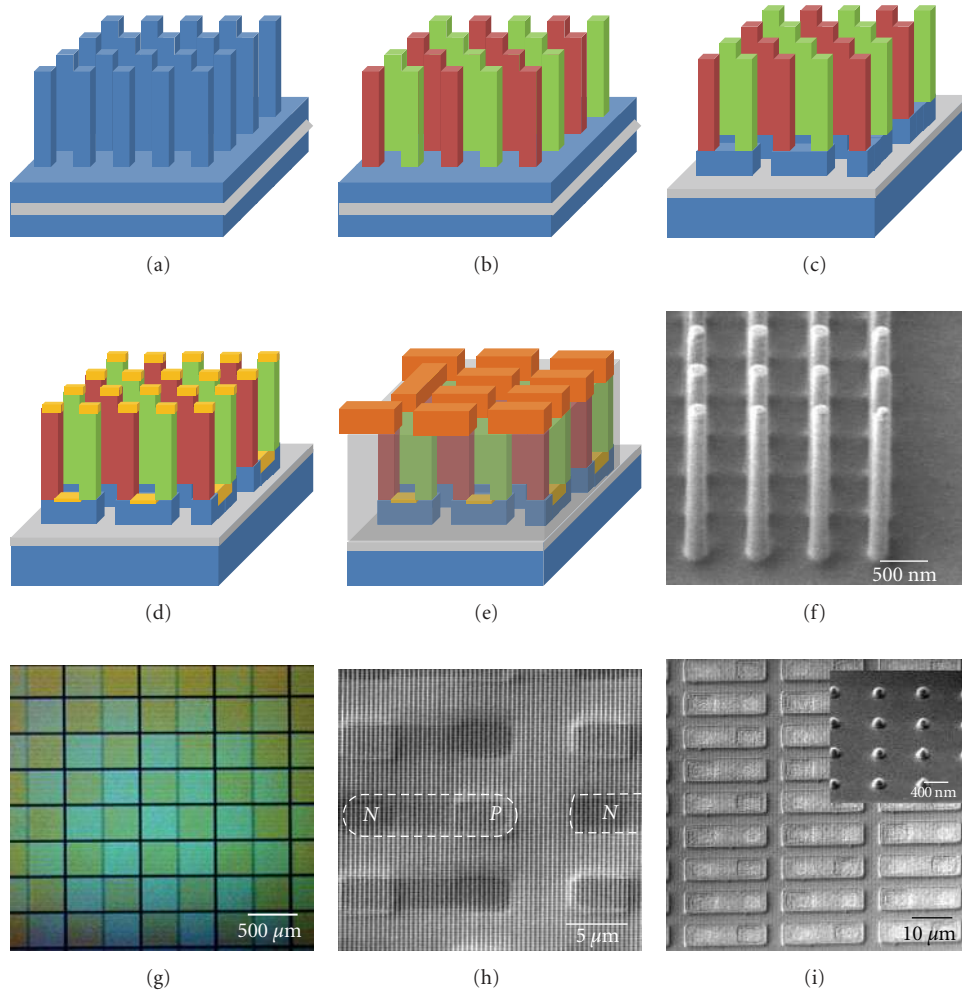
FIGURE 23: Schematic of fabrication (a) SiNW formation by dry etch, (b) Ion implantation, P/N elements definition, each element consists of hundreds of SiNW, (c) P/N couples formed by dry etch, (d) SiNW top and bottom silicidation while protecting the sidewall, (e) dielectric deposition and etch back to expose only the tip of the SiNW, and Top metallization. (f) SEM images of pillar formation, (g) N & P implants can be seen clearly under microscope with a different shade, (h) SEM image of SiNW after N/P implant, and (i) metallization etch showing individual N/P couples. Inset shows the tips of the SiNW exposing after oxide etch which confirms structure of the TEG. (h) and (i) are images of test structures, the actual design is too large to be shown in SEM image. (Reprinted with permission from [70]. [2011] IEEE.)

variation should not impact on solar efficiency, and thermoelectric power generation is expected to improve with surface roughness as a result of decreased thermal conductivity [64, 65]. Though not reviewed in this paper, the use of nanowires in Li ion batteries as anode is another high potential application where none of the issues described above will have any impact [9]. Nanowires also provide opportunity of cointegrating various types of devices either from functionality or performance perspective or for the both on silicon platform. For example, Si/III-V and Ge wires co-integration can provide high performance electronics with NMOS on Si/III-V and PMOS on Ge wire. Worth mentioning here that such hetero-integration may be limited to bottom up technologies as top down would require wafer level selective epitaxial deposition of these materials on silicon which has been a challenge for long due to lattice missmatch.

5. Summary

The status of vertical GAA nanowire technology platform developed using top-down approach has been reviewed. Area, speed, and power advantages of vertical platform for green CMOS based electronics are discussed. In addition to excellent MOSFET scaling potential, the vertical wire is projected as a natural platform for TFET devices demonstrating record low subthreshold slope. Progress on nonvolatile memory cells is reviewed and junction-less wire memory is projected as an excellent platform for 3D stacking. Nanowires seem to have possible novel solutions in low cost solar and thermal energy harvesting. The presented top-down techniques can potentially address the needs of "end-of-the-Silicon technology-roadmap" and beyond CMOS era, possibly can lead to an all nanowire autonomous system where data computation, data storage, energy harvesting,
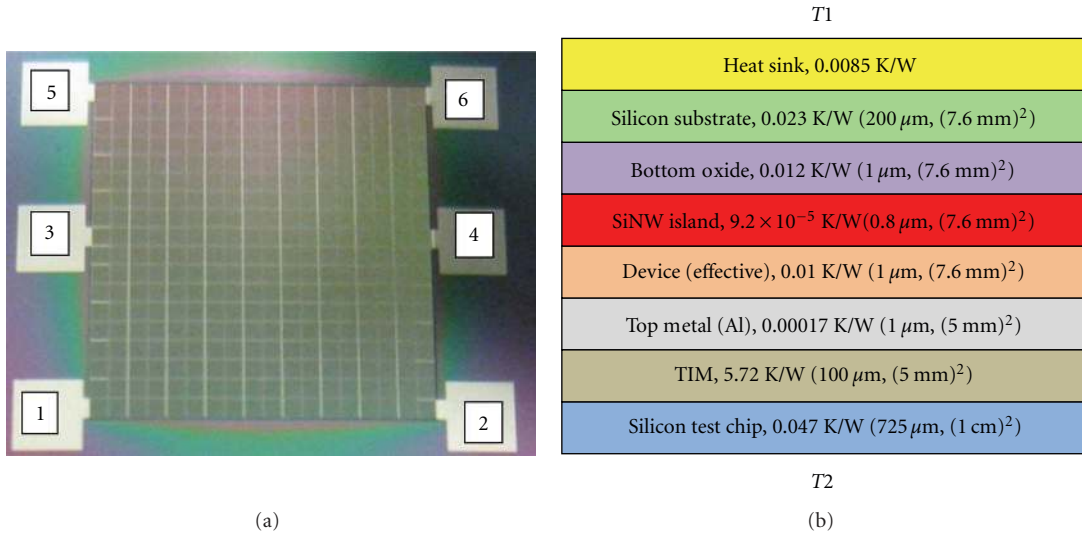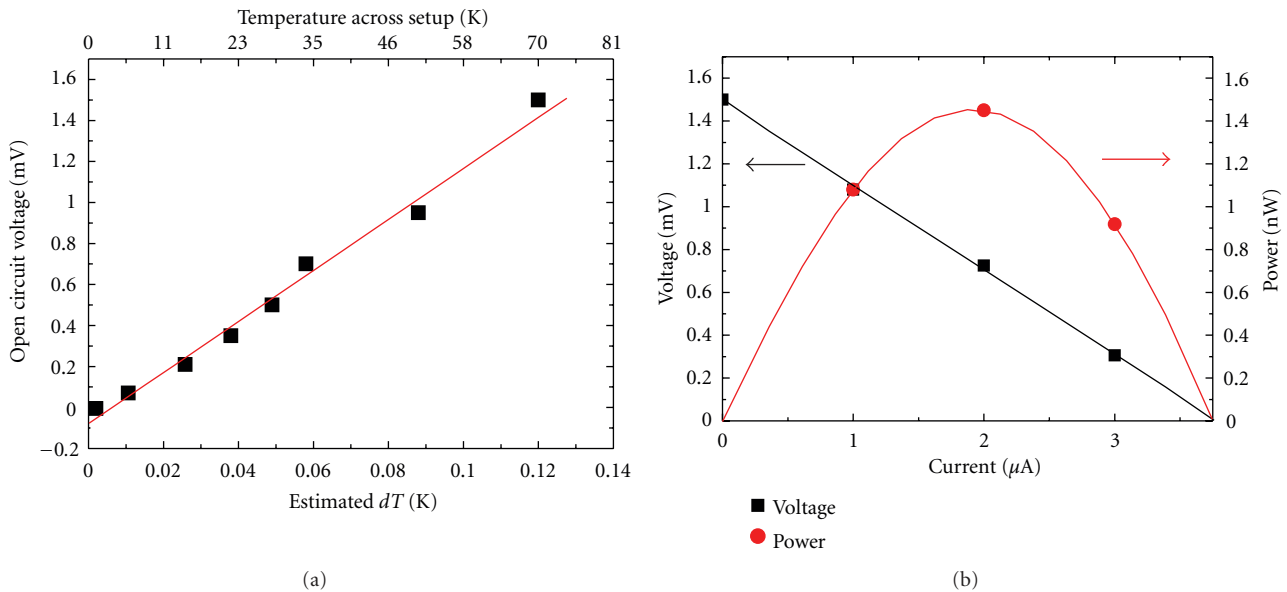
FIGURE 25: (a) Plot of the TEG's V_{oc} versus the different dT (actual/estimated) applied across it. A best fit line is drawn through all the data points. (b) Voltage/Power versus Current curve when dT (estimated) is 0.12 K with V_{oc} and I_{sc} of 1.5 mV and 3.79 µA, respectively. The black line is a linear fit and the red line a polynomial fit of the data points. (Reprinted with permission from [70]. [2011] IEEE.)

and energy storage could all be possible by using nanowire devices, all integrated on chip either at same level or different, using TSV if not direct. Thus, nanowire technology indicates feasibility of opening up newer application opportunities for Si technology.

Acknowledgment

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