Very Wide Range Frequency Synthesizer Architecture for Avionic SDR Applications

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***Abstract*—This paper presents a very wide range frequency synthesizer architecture appropriate to avionic software defined radio (*SDR*) applications. The synthesizer generates a continuous carrier frequencies range between 187 MHz and 12 GHz that covers most of avionic communication applications. The covered range is distributed into twenty sub-bands by using a voltage controlled oscillator (VCO). The considered VCO is able to achieve a tuning range from 10 GHz to 12 GHz (18.2%) and from 7 GHz to 8.5 GHz (19.35%). It includes a capacitor bank, varactors, and switched inductors and is designed in 0.13 μm CMOS technology. Using the advanced design system (ADS) simulation tool and SpectreRF simulator, the proposed VCO exhibits a phase noise of -125 dBc/Hz at 12 GHz and at a 10 MHz offset frequency with a power consumption of 4.1 mW. At 10 GHz, the simulated synthesizer phase noise is of -102 dBc/Hz at a 1 MHz frequency offset. In addition, the loop bandwidth of the phase locked loop (PLL) is 1.1 MHz whereas the settling time is 3.64 μs.**

I. Introduction

The benefits, defined by higher flexibility, lower implementation area, lower cost and lower power consumption of software defined radio (SDR) technology gave rise to a promising approach for future wireless communication systems. SDR technology presents also a suitable solution for integrating and improving the implementation of avionic communication systems. Engineers and system architects need to improve this implementation by minimizing the hardware congestion in aircraft in order to reduce cost and lower energy requirements. The requirements of avionic radio systems such as Distance Measuring Equipment (DME), Mode S transponder, Traffic collision avoidance system (TCAS) and Global Positioning System (GPS) require the implementation of several standards. Moreover, other standards, such as WiMAX and wireless cellular systems, need to be implemented in order to ensure better communication services and more wireless access applications. SDR systems can be used to fully integrate navigation radio systems, communication systems, automatic position reporting system and data links into a single reconfigurable module.

However, avionic communication systems operate under different frequency bands. The allocated spectrum for aeronautical services used by civilian aircraft is presented in Fig. 1. This shows that the center frequencies of most of avionic modules are included in a large frequency band between 100 MHz and 12 GHz (X-band). Hence, the RF front-ends used in an SDR need to be agile enough to meet frequency specifications of each system. A challenging task is to meet

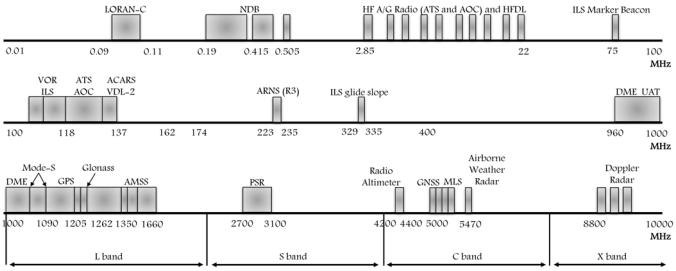

Fig. 1: Allocations spectrum for aeronautical services [1].

the specifications of the local oscillators (LO) which need to cover wide frequency ranges as well as provide high accuracy and good phase noise performance.

Approaches for adding agility to frequency synthesizers have been proposed for several applications in different technologies. Indeed, an agile frequency synthesizer can be provided by using a single voltage controlled oscillator (VCO). The architecture presented in [2] generates a frequency range between 3 GHz and 10 GHz by using four polyphase filters and three single sideband (SSB) mixers. The synthesizer proposed in [3] is able to provide carrier frequencies distributed between 3.4 GHz and 7.9 GHz with two mixers. Moreover, the frequency synthesizer presented in [4] ensures a continuous frequency band between 1.8 GHz and 6 GHz by using wide tuning range VCO and one SSB mixer. Other proposed systems use a single VCO with switching capacitor bank [5], [6]. This idea allows the extension of the frequency band while keeping low VCO gain. The synthesizer presented in [5] is able to generate the frequency band 9.2 GHz$-$12.7 GHz whereas the architecture shown in [6] provides a wide continuous frequency band between 50 MHz and 6 GHz.

A wide frequency band can also be provided by employing multiple VCOs. Using this approach, the synthesizer presented in [7] generates a frequency band of 0.4 GHz$-$6 GHz by using a dual VCO architecture. The same approach has been used in [8] to generate a frequency band from 1 GHz to 10 GHz spread into thirteen sub-bands. Moreover, twelve bands are provided in [9] between 375 MHz to 6 GHz with a single SSB mixer. For higher frequencies, such as the Ka-band, the designers may use multipliers to reach the desired frequency band. This solution is proposed by [10] with a frequency synthesizer able to generate a frequency band of 21 GHz$-$48 GHz.

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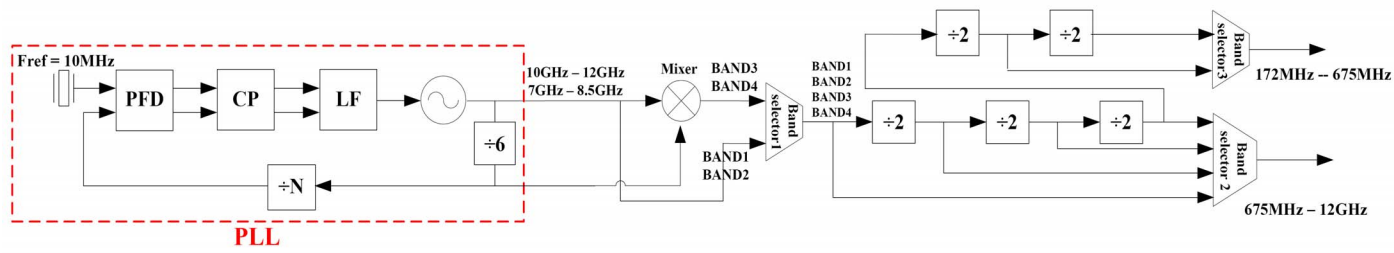

Fig. 2: Block diagram of the frequency synthesizer architecture.

By comparing the previously mentioned approaches, we can see that each architecture exhibits advantages and disadvantages. The evaluation of different synthesizer architectures leads to believe that a frequency synthesizer implemented with one SSB mixer and only a single VCO equipped by a switching inductor and a switching capacitor bank may represent a good trade-off between low power consumption, reduced complexity, and small area, while providing the widest frequency range possible.

Accordingly, the architecture proposed in this paper describes a novel frequency synthesizer architecture for avionic SDR applications that is able to cover a continuous frequency range from 187 MHz to 12 GHz. The synthesizer consists of a single wide tuning range VCO controlled with a switching capacitor bank that is included within a phase-locked loop (PLL) and one SSB mixer. Recently, CMOS technology [2], [5] has enabled high degree of integration with good energy efficiency that has enhanced hardware performance. Therefore, 0.13 μm CMOS technology will be leveraged in this work.

The rest of the paper is organized as follows. The architecture of the frequency synthesizer is outlined in Section II, followed in Section III by a description of the system components and the core VCO. Simulation results are then presented and commented in Section IV, showing the performance of the proposed architecture, and are followed by the conclusion.

II. Frequency Synthesizer Architecture

The block diagram of the synthesizer architecture is shown in Fig. 2. It consists of a PLL with a single switched inductor and capacitor bank VCO, a SSB mixer, a charge pump (CP), a phase-frequency detector (PFD), band selectors and frequency dividers.

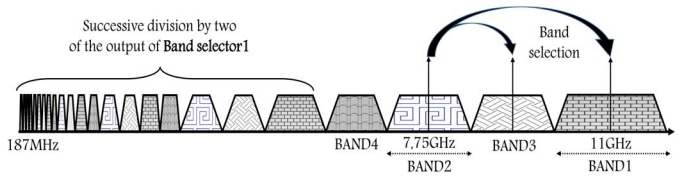

Fig. 3: Conceptual plot of the different frequency allocations.

The VCO provides two frequency bands using the switched inductor: BAND1 from 10 GHz to 12 GHz and BAND2 from 7 GHz to 8.5 GHz .The center frequencies are f_{VCO1}=11 GHz and f_{VCO2}=7.75 GHz respectively. By dividing BAND1 by six and mixing (through the SSB mixer) the resulting frequency with the BAND1 itself, the mixer output generates BAND3 ranging between 8.5 GHz and 10 GHz. The same technique is followed to provide BAND4 from 6 GHz to 7 GHz by mixing the result of BAND2 divided by six with BAND2. Therefore, the band selector (1) can ensure a continuous frequency range from 6 GHz to 12 GHz. Furthermore, five frequency bands from 3 GHz to 6 GHz, from 1.5 GHz to 3 GHz, from 750 MHz to 1.5 GHz, from 375 MHz to 750 MHz and from 187 MHz to 375 MHz respectively are obtained by dividing the output of band selector1 by 2, 4, 8, 16 and 32. The architecture frequency allocation is shown in Fig. 3. The considered SSB mixer consists of two 90-degree phase shifters and two double side band mixers as proposed in [11].

III. Architectural Design

A. Phase Locked Loop

The main part of the frequency synthesizer is the PLL presented in Fig. 4. It consists of a frequency reference clock of f_{ref} = 10 MHz, a phase frequency detector with gain of K_d, a charge pump with current I_p where $I_p = K_d.2\pi$, a passive low pass filter with a resistor R and two capacitances, C_1 and C_2, a VCO with gain of K_0, a programmable divide-by-N divider, and a divide by six prescaler. In lock, the PLL provides an output frequency f_{out} such that $f_{out} = 6.N.f_{ref} = N_p.f_{ref}$.

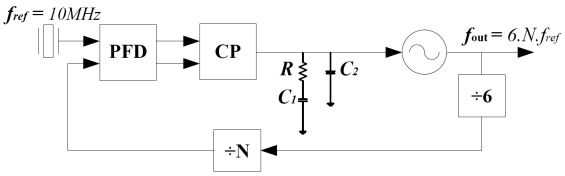

Fig. 4: Phase locked loop block diagram.

The transfer function of the loop filter is given by:

$$F(s) = \frac{1 + RC_1 s}{s(C_1 + C_2)\left(1 + \frac{RC_1C_2}{C_1+C_2}s\right)}, \quad (1)$$

whereas the closed loop transfer function $Y(s)$ can be given by:

$$Y(s) = \frac{\frac{K_0}{s}K_d F(s)}{1 + \frac{K_0}{s}K_d F(s)N_p} = \frac{\omega_n^2\left(1 + \frac{s}{\omega_z}\right)}{s^2 + 2\xi\omega_n s + \omega_n^2}, \quad (2)$$

where ω_n represents the natural frequency, N_p is the division loop factor, ω_z is the stabilizing zero while ξ is the damping factor. Several considerations shall be taken into account when designing the PLL. The wide tuning range requires high VCO gain value. However, the phase noise deteriorates under such condition. For this reason, a trade-off between large VCO tuning range and phase noise performance is always necessary.

Sufficient phase margin is essential for loop stability while achieving high loop bandwidth guarantees short settling time. Therefore, loop filter parameters should be carefully chosen in order to meet the design considerations. For the designed VCO, the R value should be between 5 kΩ and 20 kΩ to ensure sufficient phase margin. Capacitance C_1 is important for loop stability because of its relationship to both the natural frequency and the damping factor. Hence, C_1 can be between 50 pF and 400 pF. Finally, capacitance C_2 should be less than 10% of C_1 in order to preserve the phase margin, and more than 2% of C_1 in order to allow for good spur and jitter performance [12]. All design values are selected and optimized through the advanced design system (ADS) simulation tool.

B. Voltage Controlled Oscillator

Several implementation techniques can be used to design the VCO. For instance, all-PMOS VCOs have better phase noise performance due to the N-wells encompassing the transistors which reduce the impact of substrate noise [13]. However, this approach is limited by a lower tuning range. On the other hand, an all-NMOS VCOs can be more interesting thanks to their larger tuning ranges and smaller footprints compared to that of all-PMOS designs. Therefore, a complementary cross-coupled NMOS and PMOS VCO topology provides a suitable trade-off between tuning range, reduced area and phase noise performance with shorter start-up times than traditional cross-coupled pairs [14]. In addition, the use of a switched capacitor bank and switched inductor improves the phase noise performance by decreasing the VCO gain while maintaining the same covered frequency range.

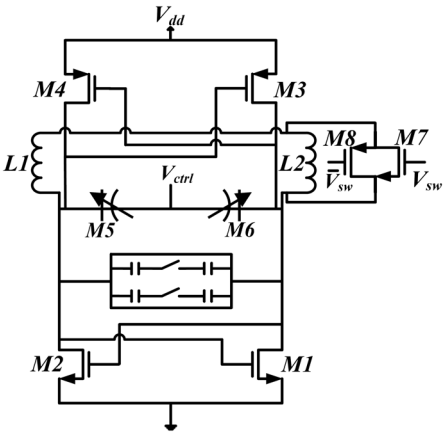

Fig. 5: Schematic of the VCO architecture.

Accordingly, the VCO architecture, presented in Fig. 5, consists of complementary cross-coupled transistors pairs, two NMOS varactors, one transmission gate NMOS/PMOS switch, capacitor bank, and two differentially excited inductors in series, one of which can be shorted. Transistors $M1$-$M4$ form the cross-coupled pairs, while $M5$ and $M6$ are used as MOS varactors. C_{bank} capacitors are controlled by a digital word. Transistors $M7$ and $M8$ represent a transmission gate used, as a switch, to short inductor $L2$. With the switch turned off, the oscillation frequency is given by:

$$f_1 = \frac{1}{2\pi\sqrt{(L_1 + L_2)(C_{var} + C_{bank})}}, \tag{3}$$

where C_{var} is the tank capacitance, including parasitic and varactors capacitances. Conversely, when $M7$ is turned on, $L2$ is shorted, changing the oscillation frequency by offsetting the impact of $L2$ in (1). Furthermore, changing the C_{bank} value allows for additional oscillation frequencies. All transistors used as switches should have the smallest possible length in order to ensure fast switching between modes and low ON-resistance. The VCO layout is presented in Fig. 6.

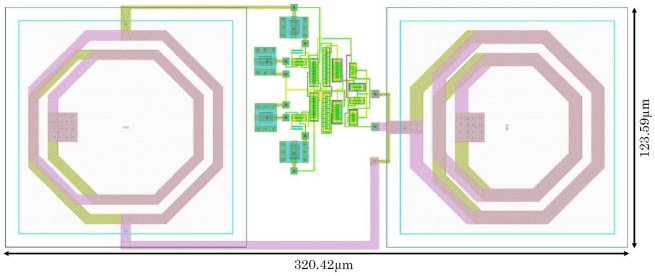

Fig. 6: The VCO layout.

C. Dividers

The synthesizer architecture uses several static dividers: a divide-by-2 and a divide-by-3 that are implemented using current mode logic (CML) approach which can reach a frequency operation of up to 40 GHz [15]. The programmable divide-by-N in the PLL feedback path is based on the pulse swallow architecture as presented in Fig. 7. This divider consists of a 1/2 dual modulus prescaler, a 7-bit program P counter and a 7-bit swallow S counter such that the achieved divider ratio is given by $P + S$.

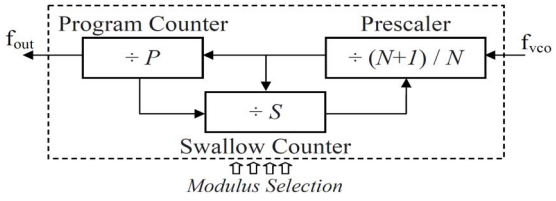

Fig. 7: Block diagram of the programmable pulse-swallow divider.

The prescaler of the pulse-swallow divider is implemented by a divide-by-two that can be selectively bypassed. Thus, this structure is simpler than typical swallow-counter implementations that utilize higher modulus prescalers. To accommodate the full frequency range of the VCO, the programmable divider can be programmed with a ratio from 116 to 200, with $P = 115$ and S bounded between 1 and 85, allowing the support of both integer-N and fractional-N implementations.

D. Band Selectors

The band selectors are implemented with transmission gates. Sufficient isolation must be achieved to avoid signal leakage, especially at higher VCO output frequencies [16].

IV. Simulation Results

The VCO is simulated using the SpectreRF simulator with a 1.2 V supply. System level simulations are carried out in ADS. The VCO output frequency for each setting of the capacitor bank as a function of the varactor control voltage is shown in Fig. 8. As can be seen, the VCO covers two frequency bands that are enabled by shorting inductor L2 or not. When switch $M7 - M8$ is ON, BAND1 is provided through overlapping sub-bands ensured by the capacitor bank while BAND2 is provided when $M7 - M8$ is OFF.

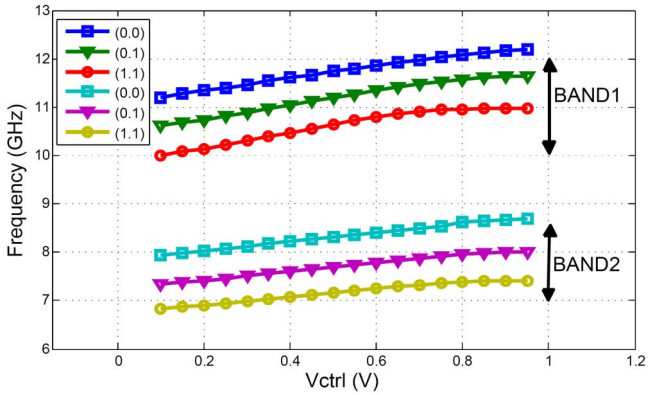

Fig. 8: VCO tuning range for both frequency bands.

The VCO ensures a tuning range of 700 MHz around 11 GHz. At 12 GHz, the free-running VCO phase noise is of -125 dBc/Hz at a 10 MHz offset frequency, whereas the power dissipation is 4.1 mW. The VCO phase noise at a 12 GHz oscillation frequency is shown in Fig. 9.

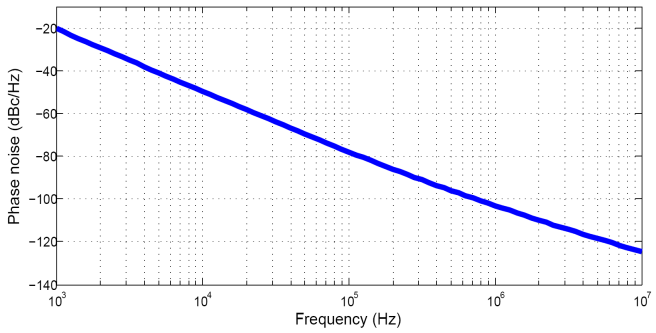

Fig. 9: The VCO phase noise.

The entire synthesizer system is simulated by inserting the VCO gain curves of both frequency bands into the ADS system model. As discussed in Section III, the loop filter components values, VCO gain, K_0, and charge pump current, I_p, have to be designed with stability and loop bandwidth trade-offs in mind. With a reference frequency of 10 MHz, the values of R, C_1 and C_2 were set to 6 kΩ, 356 pF and 30 pF, respectively, whereas the charge pump current was fixed to 2 mA. Furthermore, to provide a synthesizer phase noise estimation, the phase noise performance of both the free-running reference, based on results reported in [17], and VCO, from SpectreRF, are inserted within ADS.

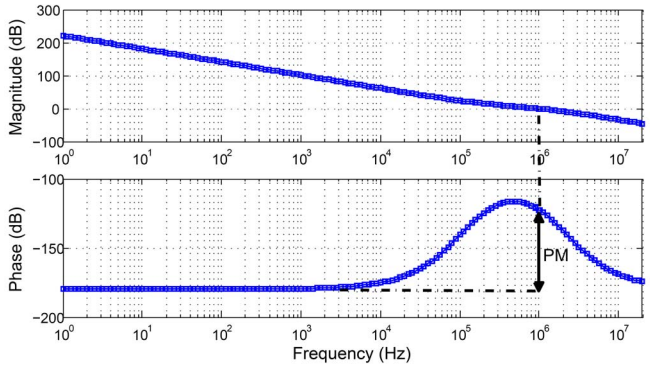

Fig. 10: PLL open-loop frequency response.

The open-loop response of the PLL in BAND1 is obtained by ADS and presented in Fig. 10. The loop provides a bandwidth of 1.1 MHz and a phase margin of around 58 degrees. Both values allow for a short settling time and stable operation.

The simulated phase noise is shown in Fig. 11 for a 11 GHz output frequency. The 1 MHz offset total phase noise is of -102 dBc/Hz. The phase noise of the system is dominated by the reference noise at low frequency offsets, which indicates at a higher reference frequency reference could be used to improve close-in phase noise performance. Conversely, the VCO noise becomes the main dominating factor at high frequency offsets, because of the noise sensitivity of the system due to the large VCO gain. As the control voltage of the VCO is limited to 1.2 V, the high VCO gain is necessary in order to ensure a sufficient tuning range. This ultimately limits the system's achievable phase noise performance.

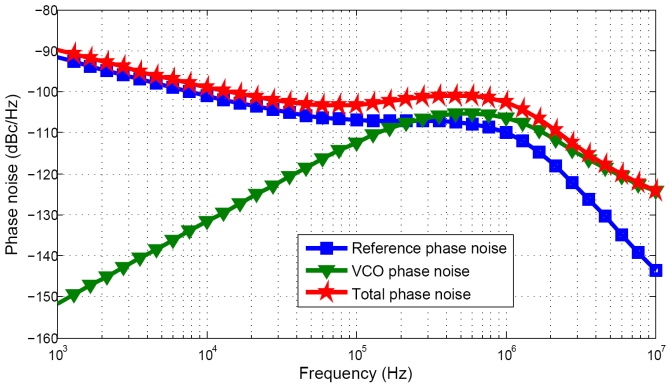

Fig. 11: PLL output phase noise plot for the different noise contributors with the total resulting phase noise.

Typical simulated transient PLL behavior is illustrated in Fig. 12, where the response to the start-up and a 2 GHz frequency jump is shown. After system start-up, the frequency

TABLE I: Comparison of frequency synthesizers

Characteristics	This work	[5]	[6]	[7]	[9]
Technology	0.13μm	28nm	0.13μm	0.13μm	0.13μm
Reference frequency (MHz)	10	40	18.75 - 37.5	40	25
Center frequency (GHz)	7.75 - 11	3	10	4.9	3.5 - 6
Output range (GHz)	0.172∼12	9.2∼12.7	0.05∼6	0.4∼6	0.375∼6
Frequency synthesis scheme	Single VCO+Div/Mux	Single VCO+Div	Cap-bank-VCO+Div	Two VCOs+Div/Mux	Dual VCO+Div/Mux
Number of mixers	1	0	0	1	1
Loop bandwidth (MHz)	1.1	1.8	-	0.1	0.89
Figure-of-merit (FoM)	225	240	229	182	233
Phase Noise (at 1 MHz)	−102(at 11 GHz)	−104(at 10 GHz)	−110(at 5.1 GHz)	−114(at 5 GHz)	−110.8(at 5.5 GHz)

shift settling time is of 3.65 μs for the selected frequency jump.

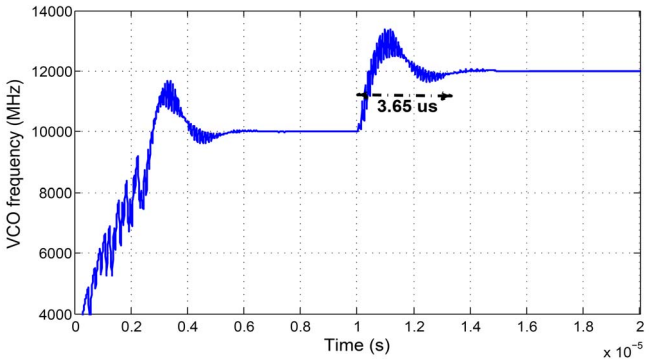

Fig. 12: Typical PLL transient response.

The performance of the proposed architecture is summarised in table I and is compared with other wide frequency range synthesizers previously presented in the literature (for instance, [5], [6], [7] and [9]). The architecture presented in this work provides the widest continuous frequency band with a single SSB mixer and only one VCO, while achieving good phase noise performance.

V. Conclusion

In this paper, a synthesizer for avionic SDR applications that provides continuous frequencies from 187 MHz to 12 GHz was presented. The proposed frequency synthesizer makes use of one SSB mixer, a single switched capacitor bank and switched inductor VCO. Using ADS-based simulations, the PLL core achieves a loop bandwidth of 1.1 MHz with a phase margin of 58 degrees. At a 11 GHz output frequency, the total phase noise exhibited is -102 dBc/Hz at a 1 MHz offset frequency. Ancillary elements of the architecture are currently being implemented in order to send out the chip for fabrication.

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