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VHDL Design of FPGA Arithmetic Processor

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Abstract - This paper involves the design and development of a single chip VHDL FPGA processor which performs all arithmetic and logical functions and the output is displayed by means of LCD interface. This processor can perform 2n number of operations, where n is the number of control bits. In this design, a 5 bit control input is used so that the processor is capable of performing up to 32 operations. The chip is designed to execute 21 operations for different specified functions and 11 more operations can be worked on for improvements and future works. Two data with a size of 8 to 16 bits can be applied as input and the results are obtained on 4 to 8 hexadecimal digits carrying 32 bits in all. A status flag is also designed with the features such as indication of overflow, carry, borrow and zero value. To implement the above design, Very High Speed Description Language simulation is required which can be performed using Altera or Xilinx softwares. Once the program has been developed, the authors demonstrate the feasibility of the proposed design by incorporating it into a FPGA chip and the required hardware can be brought into effect. The state of each output bit is shown by using Light Emitting Diodes. Based on users needs, more features can be added to the designed hardware without hindering the implemented one.

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VHDL Design of FPGA Arithmetic Processor

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Abstract - This paper involves the design and development of a single chip VHDL FPGA processor which performs all arithmetic and logical functions and the output is displayed by means of LCD interface. This processor can perform 2n number of operations, where n is the number of control bits. In this design, a 5 bit control input is used so that the processor is capable of performing up to 32 operations. The chip is designed to execute 21 operations for different specified functions and 11 more operations can be worked on for improvements and future works. Two data with a size of 8 to 16 bits can be applied as input and the results are obtained on 4 to 8 hexadecimal digits carrying 32 bits in all. A status flag is also designed with the features such as indication of overflow, carry, borrow and zero value. To implement the above design, Very High Speed Description Language simulation is required which can be performed using Altera or Xilinx softwares. Once the program has been developed, the authors demonstrate the feasibility of the proposed design by incorporating it into a FPGA chip and the required hardware can be brought into effect. The state of each output bit is shown by using Light Emitting Diodes. Based on users needs, more features can be added to the designed hardware without hindering the implemented one.

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I. Introduction

This paper deals with the design methodology of a FPGA Arithmetic Processor using VHDL to enhance the description, simulation and hardware realization. The design and implementation of FPGA based Arithmetic Logic Unit is of core significance in digital technologies as it is being an integral part of all microprocessors. As the name suggests, this is a system which is capable of performing not only arithmetic operations but also computes logic functions and provides the output through gating circuitry. All the modules described in the design are coded using VHDL which is a very useful tool with its degree of concurrency to cope with the parallelism of digital hardware. The top-level module connects all the stages into a higher level. Once identifying the individual approaches for input, output and other modules, the VHDL descriptions are run through a VHDL simulator, followed by the timing diagrams for the verification, working and performance of the above design along with the hardware implementation that shows the appropriateness of the design.

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II. Rationale

An early design involved in the computations of arithmetic and logical operations were complex and found to be time consuming. The circuitry needed to develop such an ALU of required specifications by conventional approach will lead to thousands of gates, transistors, resistors, capacitors, inductors and other digital components. The implementation of such a system raises major questions in the shape of its integration and optimization. These problems have been eliminated in this project by the use of Field Programmable Gate Array (FPGA) technology and by Hardware Descriptive Language (HDL). Since the feeding units are of binary nature and output of Hexadecimal, the complex and time consuming computations in the earlier methods are eliminated. The software interface along with the advanced options like graphical blocks, chip design and planner reduces the complexity and increases the ease of computations.

III. Technical Work Preparation

The organization and designing of this process is put forth by various tools. These tools and methods are significant in differentiating a successful one with the one carrying loop holes and discrepancies. In the present case, ALU is bricked up using synthesized operations in the form of objectives and broader aspects. The organization chart for the paper design that is needed to implement is shown in Fig. 1.

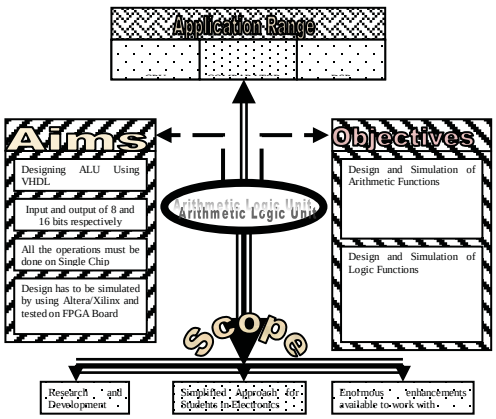

Fig.1 : Organization chart of the paper design with aims and objectives.

a) System Overview

This paper design has been embodied by many separate sub-systems. Amongst them operational design, Software design and Hardware design are of central emphasis.

b) Operational overview

The operational overview deals with two kinds of operations which an ALU can perform. First part deals with arithmetic computations and is referred to as Arithmetic Unit. It is capable of addition, subtraction, multiplication, division, increment and decrement. The second part deals with the Gated results in the shape of AND, OR, XOR, inverter, rotate, left shift and right shift, which is referred to as Logic Unit. The functions are controlled and executed by selecting operation or control bits. A select input of 5 bit size that will accommodate up to 32 operations is sufficient to achieve the objectives. The operations selected by the Control Unit are shown in the Fig. 2. Arithmetic part is quite complex as compared to logic unit and involves an additional carry input. Multiplication and Division also increases the complexity of ALU. In the Logic Block, gates such as AND, OR, XOR and NOT operations are shown. Logic Block of ALU does not need as many gates as required in Arithmetic Unit and if done separately, the LOGIC unit can be implemented using Complex Programmable Logic Devices (CPLD) or other Programmable Logic Device (PLD) technologies instead of using FPGA.

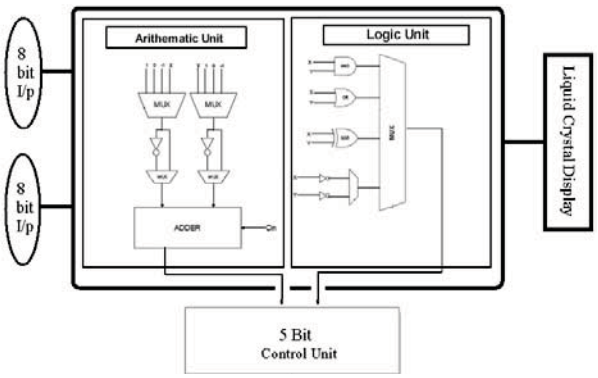

Fig.2 : General operation – ALU sub-blocks and control units using multiplexers

c) Software Overview

This paper capitalizes on the digital phenomenon; therefore software design draws most of the attention. The VHDL software interface used in this design reduces the complexity and also provides a graphic presentation of the system. The key advantage of VHDL when used for systems design is that it allows the behavior of the required system to be described (modeled) and verified (simulated) before synthesis tools translate the design into real hardware (gates and wires). This software not only compiles the given VHDL code but also produces waveform results. Graphical blocks, chip design and planner are the advanced options available and are used in the software mentioned. Altera's Quartus II and Xilinx webpack are few of the sophisticated Computer Aided Design (CAD) tools to perform the compilation and simulation of any logic circuit design.

d) Hardware Overview

The fundamental building block of ALU is shown in Fig. 3. Here bold dots (dip switches) indicate the inputs to an ALU which are selected by the user. The input can either be 1 or 0 indicating 5V and 0 V respectively. A LCD is used to display 16 bit output, whereas * indicates LEDs which are used to show the status of carry out, overflow, borrow and zero. The VHDL code which implies the hardware part of ALU is downloaded on FPGA processor using JTAG cable interfacing PC and the hardware element.

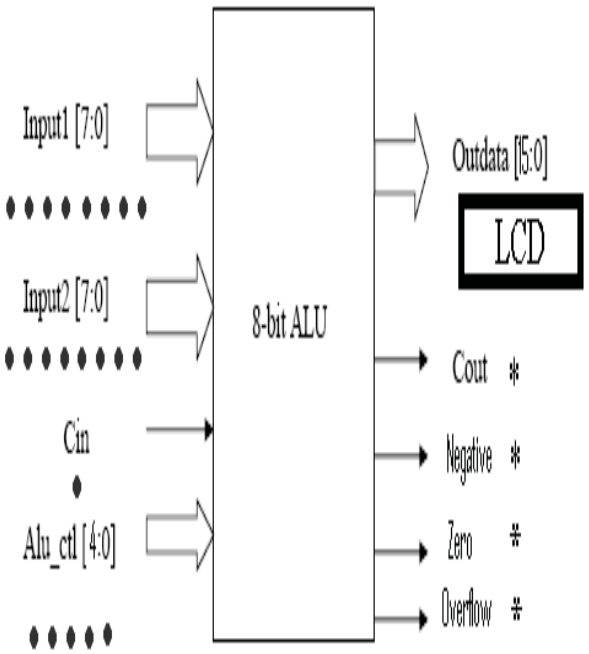

Fig.3 : Hardware representation of an 8-bit ALU.

A final point is that when a VHDL model is translated into the "gates and wires" that are mapped onto a programmable logic device such as a CPLD or FPGA, and then it is the actual hardware being configured, rather than the VHDL code being "executed" as if on some form of a processor chip.

IV. Methodology

Strategizing methods are designed by using part by part approach also known as "Divide and Conquer" or "Bit Slice". This approach provides a convenient method of operation and hence smaller blocks can be easily managed with ease as compared to the larger units.

a) *Graphical Splitting*

In this method, an ALU is chopped into several segments each incorporating its specific operations. A model of this technique containing Arithmetic, Logic, Multiplexer and Shift and Rotate Units are shown in Fig.4.

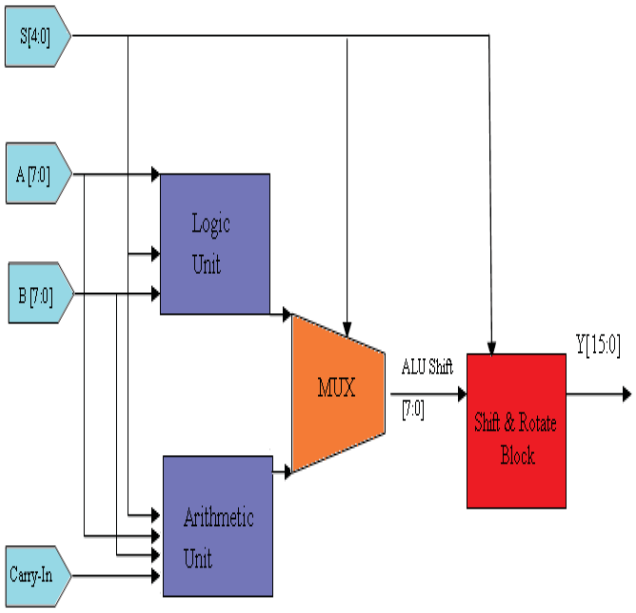

Fig.4 : Block diagram of 8-bit ALU.

b) Truth Table Design

Truth table design is an effective method compiling all those functions that are needed by the user on a single platform. Table 1 indicates the combination of five bit control input S[4 down to 0] with their operation and functions that are used in ALU. Arithmetic, Logic and Shifter units are separated in the table.

Table 1 : Combination of five bit control input S [4 down to 0] with their operation and functions that are used in ALU.

S4	S3	S2	S1	S0	Operation	Function	Implementation
0	0	0	0	0	Y<=a+b	Addition	Arithmetic Unit
0	0	0	0	1	Y<=a+ 2's C of b	Subtraction a-b	Arithmetic Unit
0	0	0	1	0	Y<=b+2's C of a	Subtraction b-a	Arithmetic Unit
0	0	0	1	1	Y<=a+1	Increment a	Arithmetic Unit
0	0	1	0	0	Y<=a-1	Decrement a	Arithmetic Unit
0	0	1	0	1	Y<=b+1	Increment b	Arithmetic Unit
0	0	1	1	0	Y<=b-1	Decrement b	Arithmetic Unit
0	0	1	1	1	Y<=a*b	Multiplication	Arithmetic Unit
0	1	0	0	0	Y<=a/b	Division a by b	Arithmetic Unit
0	1	0	0	1	Y<=b/a	Division b by a	Arithmetic Unit
0	1	0	1	0	Y<=a comp	Complement a	Logic Unit
0	1	0	1	1	Y<=b comp	Complement b	Logic Unit
0	1	1	0	0	Y<=a AND b	AND	Logic Unit
0	1	1	0	1	Y<=a OR b	OR	Logic Unit
0	1	1	1	0	Y<=a XOR b	XOR	Logic Unit
0	1	1	1	1	Y<=shl a	Shift left a	Shifter Unit
1	0	0	0	0	Y<=shl b	Shift left b	Shifter Unit
1	0	0	0	1	Y<=shr a	Shift right a	Shifter Unit
1	0	0	1	0	Y<=shr b	Shift right b	Shifter Unit
1	0	0	1	1	Y<=RAL a	Rotate left a	Rotate Unit
1	0	1	0	0	Y<=RAR a	Rotate right a	Rotate Unit

V. Implementation

The VHDL coding of this paper design is compiled and simulated using Altera Quartus-II and has been downloaded in FPGA using Xilinx Spartan XC3S100E kit shown in Fig. 5. The data is updated to the kit using two separate select inputs A and B each carrying 8 bits. The function of FPGA is embedded on the kit along with PROM, LCD, LEDs and DIP switches. A Joint Test Action Group (JTAG) interface connects the FPGA chip with PROM and leads to PC through a serial interface. The structure of such a PROM assembly XC10S is shown in Fig. 6. Since FPGA is user programmable, therefore JTAG is of core significance. PROM has several postulates in the shape of data storage and debugging, permanent storage of data, consistency of operation, low cost, high speed and compactness. PROM used in this design of ALU is "XC10S", which is equipped with the inbuilt circuitry to support and store complex functions. It supports both mode of Master and Slave serial Field Programmable Gate Array.

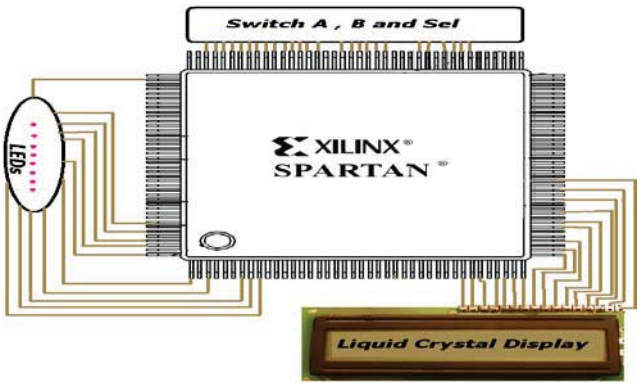

Fig.5 : Circuit design of FPGA kit.

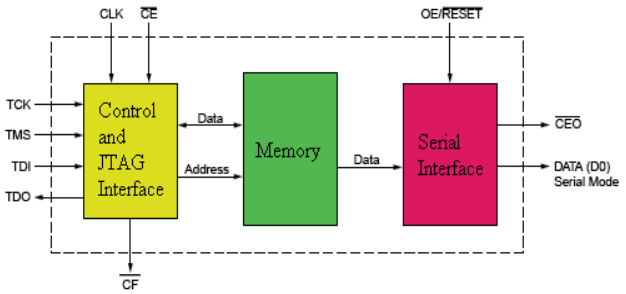

Fig.6 : Structure of XC10S PROM.

In real time application, after the process of compilation and simulation of the VHDL design, the hardware realization is constructed and tested as shown in Fig. 7. Here the 8-bit inputs are given by means of two sets of DIP switches and the 16-bit output can be displayed on a LCD panel and the result can be verified with the simulated output. The status of the flag register is indicated by a series of 8-bit LEDs. The provision of a select switch used in this hardware enables the user to perform the required operation on the FPGA processor.

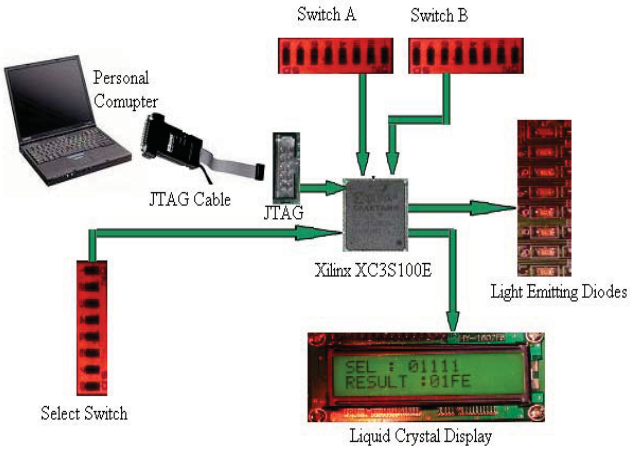

Fig.7 : Real time hardware implementation.

V. Achieved Results

This paper requires the building and simulation of the VHDL coding using Xilinx or Altera program. Once the program has been developed, it will be burnt on to a FPGA chip with which the required hardware is obtained. Designing and Testing of ALU is achieved by differentiating the system into four blocks, first deals with Arithmetic Aspects while second is concerned with Logical Unit, similarly third and fourth blocks are for Shifter and Rotate Operations respectively. Simulated output of a sample multiplication operation is shown in Fig. 8.

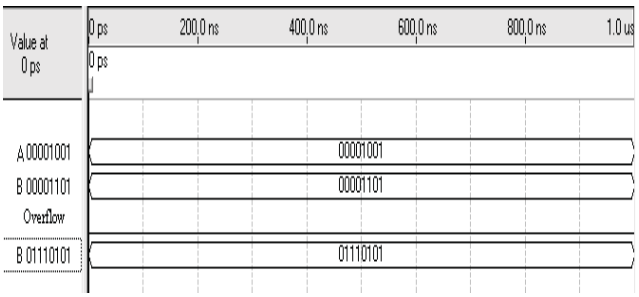

Fig.8 : Simulated output of 8-bit multiplication operation.

VI. Conclusion

In this project, Arithmetic Logic Unit was successfully designed and implemented using Very High Speed Hardware Descriptive Language and Xilinx Spatan-3E Field Programmable Gate Array. All the primary operations of Arithmetic Logic Unit are fabulously done alongside some extra features that provide status of output. Graphical Splitting and Truth Table formation provided a synthesizable system design by separating Arithmetic, Logic, Shifter and Rotator blocks which were integrated in later stages. Design methods involved follows a TOP-DOWN approach in which software design leads the physical and hardware construction. Software section has been realized using Behavioral Model of VHDL. The programming is done

for 8 bit lanes of 2 inputs each but system can accommodate up to 6 input channels. The 5 bit control unit holds responsibility for shaping the output of specified operation. Further enhancements can be made on this system by adding more number of inputs with increased number of bit size. Digital Signal Processing (DSP) is being credited with lots of applications from VHDL designs. Advancement in floating point applications of ALU can mutually benefit the two fields.

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