Vibration-to-Electric Energy Conversion

Scott Meninger, Jose Oscar Mur-Miranda, Rajeevan Amirtharajah
Anantha Chandrakasan and Jeffrey Lang
Massachusetts Institute of Technology, Cambridge, MA 02139

Abstract— **A system is proposed to convert ambient mechanical vibration into electrical energy for use in powering autonomous low-power electronic systems. The energy is transduced through the use of a variable capacitor, which has been designed with MEMS (microelectromechanical systems) technology. A low-power controller IC has been fabricated in a 0.6μm CMOS process and has been tested and measured for losses. Based on the tests, the system is expected to produce 8μW of usable power.**

Keywords— **Energy Conversion, MEMS, Low-Power, Self-Powered**

I. Introduction

The trend in modern VLSI design towards low-power DSP and remote sensing applications creates an opportunity for the exploitation of novel energy sources. The extremely low duty cycle of such systems pushes power requirements of a source into the μW range [1], [2], [3]. Self-powered systems based on harvesting ambient energy become viable alternatives, eliminating the need for batteries and creating low-maintenance, autonomous systems. Several different ambient sources have already been exploited. These include solar, electromagnetic, RF [4], and mechanical vibration [5], [6], [7] sources. With advances in MEMS technology, it is possible to implement a self-powered system with the MEMS device acting as an electromechanical transducer in the form of a variable capacitor, provided that energy conversion is governed by a low-power digital controller. This paper presents the design of such a system, with emphasis on the controller IC.

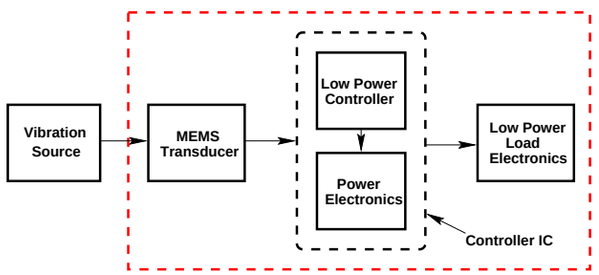

Fig. 1. System Block Diagram

II. Energy Conversion

The method proposed to convert ambient mechanical vibration into electrical energy is to use a MEMS variable capacitor. By placing charge on the capacitor plates and then moving the plates apart, mechanical energy can be converted into electrical energy which can then be stored and utilized by a load. The system is depicted in Figure 1. The mechanical system is modeled as a vibration source which couples into the electrical system through the MEMS transducer. A low power controller directs energy conversion and supplies power to the load. The controller consists of a power electronics subsystem which is responsible for exciting the transducer through its energy conversion cycle, and has been optimized to minimize losses, and a digital control core which generates the timing pulses which drive the gates of the power FETS in the power electronics subsystem.

Two common energy conversion cycles for the MEMS transducer as shown in Figure 2. Path A-B-D-A depicts charge-constrained conversion, while path A-C-D-A depicts voltage-constrained conversion. One basic constraint for both cycles is that there is some maximum allowable voltage, V_{max}, which is set by some process or system requirement. For example, the power switches which are employed in the converter will have some oxide or channel breakdown limit which must be considered. Also, the MEMS device itself will have a maximum field limit which it can withstand when its plates are closest together.

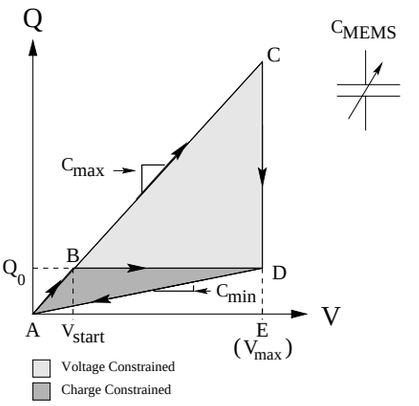

Fig. 2. Conversion Cycles

For the voltage-constrained case, the cycle starts when the capacitor is charged up to V_{max} from a reservoir. This is done when the capacitance of the MEMS transducer is at a maximum (C_{max}). During this time, the value of C_{MEMS} is taken to be constant, and so segment A-C is a straight line. This is a valid assumption since the charge-up time to traverse path A-C (and discharge path D-A) is an electrical time near 600ns, while path segment C-D, which corresponds to the plates moving, is traversed over a mechanical time near 400μs. As the plates move and the capacitance decreases, path segment C-D is traversed, where the capacitance is at a minimum. The mechanical force does work by causing charge to move from the capacitor back into the reservoir. The charge remaining on the plates is then recovered while $C_{MEMS} = C_{min}$ following path D-A. The net energy that has been gained, E, is the shaded area ACD in Figure

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2, and is given by [8]

$$E = \frac{1}{2}(C_{max} - C_{min})V_{max}^2 \quad (1)$$

This method sets a maximum limit on the conversion process. The major problem with this approach is that some method must be employed to constrain the voltage across the MEMS device during the conversion process, which would require another source of value V_{max}. This is an additional source to that of the conversion charge reservoir, which is of a lower voltage and is also used to power the control electronics. It is desirable to perform the conversion with a single source.

In the charge-constrained case, C_{MEMS} is charged to some initial voltage while its capacitance is at a maximum, which corresponds to path segment A-B in Figure 2. As the capacitor separates, the voltage increases as capacitance decreases until the plate displacement is at a maximum ($C_{MEMS} = C_{min}$) at point D. The amount of charge initially placed on the plates was precalculated such that when C_{MEMS} reaches its minimum, the value of the voltage across the capacitor is V_{max}. The charge is then returned to the reservoir from a greater voltage along path D-A. During this process the amount of charge on the plates does not change as the mechanical work is converted into electrical potential energy. The net energy out is the shaded area ABD. It is immediately obvious that this energy is less than what is possible with the voltage-constrained conversion cycle. The advantage is that now only a single charge source is needed to begin the process, and its value can be much less than V_{max}.

Figure 3 depicts another alternative. Here, a second capacitor of constant value, C_{par}, has been added in parallel to the MEMS device. The energy converted in shaded area acda, $E'_{voltcons}$ equals the converted energy of shaded area ac'd'a, so no benefit for the voltage-constrained cycle has been gained by incorporating C_{par}. However, if the energy converted for charge-constrained cycles abda and ab'd'a are compared, it is evident that more energy, $E'_{chrgcons}$ is converted in area ab'd'a.

$$E'_{chrgcons} = E'_{voltcons} - \frac{(\Delta Q)^2}{2(C_{par} + C_{max})} \quad (2)$$

Equation 2 shows that in the limit as C_{par} approaches infinity, the charge-constrained energy approaches that available through voltage-constraint. Therefore, it is desirable to have a parallel capacitor to, in effect, "hold" the voltage across the MEMS device constant, mimicking the behavior of the voltage constrained condition. The disadvantage to adding C_{par} is that now more initial charge is required for the conversion process. This means that the losses associated with reactive energy flow in the system will be increased. The tradeoff between increasing the capacitance of C_{par} and the increase in losses will be discussed in detail in section IV.

III. MEMS Device

The variable capacitor will be implemented using MEMS (microelectromechanical systems) technology, as shown in Figures 4 and 5. The capacitor has been analyzed and designed, and is now in fabrication. It will consist of a 1.5cm-by-0.5cm silicon structure etched in a wafer of 500μm thickness through a deep-reactive-ion etching process [9], as shown in Figure 4. The device wafer will be supported by an identical silicon handle wafer. The two wafers will be separated by a thin layer

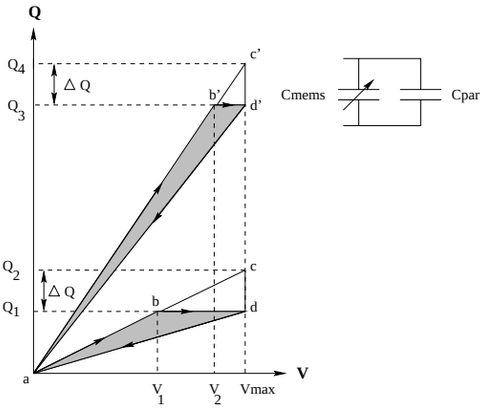

Fig. 3. Modified Energy Conversion with C_{par}

of silicon dioxide. The silicon will be heavily doped so that it acts as a very good conductor. The silicon dioxide acts as a bonding agent and as an insulator, thus forming a parasitic capacitor between the device and the handle wafer. The width of the silicon dioxide layer can be controlled to set the value of this parasitic capacitance as desired. The advantages of this parasitic capacitance were explained in section II.

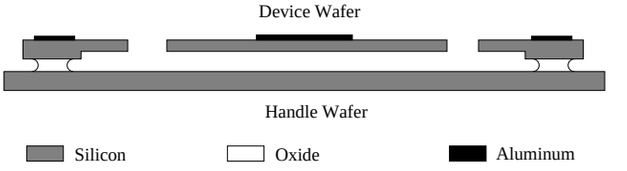

Fig. 4. MEMS Device Side View (Not to Scale)

A plan view of the MEMS capacitor is shown in Figure 5. It consists of three basic parts: a floating mass, a folded spring (one per side), and two sets of interdigitated combs, one per side. Each spring consists of four spring bars, a free rigid beam and a rigid anchor. The spring bars are connected to both the anchor and the free beam, limiting the motion of the mass to one dimension, as indicated in the figure.

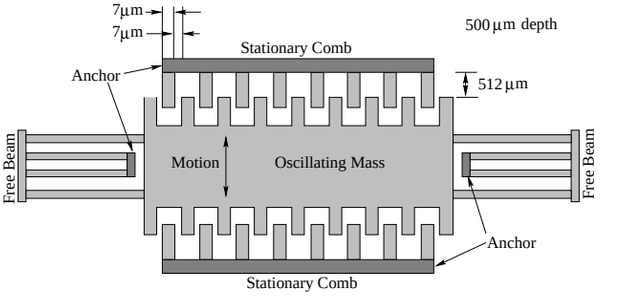

Fig. 5. MEMS Device Plan View (Not to Scale)

The interdigitated combs form two variable capacitors by connecting one terminal to the moving mass at the anchors and the others to each of the stationary combs. Since the characteristics of the variable capacitors are identical, the analysis in this

paper will focus on one of the variable capacitors and only one set of interdigitated combs. Note that the output power for one device can be doubled by taking into account the power obtained from the two variable capacitors.

The spring-mass system is designed to resonate with a mechanical vibration source applied to the casing to which the anchors are attached. The converter described here is designed for a mechanical vibration of 2,520Hz. The transfer of energy from the source to the spring-mass system is maximized by tuning the resonant frequency of the spring-mass system to that of the vibration source. This can be achieved by varying the dimensions of the spring in order to change its effective spring constant, or by changing the mass of the moving element.

As the mass oscillates, the interdigitated combs move together and apart, effectively varying the area of the variable capacitor, and, thus, its capacitance. The transfer of energy from the spring-mass system to the electrical circuit is governed by the change in capacitance of the interdigitated combs, as viewed from their electric terminals. In order to maximize this energy transfer, the change of capacitance must be maximized given constraints of space and structural soundness. In fact, one of the fundamental challenges in the design of the MEMS device is to provide a large enough change of capacitance given the design constraints. A large change of capacitance can be obtained by: (1) reducing the gap between the opposing elements of the comb structure, (2) increasing the height of the device, (3) elongating the fingers of the comb structure, and (4) increasing the length of the comb structure.

The minimal gap is limited by device fabrication technology. The current state-of-the-art sets this limit at around 7μm. This minimal gap limits the height of the device. As the height of the device increases, the minimal gap increases. It is expected that a 7μm gap may be etched as deep as 500μm. Spring travel and structural resonance limit the length of the fingers in the comb structure. Note that as the length of the combs is increased, the travel of the spring must also increase. Also, the combs' natural resonant frequency decreases as the comb fingers become longer. Given a minimal width for each comb finger of 7μm, a length of 512μm is required in order to keep the combs' natural frequency ten times larger than the mechanical vibration frequency. A spring with a peak-to-peak travel of 512μm appears feasible. The length of the comb structure is constrained by the dimensions of the spring and the overall device. As the length of the comb structure is increased, so does the moving mass. In order to keep the spring-mass system tuned to the desired frequency, the spring must be stiffened accordingly. However, the stiffness of the spring is limited by the length of the spring. As the spring gets longer, other undesirable modes of vibration are introduced. Furthermore, the dimensions of the device are specified to fit inside a 1.5cm-by-1.5cm square, including the springs. After an optimization is performed, the optimal size for the mass is found to be 1cm by 0.3cm. Given the previous constraints of gap size and comb finger width, each comb structure can have about 400 individual comb fingers.

An analysis of the capacitance with the comb structure fully closed yields a value of 260pF. Similarly, the value of the capacitance with the comb structure fully open is approximately 2pF. The analysis and design of the control and power electronics is based in these two values with a maximum gap voltage of 8V, which is set by the power electronics switch breakdown.

IV. Power Electronics

Figure 6 shows the implementation of the converter and accompanying waveforms associated with timing and system state variables. This represents one phase of the conversion process, as described in section III. The complete circuit would simply be Figure 6, with a counterpart mirrored about the load and control electronics. For all discussions of its operation, we will assume that the resonant LC period is much shorter than the vibration period. This is represented by the break on the time axis.

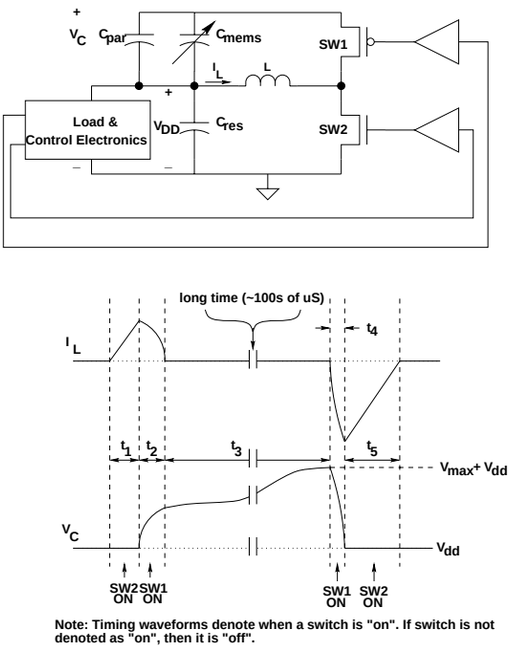

Fig. 6. System Implementation and Timing Waveforms

At startup, the capacitor combination of C_{par} and C_{MEMS} has no voltage across it, so $V_C = V_{DD}$. (Note that all voltages in Figure 6 are referred to ground.) At this point, the power electronics are waiting for the controller to determine when $C = C_{max}$ to begin the conversion process. Currently, this is an external signal input to the controller. This trigger occurs at the beginning of t_1. During t_1, SW2 is on, SW1 is off, and the inductor current ramps up. At t_2, SW2 is off, SW1 is on, and the inductor transfers energy to the capacitor. During t_3, both switches are off and the variable capacitor plates move apart. This time constant is near 400μs while the resonant on-time of the switches is approximately 600ns. It is therefore a reasonable approximation to say that the MEMS capacitor value is constant during t_1, t_2, t_4, and t_5. During t_3 the plates move from their minimum separation ($C_{max} + C_{par}$) to their maximum separation ($C_{min} + C_{par}$). The mechanical energy has moved the plates apart and caused the voltage across the capacitor combination to reach a maximum. Thus, energy harvesting is performed. During t_4 SW1 is on, SW2 is off, and the capacitor combination charges the inductor. Note that this LC time constant is smaller than t_2 because the overall capacitor value has decreased. Once

the capacitor voltage rings down, corresponding to one quarter of the resonant period of the LC, SW1 is turned off, SW2 is turned on, and the energy put into the inductor is transferred to the reservoir for t_5. This process repeats at the frequency of the mechanical vibration, which corresponds to variations in C_{MEMS}.

The overall system gains energy when the losses associated with the conversion process are less than the harvested energy. Because the values of L, C_{min}, C_{max}, and C_{par} are known, the timing pulses can be set such that synchronous rectification may be used, eliminating the need for diodes across SW1 and SW2. The main loss mechanisms in the conversion are switching and conduction losses associated with the power FETs, and conduction losses in the inductor.

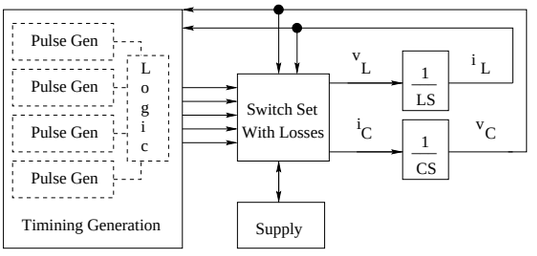

Fig. 7. Model Used for Analysis

As stated in section II, it is desirable to have a large valued capacitor in parallel with the MEMS device to improve energy conversion. This requires that more charge be initially placed on the capacitor plates, as shown in Figure 3. There is a practical limit to this charge due to the losses that occur in the inductor and SW2. They will have some series resistances, R_L and R_{DS} respectively, and this will limit the maximum value of current that the inductor will charge to, and therefore the initial energy we can place into the system. This maximum current will be $I_{Lmax} = V_{DD}/(R_L + R_{DS})$, where V_{DD} is the supply voltage. The main job of the inductor is to act as a charge source for the capacitor combination ($C_{MEMS} + C_{par}$), and this is accounted for when sizing L. The limits on the MEMS capacitor, C_{min} and C_{max} are fixed, so it is necessary to focus on the relationship between L and C_{par}. To do this, a mathematical model of the system was used along with real inductor specifications. This is depicted in Figure 7. L was modeled as the nominal values from the specifications, and C_{par} was varied to observe performance. Figure 8 shows optimization curves for C_{par} for three values of L, as well as the case where L and SW2 are lossless. For the non-lossless cases, $R_{DS} = 10\Omega$ based on simulation.

The peaking in the curves show that after some optimal value of C_{par}, the net energy gained decreases. This is due to the increased conduction losses in the inductor and power FETs (which are also included in the model). An optimum, therefore, occurs at $C_{par} = 180pF$ and $L = 220uH$ (with an $R_L = 19.8\Omega$). The lossless case was included to verify that as C_{par} was allowed to go to infinity, the energy out equaled that possible with a voltage constrained approach as discussed in section II. This was used to validate the model.

Once the value of C_{par} has been determined, it is possible to implement it as a parasitic capacitance in the MEMS device. Figure 4 shows a cross sectional view of the structure. It is possible to tailor the bonding oxide thickness such that a capacitance of value C_{par} is developed between the top and bottom wafers, eliminating the need for an external component or additional wafer area.

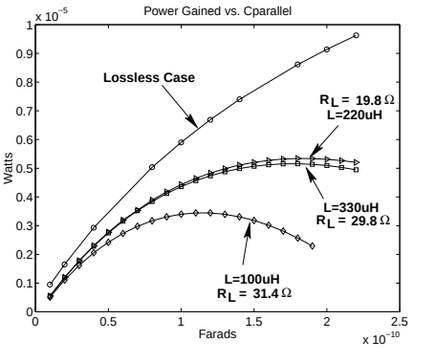

Fig. 8. C_{par} Optimization Curves

A straightforward approach to optimizing transistor width has been developed [10]. (In general we assume that the FETs will be sized to minimum or near minimum lengths and appropriate widths. The choice between minimum or non-minimum gate length depends on the voltages in the system and whether or not short channel effects are a concern.) This approach models the FETs as being in the linear region during operation with some constant gate drive V_{GS}. This model forms a useful basis for analysis of our converter, but will offer better results if we modify the assumptions to provide for a gate drive that varies over the course of one conversion period. This modified model more accurately reflects our converter as shown in Figure 6, where the PFET gate drive is given by $-V_C$. The power, P_{tot}, dissipated by a FET over the course of one switching period is given by

$$P_{tot} = I_{rms}^2 R_{DS} + f_{sw}(C_{GS}V_{GS}^2 + C_{dyn}V_{dyn}^2) \quad (3)$$

where the first term represents conduction losses (P_{cl}) and the second, lumped, term represents switching losses (P_{sw}). I_{rms} is the rms current through the device, R_{DS} is the on resistance of the FET, f_{sw} is the switching frequency, C_{GS} is the gate capacitance, V_{GS} is the gate drive voltage, C_{dyn} is the capacitance of the switched dynamic drain or source node, and V_{dyn} is the voltage the dynamic node is switched at. It is possible as in [10] to make some simplifications to the power loss optimization problem. The first is to combine the gate and drain or source capacitances if the drain and source extensions are roughly equivalent to the gate area. Also, if a further restriction on the system is that the gate drive voltage is always the same and is roughly equal to the switched voltage at the dynamic node, then the two lumped switching terms in (3) may be linearly combined to produce a simpler equation. For our system, this is not true. If we refer again to Figure 6, we see that the PFET causes special conditions to occur. For proper operation, we must ensure that during t_3 the PFET is off. This requires that there be a level converter driving its gate since the dynamic capacitor voltage V_C will start off at V_{DD} and increase to some V_{max}. This means that the PFET has a much higher gate drive during t_4 than during t_2. Figure 9 shows optimization curves for the power switches with the difference in gate drive accounted for.

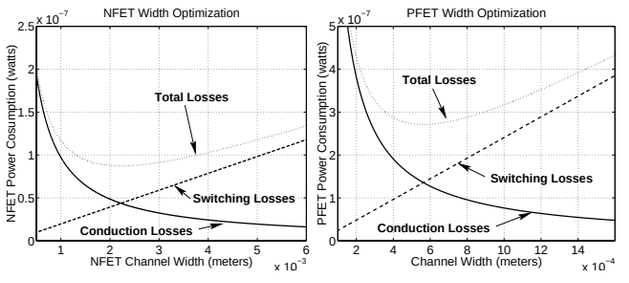

Fig. 9. Switch Optimization Curves

The values obtained from Figure 9 are $W_P = 538\mu$m and $W_N = 1399\mu$m. We can see that unlike previous complementary switcher designs [1], [10] the PFET is actually smaller than the NFET for minimal power losses. This is due not only to the fact that the PFET experiences higher gate drive for half of its switching duties, but also because of the fact that the NFET passes higher rms currents. One characteristic to note is that the curves, especially for the NFET, exhibit shallow troughs. This means that we can take a value off of the optimum and save in area at a very low power cost. Also, some of the power that appears to be lost by going to a shorter width is actually saved because the buffers needed to drive the power FETs' gates, as depicted in Figure 6 can become smaller. (The buffer losses were not included in the optimization algorithm because their sizing is dependent on the power FETs' width).

V. Controller Architecture

In order to experimentally verify the validity of the proposed method, a programmable controller was developed based on the mathematical model of Figure 7. Because the important system parameters $L, C_{par}, C_{max}, C_{min}$ and f_{sw} are known, we can realize the timing pulses through the use of a programmable delay line. The block diagram for a single pulse generator is shown in Figure 10. This is a hybrid delay

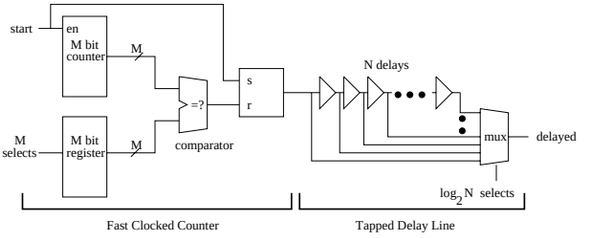

Fig. 10. Controller Block Diagram

line design which combines the area savings of a fast clocked counter approach with the resolution flexibility of a tapped delay line. The counter acts as a coarse adjust while the tapped delay line is used to fine tune the pulsewidth. The delay time for the counter block is set by comparing the count to some reference value. Once this has occurred, a pulse is sent down the tapped delay line and is picked off by a multiplexer. This sets the overall delay time. A simple power saving technique is to use an AND gate tied to the MSB of the multiplexer selects and placed in the middle of the delay line to decide whether the pulse propagates to the second half of the line. In cases where the MSB is not selected this prevents half of the delay line buffers from needlessly switching. It would be possible to gate all of the buffers in the delay line, but the additional overhead associated with decoding the multiplexer selects to vary the delay line length may make this approach undesirable.

Once the delay line has been designed, it may be duplicated four times and these individual sections combined with random logic to generate the four necessary timing pulses of duration t_1, t_2, t_4 and t_5.

Since the hybrid counter delay line architecture was chosen, it is necessary to generate a clock signal for the counter. One possibility is to bring in an external clock, and then gate the signal on chip to save power. However, the power that would be wasted in the IO pads would be constant and significant. Another possibility would be to integrate a low power oscillator on-chip, such as in [11]. In this case, the oscillator would consume static power. Since we have as inputs timing signals denoting when C_{min} and C_{max} occur, it would be beneficial for additional power savings to only have the clock operational when timing pulses are being generated. Also, it is desirable, for optimal conversion, to have the rising edge of the clock signal synchronous with the rising edge of the gate timing signal, and this would not be possible with an external oscillator. Instead, a resettable, synchronous, gated oscillator was used in order to conserve power. The oscillator circuit is shown in Figure 11. M1 serves to assure that the clock will have a rising

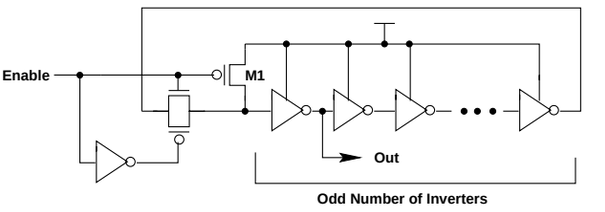

Fig. 11. Gated Oscillator Circuit

edge synchronous with the enable signal. The enabling gate assures that oscillations will only occur during timing pulses, reducing power consumption. Figure 12 shows output waveforms from the fabricated IC, demonstrating the oscillator's behavior.

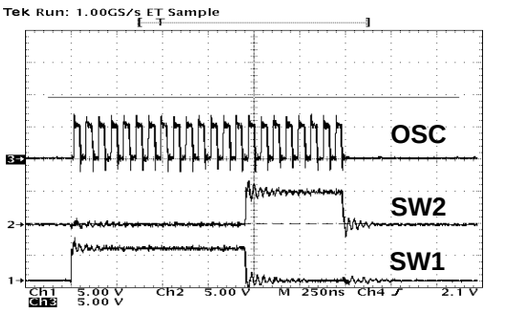

Fig. 12. Gated Oscillator Waveform

VI. Results

The programmable controller and associated power electronics have been implemented in a 0.6μm CMOS process. Figure 13 shows a photograph of the controller IC. This represents

one half of the total circuit. As stated in section III there are two phases of conversion; the controller IC was designed for a single phase. In order to extend the design for both phases, the present layout may simply be duplicated and will fit in the same area since the IC was pad, not area, limited. The system

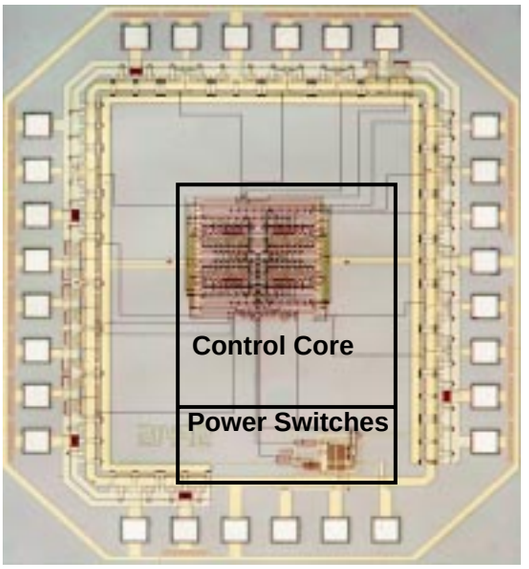

Fig. 13. Controller Block Diagram

has been tested for functionality and the controller measured for losses. Presently, the MEMS device is in fabrication, so a constant value capacitor was used in its place to verify correct operation. For purposes of verifying non-breakdown of the power switches, a DC source was switched in during t_3 of Figure 6 to emulate the MEMS device's behavior. Figure 14 depicts the correct operation of the controller. Table I presents the

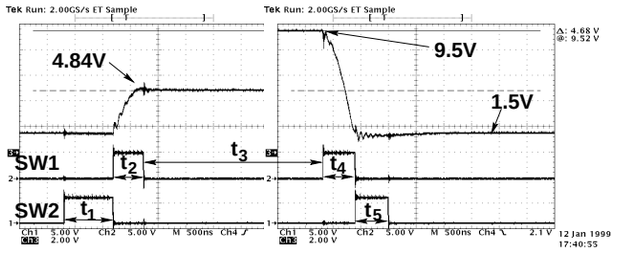

Fig. 14. Experimental Waveforms

relevant data taken during controller testing. All power values in the table may be doubled to account for both phases of the conversion period. Therefore, we may expect approximately 8μW out of the system at a $\Delta V_{MEMS} = 8.0$V.

VII. Conclusions

A system has been presented to convert ambient mechanical vibration into electric energy. The conversion process has been modified through the use of C_{par} to provide for maximal energy transfer. Several controller IC optimizations for low power, including power switch sizing, C_{par} capacitance, and oscillator design, have been performed. The controller has been verified to operate correctly and its losses have been measured. Based on predicted values of capacitance from the MEMS transducer, 8μW of power is expected to be available for use by a load, resulting in a self-powered electronic system.

Area	2163μm x 2554μm
Transistor Count	2661
Process	0.6μm CMOS
Predicted Converted Energy	8.66μW
Core Power	500nW ($f_{vib} = 2.5$kHz, $V_{dd} = 1.5$V)
Switch Loss Power	3.87μW ($\Delta V_{MEMS} = 8.0$V)
Predicted Power Out	4.29μW ($\Delta V_{MEMS} = 8.0$V)

TABLE I
Controller Specifications (half circuit)

VIII. Acknowledgments

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