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Virtual Impedance Based Fault Current Limiters for Inverter Dominated AC Microgrids

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***Abstract*—In this paper, a virtual impedance based fault current limiter (VI-FCL) is proposed for islanded microgrids comprised of multiple inverter interfaced distributed generators (DGs). Considering the increased fault current capability induced by high penetration of renewable energy sources (RESs), FCLs are employed to suppress the fault current and the subsequent oscillation and even instability in the modern distribution network with microgrids. In this study, rather than involving extra hardware equipment, the functionality of FCL is achieved in the control diagram of DG inverters by employing additional virtual impedance control loops. The proposed VI-FCL features flexible and low-cost implementation and can effectively suppress the fault current and the oscillation in the following fault restoration process in AC microgrids. The systematic model of the inverter dominated AC microgrid is derived, and the stability analysis in consideration of VI-FCLs is thereby studied. MATLAB/Simulink model comprised of three inverter-interfaced DGs is implemented to verify the feasibility of the proposed method.**

***Index Terms*—AC microgrid, distributed generation, fault current limiter, interface inverter, virtual impedance**

I. Introduction

THE increasing penetration of renewable energy sources (RESs) has significantly challenged the modern distribution systems in terms of bidirectional power flow in active distribution network [1], stochastic and intermittent power generation [2], different fault current capability [3], etc. In order to effectively control and manage the distributed generators (DGs), the concept of microgrid was proposed years ago to aggregate distributed sources and loads [4]. By employing the proper design and control algorithm, a microgrid can be used to enhance the reliability of distributed generation networks and reduce the operation cost. Meanwhile, by integrating microgrid controller with distribution management system (DMS), the functionality of microgrid can be further extended.

In order to improve the controllability of RESs and ensure the required power quality, power electronic inverters are widely employed as the interfaces [5]. Considering the distributed configuration of DGs, the interface inverters are usually connected in parallel [6]. A general configuration of AC microgrids is depicted in Fig. 1. It should be noted that the proper power sharing among different interface inverters should be achieved to avoid the unnecessary power circulation and the additional power loss. Different control strategies are proposed to realize the proper active and reactive power sharing, e.g. master-slave control [7], circular-chain-control (3C) [8], average current control [9], etc. It should be noticed that the above power sharing methods and their variants are realized based on dedicated high bandwidth communication network, which is less applicable for microgrids considering its distributed nature. Droop control and its modified versions are widely employed in microgrids [10]–[13]. Since it relies on only local information, a decentralized control diagram can be reached. Hence, it is more suitable for power sharing in microgrids compared to the communication-based methods. In order to fulfill the multiple requirements in microgrid operation and implement a systematic control algorithm, a hierarchical control diagram is proposed in [14], including the control objectives of local power sharing, voltage frequency and amplitude restoration, and active and reactive power control when interacting with external utility grid. The lower control layer of the hierarchical control diagram is reached based on decentralized control method, and the higher control layers are implemented based on low bandwidth communication links.

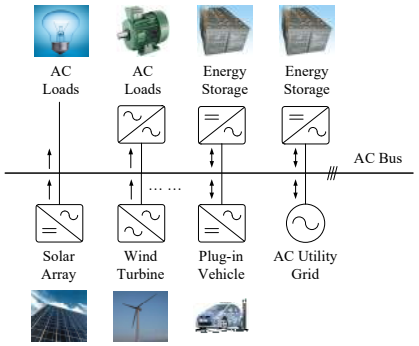

Fig. 1. General configuration of AC microgrids.

Fault protection schemes should be designed properly to ensure the safe and reliable operation of microgrids. In consideration of DG participation, the protection strategies of microgrids are more complicated than conventional passive distribution systems. The DGs may lead to missing operation or sympathetic tripping of the protective devices (PDs) during fault conditions. Meanwhile, since the fault current inside a microgrid is synthesized by the upstream utility grid and DG branches, the related relay settings for conventional distribution systems should be modified accordingly [3]. Especially for inverter dominated microgrids, the inertia of inverter-interfaced DGs is lower compared to the rotation-based DGs, e.g. small hydro, diesel generator, etc., and the

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fault current limits are reduced due to the inverter power rating.

Various strategies are proposed to improve the protection schemes for inverter dominated microgrids. In [15], the amplitude of the inverter output current is calculated to detect the fault, and it is constrained to the maximum value during fault condition. For fault restoration, the post- and pre-fault values of the output current are compared to identify if significant change is entailed in the microgrid. In [16], the voltage magnitude regulation scheme and phase lock loop (PLL) are modified to enhance the performance during faults, and a phase angle restoration loop is employed to improve the fault ride through capability of the inverter interfaces and improve the process of post-fault recovery. In [17], the fault responses of AC microgrids with single inverter and multiple inverters are discussed, and the positive sequence equivalent P&Q model and current source model are derived for analyzing the operation of the interface inverter during faults. In [18], a fault current alleviation method is accomplished by measuring the remote voltage signal of the point of common coupling (PCC). By comparing the local output voltage and PCC voltage, the difference between the amplitudes and the phase angles are minimized to reduce the fault current. In [19], the protection strategy is implemented by using digital relays with communication capability. The failures of hardware devices and communication links are taken into account in the hierarchy of protection scheme. In [3], a multi-layer protection diagram is proposed, including load-way level, loop level, loop-feeder level and microgrid level, which is suitable for different microgrid configurations.

In order to mitigate the influence of fault current in microgrids, fault current limiters (FCLs) are studied and developed. The FCLs behave as rather low impedances in microgrids in the normal operation, while during faults, it becomes a large impedance and limit the amount of fault current. Hence, the uninterrupted operation of electrical systems can be obtained. Two types of technologies for FCLs currently exist, i.e., high temperature superconducting (HTS)-based FCL and solid-state circuit (SSC)-based FCL [20]. For HTS-based FCL, the characteristic of superconductor is utilized to change the impedance. For SSC-based FCL, it is essentially an additional power electronic converter series-connected in the power cable. The discussion of FCLs is found in existing literature. In [21], the functionality of dynamic voltage restorer (DVR) is extended to implement a SSC-based FCL and alleviate the impact of downstream fault current. In [22] and [23], additional inverters are series-connected to the feeder impedance to form a SSC-based FCL and emulate resistive or inductive impedance during faults. In [24], a unidirectional FCL is developed and placed between downstream microgrid and upstream utility grid to cope with the downstream faults. In [25] and [26], the optimal positioning of HTS-based FCLs is discussed. Especially in [26], the location of FCLs in hybrid AC and DC microgrids is studied to ensure the effective suppression of fault current. In [27], HTS-based FCL is employed to protect the key energy storage units in the system. In [28], a constrained nonlinear programming problem is formulated to optimally select the relay settings and size FCLs.

Virtual impedance as a cost-effective and flexible approach has been employed in the control diagram of microgrids in the past years. It can be used to match the output impedance of each interface inverter and decouple the active and reactive power sharing in droop-controlled microgrids [29], [30]. Meanwhile, a virtual impedance can be also used to dampen the resonance peaks in LCL-filtered inverters to increase the stability margin [31], or emulate required damping impedance at different harmonic frequencies so that the certain harmonic components can be eliminated [32].

In this paper, a virtual impedance based FCL (VI-FCL) is proposed to suppress the fault current in islanded AC microgrids. Since three-phase faults have the highest impact on system operation, the proposed method is mainly designed for alleviating the influence of symmetrical three-phase faults. For asymmetrical faults, similar approaches can be developed by implementing VI-FCLs in positive and negative sequences, respectively. Compared to the existing methods of implementing FCLs, the VI-FCL features lower capital and maintenance costs. No extra superconducting devices or inverters are required to work as FCLs. The existing current controller in the primary control level of a DG unit does not work for limiting the fault current considering controller saturation, huge amount of fault current and low voltage at the fault location. By involving additional virtual impedance loops in the DG interface inverters, large output impedances can be implemented during faults to emulate the physical inductance and resistance in the real FCLs. Meanwhile, in normal operation, the VI-FCLs keep zero to avoid unnecessary voltage drops. Furthermore, it should be noted that by using the proposed VI-FCL, the fault ride through capability of DG unit can be enhanced. Hence, they do not need to be cut off although the fault occurs. Compared to the conventional current/voltage based protection schemes, the proposed method does not interrupt the DG operation, so the complicated resynchronization algorithm for DG reconnection can be avoided. The principle and implementation of the proposed VI-FCL is introduced in this study. Meanwhile, a systematic model of inverter dominated AC microgrids during faults is derived, and the stability analysis of the overall system is thereby analyzed. A MATLAB/Simulink model comprised of three interface inverters is implemented to verify the effectiveness of the proposed VI-FCL. Meanwhile, real-time hardware-in-the-loop (HIL) test based on OPAL-RT platform is also conducted to further verify the feasibility of the proposed method.

The following paper is organized as follows. Section II introduces the principle and implementation of VI-FCL. Section III analyzes the model of AC microgrids during faults and conduct the stability analysis of the overall control diagram with VI-FCLs. Section IV shows the simulation results for different cases. Finally, Section V summarizes the paper and draws the conclusion.

II. Principle and Implementation of VI-FCLs

A. Principle of VI-FCL

The simplified configuration of AC microgrids dominated by multiple interface inverters is shown in Fig. 2. Each inverter interfaced DG unit is modeled by using a voltage source and two virtual impedances. The reference value of the voltage source is calculated by droop control method [14]. In particular, the reference values of the voltage frequency and amplitude are generated as follows:

$$f_i = f^* - mP_{oi} \tag{1}$$

$$E_i = E^* - nQ_{oi} \tag{2}$$

where f_i and E_i are the voltage frequency and amplitude, f^* and E^* are their reference values, m and n are the droop coefficients, and P_{oi} and Q_{oi} are the output active and reactive power, i = 1, 2, …, n.

Note that the frequency and amplitude deviation of the local output voltage should be limited within the acceptable range, namely

$$\left|f^* - f_i\right| \le \Delta f_{max} \tag{3}$$

$$\left|E^* - E_i\right| \le \Delta E_{max} \tag{4}$$

where Δf_{max} and ΔE_{max} are the maximum acceptable deviation of the frequency and amplitude.

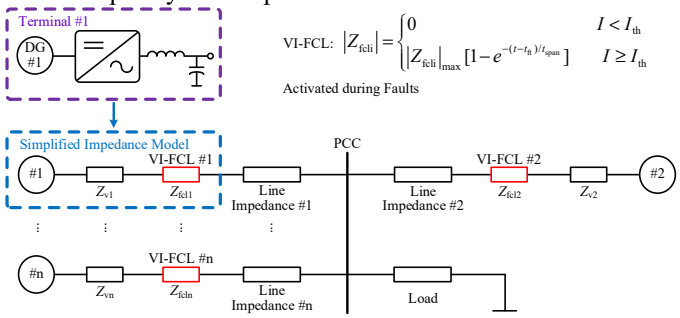


Fig. 2. Configuration of AC microgrids dominated by multiple interface inverters.

The two virtual impedances in the equivalent model of the inverter interfaced DG unit are represented by Z_{vi} and Z_{fcli}, respectively. Here, Z_{vi} is used to decouple the active and reactive power sharing and ensure the droop relationship shown in (1) and (2) [29], [30], and Z_{fcli} is involved to represent the VI-FCL, which is activated only during faults and keeps zero in normal operation. The amplitude of Z_{fcli} is calculated as:

$$|Z_{fcli}| = \begin{cases} 0 & I < I_{th} \\ |Z_{fcli}|_{max}[1-e^{-(t-t_{ft})/t_{span}}] & I \ge I_{th} \end{cases} \tag{5}$$

where $|Z_{fcli}|_{max}$ is the maximum amplitude of the virtual impedance that is determined by considering the acceptable fault current level, t_{ft} is the time when the measured peak current exceeds the threshold, t_{span} is the transient time for the amplitude of the virtual impedance changing from 0 to the maximum value, I is the peak value of the current, and I_{th} is the current threshold of triggering the FCLs.

Based on the above definition, the overall control diagram is shown in Fig. 3, and the flow chart of the working principle of VI-FCL is shown in Fig. 4. In the control diagram in Fig. 3, proportional-resonant (PR) controllers are used in the inner voltage and current control loops [30], which can be shown as:

$$G_v = k_{pv} + \frac{k_{rv} \cdot s}{s^2 + \omega^2} \tag{6}$$

$$G_c = k_{pc} + \frac{k_{rc} \cdot s}{s^2 + \omega^2} \tag{7}$$

where G_v and G_c are the transfer functions of the inner voltage and current controllers, k_{pv} and k_{rv} are the coefficients of the proportional and resonant terms in G_v, k_{pc} and k_{rc} are the coefficients of the proportional and resonant terms in G_c, ω is the angular frequency, s is the Laplace operator.

Meanwhile, it should be noted that secondary control is employed to eliminate the deviations of frequency and amplitude in normal operation. By using secondary frequency and voltage amplitude control, two compensation terms related to the phase angle Φ and voltage amplitude E, i.e., $\delta\Phi$ and δE, are generated and added to the voltage reference. The fault is detected when the peak value of output current reaches its threshold, and the secondary control is deactivated while the VI-FCL is activated. Then, the amplitude of Z_{fcl} reaches its maximum value to alleviate the amount of fault current. When the peak value of output current falls below its threshold, the VI-FCL is deactivated to avoid unnecessary voltage drop, and the secondary control is reactivated to restore the voltage frequency and amplitude. Here, deactivating secondary control refers to resetting the proportional-integral (PI) controllers in the secondary control level and stop adding the compensation terms, i.e., $\delta\Phi$ and δE, into the voltage reference.

It can be seen that the VI-FCL, i.e., Z_{fcli}, is only activated during fault conditions. However, as aforementioned, when the fault occurs, secondary control should be deactivated. The reason for deactivating secondary control during faults is that the voltage is forced to drop down due to the existence of fault impedance and this voltage drop is inevitable. Since secondary control is used to restore the voltage, it conflicts with voltage drop induced by the faults. Hence, it should be deactivated to avoid the instable operation of the control diagram.

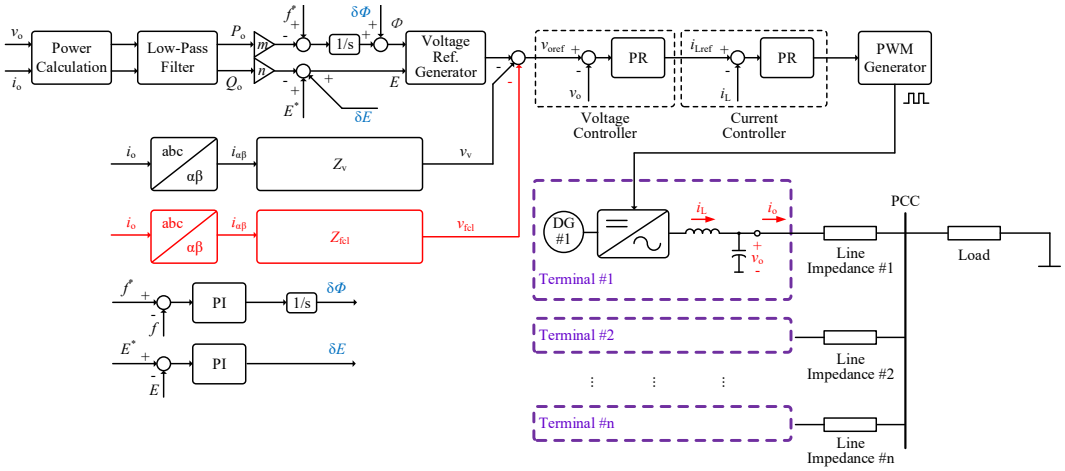


Fig. 3. Overall control diagram including the additional control loop of VI-FCL.

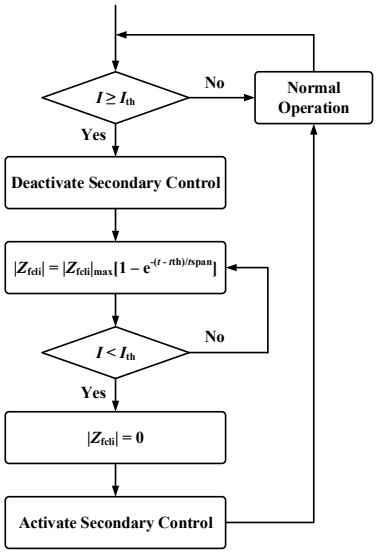


Fig. 4. Flow chart of the working principle of VI-FCL.

B. Design and Implementation of VI-FCL

In order to properly design the VI-FCL, as shown in Fig. 5, the representative system is employed, where the $\dot{Z}_l$, $\dot{Z}_v$, $\dot{Z}_{fcl}$ and $\dot{Z}_g$ represent the vectors of line impedance, virtual impedance Z_v, VI-FCL Z_{fcl} and the ground impedance at the fault location, respectively, and $\dot{Z}_{fcl}$ is only activated during faults. The impedances $\dot{Z}_l$, $\dot{Z}_v$ and $\dot{Z}_{fcl}$ can be written as:

$$\begin{cases} \dot{Z}_l = |\dot{Z}_l| \angle \theta_l \\ \dot{Z}_v = |\dot{Z}_v| \angle \theta_v \\ \dot{Z}_{fcl} = |\dot{Z}_{fcl}| \angle \theta_{fcl} \end{cases} \tag{8}$$

where θ_l, θ_v and θ_{fcl} are the phase angles of the corresponding impedances.

In order to simplify the analysis and avoid the potential instability issue, $\dot{Z}_{fcl}$ is selected to be in phase with $\dot{Z}_v$. Therefore, it is achieved that:

$$\begin{cases} \theta_{fcl} = \theta_v \\ |\dot{Z}_{fcl}| = k|\dot{Z}_v| \end{cases} \tag{9}$$

where k represents the ratio between $|\dot{Z}_{fcl}|$ and $|\dot{Z}_v|$.

As shown in [29]-[30], the virtual impedance Z_v is used to ensure that the active and reactive power sharing follows the droop control expression shown in (1) and (2) in normal condition. In order to meet this requirement, Z_v should be significantly inductive. To quantitatively identify the required $|\dot{Z}_v|$ and θ_v, the phasor diagram of the impedances as shown in Fig. 6 are employed. It is defined that:

$$\dot{Z}_{eq} = \dot{Z}_l + \dot{Z}_v \tag{10}$$

Hence, in order to guarantee that the equivalent line impedance $\dot{Z}_{eq}$ in normal condition is significantly inductive, the phase angle of $\dot{Z}_{eq}$, i.e., θ_{eq}, should be almost 90°. Namely,

$$90^\circ - \theta_{eq} \le \theta_{eqm} \tag{11}$$

where θ_{eqm} is the maximum acceptable phase difference, which is selected as 2° here.

By using the cosine law in the triangle ΔOBC, it is derived that:

$$|\dot{Z}_{eq}| = \sqrt{|\dot{Z}_v|^2 + |\dot{Z}_l|^2 - 2|\dot{Z}_v||\dot{Z}_l|\cos(90^\circ - \theta_v + \theta_l)} \tag{12}$$

Meanwhile, by using the sine law in the same triangle, it yields that:

$$\alpha = \arcsin\left[\frac{|\dot{Z}_v|}{|\dot{Z}_{eq}|}\sin(\theta_v - \theta_l)\right] \tag{13}$$

where $\alpha = \angle COB$.

Hence, it can be derived that:

$$\theta_{eq} = \alpha + \theta_l \tag{14}$$

For a given system, $|\dot{Z}_l|$ and θ_l are commonly vary within a certain range that is determined by the practical condition of the DG branch. The selection of $|\dot{Z}_v|$ and θ_v should make sure that for arbitrary $|\dot{Z}_l|$ and θ_l within their ranges, the equivalent line impedance $\dot{Z}_{eq}$ should be significantly inductive, i.e., the criteria established by combining (11) – (14) should be satisfied. In the given system, assuming that $|\dot{Z}_l|$ varies within the range of 0.5 ~ 1 Ω and θ_l varies within the range of 80° ~ 87.5°, by using MATLAB m-script to search the suitable $|\dot{Z}_v|$ and θ_v, it can be reached that:

$$\begin{cases} |\dot{Z}_v| = 1.40\Omega \\ \theta_v = 89^\circ \end{cases} \tag{15}$$

Note that some more choices of $|\dot{Z}_v|$ that is larger than 1.40 Ω can be selected to meet the criteria established by (11) – (14). Since larger $|\dot{Z}_v|$ reduces the output voltage in normal condition, the smallest $|\dot{Z}_v|$ that fulfills the criteria is selected

here in (15).

After designing $|\dot{Z}_v|$ and θ_v, as mentioned in (9), it is achieved that:

$$\theta_{fcl} = \theta_v = 89^\circ \tag{16}$$

Therefore, the next step for the design procedure is to select the suitable k so that the vector $\dot{Z}_{fcl}$ can be determined.

As shown in the representative system in Fig. 5, in case of a fault occurring at the DG branch, a parameter λ is employed to indicate the fault location. It is defined as:

$$\lambda = \left| \frac{\dot{Z}_{la}}{\dot{Z}_{la} + \dot{Z}_{lb}} \right| \tag{17}$$

where $\dot{Z}_{la}$ is the part of the line impedance near the DG unit, while $\dot{Z}_{lb}$ is the part of the line impedance near the PCC, and $\dot{Z}_{la} + \dot{Z}_{lb} = \dot{Z}_l$. The smaller λ indicates that the fault is near the DG terminal, while the larger λ indicates the fault is near the PCC.

The variable k should be determined by limiting the maximum $|\dot{I}_o|$ lower than $|\dot{I}_o|_{max}$. As shown in Fig. 5, when the fault occurs, the voltage at the fault location can be regarded as almost zero. Hence, it can be calculated that:

$$\left|\dot{I}_o\right| = \left| \frac{\dot{V}_{ref}}{\left|\dot{Z}_{l1}\right|\angle\theta_l + \left|\dot{Z}_v\right|\angle\theta_v + k\left|\dot{Z}_v\right|\angle\theta_v} \right| \le \left|\dot{I}_o\right|_{max} \tag{18}$$

Assuming that the phase angle of $\dot{V}_{ref}$ is zero and $|\dot{V}_{ref}|$ = 110 V, (18) should be satisfied with arbitrary line impedances and fault locations. In other words, for the given system, (18) should be fulfilled with arbitrary $|\dot{Z}_l|$ within the range of 0.5 ~ 1 Ω, arbitrary θ_l within the range of 80° ~ 87.5°, and arbitrary λ within the range of 0 ~ 1.

Similar to the design procedure of $|\dot{Z}_v|$ and θ_v, the suitable value of the variable k can be searched by using MATLAB m-script. Here, it is obtained that k equals 4.

Note that larger k can be also selected to meet the requirement in (18). In order to avoid the unnecessary voltage deviation during faults, the minimum k that satisfies (18) is selected here.

Hence, by summarizing the above results, it yields:

$$\dot{Z}_{fcl} = \left|\dot{Z}_{fcl}\right|\angle\theta_{fcl} = k\left|\dot{Z}_v\right|\angle\theta_v = 4\times1.4\angle89^\circ = 5.6\angle89^\circ \tag{19}$$

It should be noticed that for multiple inverters in an AC microgrid, the VI-FCL for each interface inverter should be designed individually based on the practical line impedance $\dot{Z}_l$ and the virtual impedance $\dot{Z}_v$.

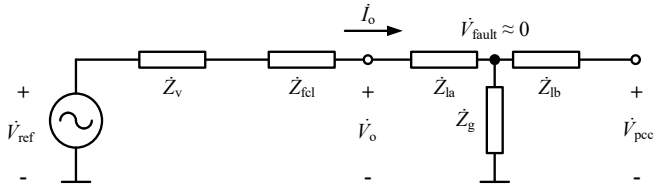


Fig. 5. Representative system for the design of VI-FCL.

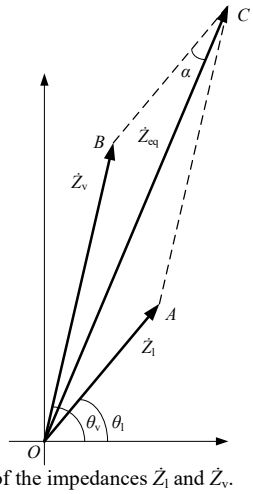


Fig. 6. Phasor diagram of the impedances $\dot{Z}_l$ and $\dot{Z}_v$.

III. Modeling and Analysis of AC Microgrids with VI-FCLs

A. Modeling of AC Microgrids with VI-FCLs during Faults

In order to analyze the effectiveness of VI-FCLs, the model of AC microgrids during faults is analyzed as follows. Take an AC microgrid with three DGs as an example. The impedance model of AC microgrids during faults is shown in Fig. 7, where Z_{load} is the load impedance and Z_g is the ground impedance of the fault. It is assumed that the fault occurs at the branch of DG #1.

For each DG interface inverter, the configuration of the main power circuit and the corresponding control diagram are shown in Fig. 8 (a) and (b). It can be derived based on the control diagram in Fig. 8 (b) that:

$$\begin{aligned} v_{oi} = {} & \frac{G_{vi}G_{ci}G_dG_{capi}}{G_{ci}G_d + G_{indi} + (1+G_{vi}G_{ci}G_d)G_{capi}} \cdot v_{refi} \\ & - \frac{G_{vi}G_{ci}G_dG_{capi}(Z_{vi}+Z_{fcli}) + (G_{ci}G_d + G_{indi})G_{capi}}{G_{ci}G_d + G_{indi} + (1+G_{vi}G_{ci}G_d)G_{capi}} \cdot i_{oi} \end{aligned} \tag{20}$$

where G_{vi} and G_{ci} are the inner voltage and current controllers, respectively, G_d represents the PWM generation unit, G_{capi} is the transfer function of the inverter filter capacitor, G_{indi} is the transfer function of the inverter filter inductor, v_{oi} and i_{oi} are the output voltage and current of inverter #i, and v_{refi} is the reference value of v_{oi} (i = 1, 2, 3).

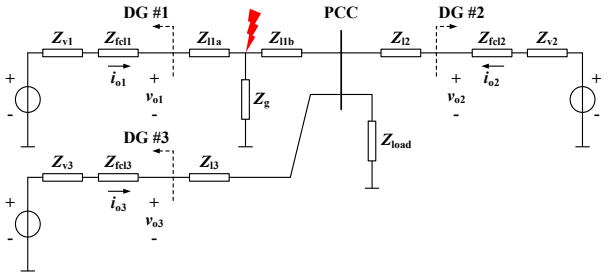
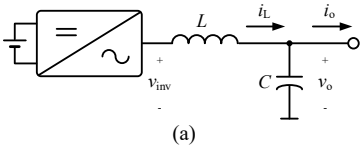
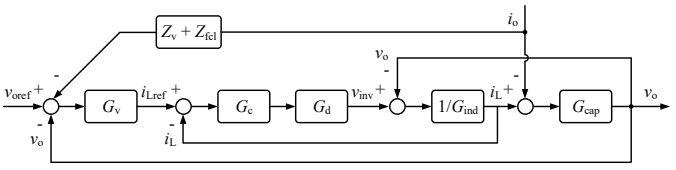


Fig. 7. Impedance model of the AC microgrid with VI-FCLs during faults.



(a)



(b)

Fig. 8. Detailed configuration of each DG interface inverter.
(a) Main power circuit configuration. (b) Control diagram of each DG interface inverter.

It should be noted that first-order approximation, as shown in the transfer function G_d, is used here to represent the procedure of PWM generation [33]. Meanwhile, G_{vi} and G_{ci} are the common PR voltage and current controllers, respectively. The transfer functions of G_{vi}, G_{ci}, G_d, G_{capi} and G_{indi} are shown below:

$$G_{vi} = k_{pvi} + \frac{k_{rvi} \cdot s}{s^2 + \omega^2}, G_{ci} = k_{pci} + \frac{k_{rci} \cdot s}{s^2 + \omega^2}$$
$$G_d = \frac{1}{1 + T_d \cdot s}, G_{capi} = \frac{1}{sC_i}, G_{indi} = sL_i \quad (21)$$

where k_{pv} and k_{rv} are the proportional and resonant coefficients of the voltage PR controller, k_{pci} and k_{rci} are the proportional and resonant coefficients of the current PR controller, T_d is the delay induced by PWM generation and duty cycle updating, C_i is the inverter filter capacitance, and L_i is the inverter filter inductance.

For simplification, (20) can be rewritten as:

$$v_{oi} = G_{refi} \cdot v_{refi} - Z_{oi} \cdot i_{oi} \ (i=1, 2, 3) \quad (22)$$

where

$$G_{refi} = \frac{G_{vi}G_{ci}G_dG_{capi}}{G_{ci}G_d + G_{indi} + (1 + G_{vi}G_{ci}G_d)G_{capi}}$$
$$Z_{oi} = \frac{G_{vi}G_{ci}G_dG_{capi}(Z_{vi} + Z_{fcli}) + (G_{ci}G_d + G_{indi})G_{capi}}{G_{ci}G_d + G_{indi} + (1 + G_{vi}G_{ci}G_d)G_{capi}}$$

The system model can be derived by using superposition theorem based on the impedance network in Fig. 7, namely each output current or voltage can be calculated by considering the sum of that variable in each case with single source. Take the output current of DG #1 as an example. It is obtained that:

$$i_{o11} = \frac{v_{o1}}{[Z_{load} // Z_{l2} // Z_{l3} + (1-\lambda)Z_{l1}] // Z_g + \lambda Z_{l1}} \quad (23)$$

$$i_{o12} = -\frac{v_{o2}}{[(\lambda Z_{l1}) // Z_g + (1-\lambda)Z_{l1}] // Z_{load} // Z_{l3} + Z_{l2}} \cdot \frac{Z_{load} // Z_{l3}}{(\lambda Z_{l1}) // Z_g + (1-\lambda)Z_{l1} + Z_{load} // Z_{l3}} \cdot \frac{Z_g}{\lambda Z_{l1} + Z_g} \quad (24)$$

$$i_{o13} = -\frac{v_{o3}}{[(\lambda Z_{l1}) // Z_g + (1-\lambda)Z_{l1}] // Z_{load} // Z_{l2} + Z_{l3}} \cdot \frac{Z_{load} // Z_{l2}}{(\lambda Z_{l1}) // Z_g + (1-\lambda)Z_{l1} + Z_{load} // Z_{l2}} \cdot \frac{Z_g}{\lambda Z_{l1} + Z_g} \quad (25)$$

where i_{o11}, i_{o12} and i_{o13} are the output current of DG #1 in each decomposition system, and v_{o1}, v_{o2} and v_{o3} are the corresponding output voltage of each DG unit.

Hence, it yields:

$$i_{o1} = i_{o11} + i_{o12} + i_{o13} = Y_{11} \cdot v_{o1} + Y_{12} \cdot v_{o2} + Y_{13} \cdot v_{o3} \quad (26)$$

where Y_{11}, Y_{12} and Y_{13} are the coefficients in (23) – (25).

By using the same procedure, the output current of each DG branch can be reached, which can be summarized as:

$$\begin{bmatrix} i_{o1} \\ i_{o2} \\ i_{o3} \end{bmatrix} = \overline{Y} \cdot \begin{bmatrix} v_{o1} \\ v_{o2} \\ v_{o3} \end{bmatrix} \quad (27)$$

where $\overline{Y}$ is the coefficient matrix with elements Y_{ij} (i, j = 1, 2, 3).

Combining (22) (i = 1, 2, 3) and (27), it is achieved that:

$$\begin{bmatrix} v_{o1} \\ v_{o2} \\ v_{o3} \end{bmatrix} = (1 + \overline{Z}_o \overline{Y})^{-1} \overline{G}_{ref} \cdot \begin{bmatrix} v_{ref1} \\ v_{ref2} \\ v_{ref3} \end{bmatrix} \quad (28)$$

where

$$\overline{Z}_o = \begin{bmatrix} Z_{o1} & & \\ & Z_{o2} & \\ & & Z_{o3} \end{bmatrix}, \overline{G}_{ref} = \begin{bmatrix} G_{ref1} & & \\ & G_{ref2} & \\ & & G_{ref3} \end{bmatrix}$$

Hence, the stability of the system with VI-FCLs can be studied by analyzing the dominant poles of the transfer functions v_{oi}/v_{refi} (i = 1, 2, 3) in (28).

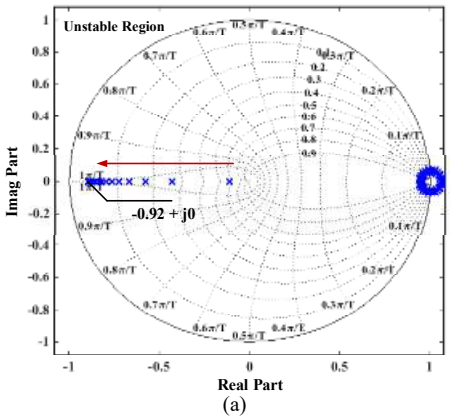
B. Stability Analysis of VI-FCLs

For the given system in Table I [34], by defining that $Z_v = R_v + s \cdot L_v$, $Z_{fcl} = R_{fcl} + s \cdot L_{fcl}$, $Z_{load} = R_{load} + s \cdot L_{load}$, $Z_g = R_g + s \cdot L_g$, and using bilinear transformation of $s = 2/T_d \cdot (1 - z^{-1})/(1 + z^{-1})$, where T_d is the unit delay induced by PWM generation, the stability analysis during faults is conducted by assessing the locations of dominant poles in z domain [35]–[40]. It should be noticed that the transient rising time t_{span} of VI-FCL in (5) is much smaller than the fault duration. Hence, only the steady state value of Z_{fcl} during fault needs to be considered here.

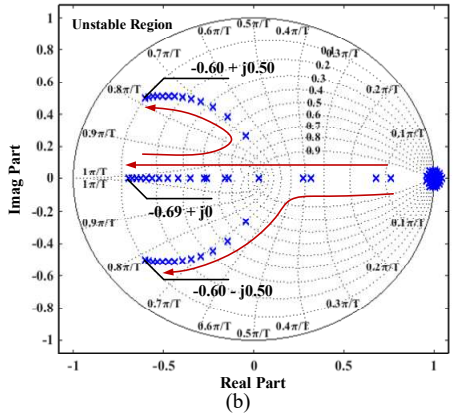
When increasing the virtual inductance L_{fcl} from 50 nH to 80 mH and having R_{fcl} as 97.6 mΩ, it can be seen in Fig. 9 (a) that the dominant pole of system moves towards the unstable region. When the dominant pole locates near the stability boundary (the unit circles in Fig. 9 (a)), e.g., p_{L1} = -0.92 + j0, the system stability is challenged to be at risk. It should be noted that the poles locating on the right side of the figure are not the dominant poles since they are cancelled by the zeros. Similar situations exist for the z domain stability analysis in Fig. 9 (b) and (c). When increasing the virtual resistance R_{fcl} from 5 mΩ to 1 Ω and keeping L_{fcl} as 14.8 mH, it can be seen that three dominant poles move towards the stability boundary. As shown in Fig. 9 (b), the dominant poles are finally shown as p_{R1} = -0.69 + j0 and $p_{R2,3}$ = -0.60 ± j0.50. It should be noticed that the impact of p_{R1} and $p_{R2,3}$ are less significant compared to the case with increasing virtual inductance L_{fcl} since their magnitudes are smaller than the dominant pole p_{L1} in Fig. 9 (a). Meanwhile, as aforementioned, a parameter λ is involved to indicate the fault location. When changing λ and keeping L_{fcl} = 14.8 mH and R_{fcl} = 97.6 mΩ, all the dominant poles statically locate in the stable region without a trend to orient the unstable boundary. Hence, the proposed VI-FCL method is valid for different fault locations.

TABLE I
SYSTEM PARAMETERS

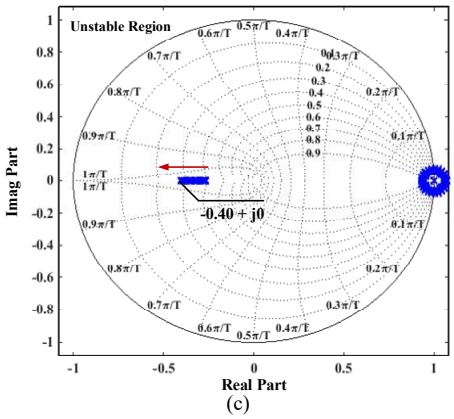
Symbol	Parameter	Value	
f^*	Rated voltage frequency	60	Hz
E^*	Rated RMS voltage	110	V
L_{l1}	Line inductance #1	2.5	mH
R_{l1}	Line resistance #1	0.08	Ω
L_{l2}	Line inductance #2	1.8	mH
R_{l2}	Line resistance #2	0.03	Ω
L_{l3}	Line inductance #3	1.8	mH
R_{l3}	Line resistance #3	0.03	Ω
L_{load}	Load inductor	20	mH
R_{load}	Load resistor	0.4	Ω
L_g	Grounding inductance	0.03	mH
R_g	Grounding resistance	0.6	mΩ
L	Filter inductance of the inverter	1	mH
C	Filter capacitance of the inverter	47	μF
k_{pv}	Proportional coefficient of the voltage PR controller	0.6	-
k_{rv}	Resonant coefficient of the voltage PR controller	2	-
k_{pc}	Proportional coefficient of the current PR controller	1	-
k_{rc}	Resonant coefficient of the current PR controller	2	-
M	Droop coefficient for voltage frequency	0.0006	rad/(W·s)
n	Droop coefficient for voltage amplitude	0.02	V/Var
k_{pfs}	Proportional term of secondary frequency control	3×10^{-4}	-
k_{ifs}	Integral term of secondary frequency control	1.4	-
k_{pes}	Proportional term of secondary voltage amplitude control	2×10^{-3}	-
k_{ies}	Integral term of secondary voltage amplitude control	4	-
f_s	Switching frequency	10	kHz
T_d	PWM delay	100	μs



(a)



(b)



(c)

Fig. 9. Locations of the dominant poles in z domain.
(a) 50 nH ≤ L_{fcl} ≤ 80 mH, R_{fcl} = 97.6 mΩ. (b) 5 mΩ ≤ R_{fcl} ≤ 1 Ω, L_{fcl} = 14.8 mH. (c) 0.05 ≤ λ ≤ 0.95, L_{fcl} = 14.8 mH and R_{fcl} = 97.6 mΩ.

IV. SIMULATION VALIDATIONS

In order to verify the proposed control diagram with VI-FCLs, a MATLAB/Simulink model comprised of three DGs is implemented. The system configuration is shown in Fig. 10 and the fault locations in different test cases are highlighted by using the circled numbers. Meanwhile, real-time HIL test is also conducted based on OPAL-RT platform. The system parameters are the same as those shown and Table I. It should be noted that the proposed method can be also used in practical applications. For practical implementation, the VI-FCL should be designed based on the real condition of power cable, acceptable fault current level, desired transient time for fault clearance, etc. Due to the present hardware limitations, only offline and real-time simulations are shown below for case studies.

Case I: Different Values of VI-FCLs

Different values of VI-FCLs are tested to study their impacts on fault current limiting and transient oscillation mitigation. As shown in Fig. 10, taking the fault at the PCC as an example, it occurs at t = 36 s and lasts for 0.2 s. The comparative study of different VI-FCLs is investigated in this test case. In the illustrative system, as shown in Table I, the length of the power cable for DG #2 and #3 is the same, while the length of the cable for DG #1 is longer. The waveforms of the RMS current for DG #1 and #2 and the system frequency are selected as examples.

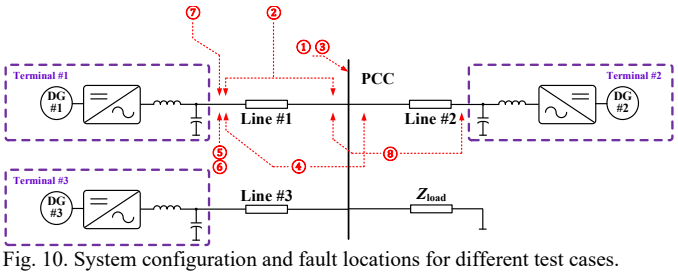


Fig. 10. System configuration and fault locations for different test cases.

Four parameters are defined to evaluate the effect of fault current limiting, i.e., ΔI_m, Δf_m, Δt_{si} and Δt_{sf}. Here, ΔI_m and Δf_m represent the maximum deviation of the RMS current and frequency compared to their normal values, and Δt_{si} and Δt_{sf} represent the response time during which the current and frequency return to their normal values.

It can be seen from Fig. 11 that the VI-FCLs are activated during faults. Different curves in Fig. 11 represent the results with different VI-FCLs. In particular, as shown in the results and legends in Fig. 11 (a), when the amplitude of the VI-FCL, namely $|Z_{fcl}|$, is selected as 0, 1.5 Ω and 9.2 Ω, respectively, ΔI_m is measured as 5.36 A, 4.01 A and 1.16 A. Meanwhile, for the waveforms of frequency shown in Fig. 11 (b), when $|Z_{fcl}|$ is selected as 0, 1.5 Ω and 9.2 Ω, Δf_m is shown as 0.33 Hz, 0.25 Hz and 0.21 Hz. Therefore, it is demonstrated that the VI-FCLs can be used to alleviate the fault current and mitigate the transient oscillations. Meanwhile, with larger $|Z_{fcl}|$, the transient over-shoot fault current is smaller.

Since the fault current is limited, the system can restore to the normal status in shorter adjustment time. As shown in the current waveform, when $|Z_{fcl}|$ changes, Δt_{si} is reduced, as shown as 10.4 s, 9 s and 6.1 s, respectively. In the meantime, as shown in the frequency waveform, Δt_{sf} is reduced as shown as 6.5 s, 5 s and 1.4 s.

As indicated in (5), a transient time t_{span} is involved to flexibly adjust the rising time of $|Z_{fcl}|$. Here, t_{span} is selected as 5 ms, as shown in Fig. 11 (c).

Case II: Fault Occurs at the DG Branch

As shown in Fig. 10, in this test case, the fault occurring at the branch of DG #1 is selected as an example. Both the faults near the DG unit and PCC are taken into account. As the same as Case I, the fault occurs at t = 36 s and lasts for 0.2 s. It should be noticed that the impact of the fault changes with different fault locations.

For the case with the fault near the DG unit, i.e., λ = 0.15, the waveforms of the RMS current of DG #1 and #2 are shown in Fig. 12 (a) and (b), respectively. It can be seen that although the fault occurs at the branch of DG #1, each DG unit contributes to the fault current. Meanwhile, the DG unit near the fault location delivers larger fault current. When activating the VI-FCL in each DG unit, the fault current and the transient oscillation can be significantly mitigated. In particular, for the RMS current of DG #1, ΔI_m is reduced from 43.2 A to 15.4 A and Δt_{si} is reduced from 17.7 s to 4.6 s. For the RMS current of DG #2, ΔI_m is reduced from 7.1 A to 1.65 A and Δt_{si} is reduced from 12.6 s to 3.8 s. The improvement of transient performance can be also clearly seen in the waveforms of the system frequency. As shown in Fig. 12 (c), large oscillations can be found in the frequency waveform when the VI-FCLs are not employed. When activating the VI-FCLs, large oscillations are removed. Meanwhile, Δf_m is reduced from 1 Hz to 0.29 Hz and Δt_{sf} is reduced from 13.6 s to 0.9 s.

For the case with the fault near the PCC, i.e., λ = 0.85, the waveforms of RMS current of DG #1 and #2 are shown in Fig. 13 (a) and (b), respectively. It can be seen that for the RMS current of DG #1, ΔI_m is reduced from 7.95 A to 2.96 A and Δt_{si} is reduced from 11.0 s to 3.4 s. For the RMS current of DG #2, ΔI_m is reduced from 5.82 A to 3.02 A and Δt_{si} is reduced from 5.2 s to 3.6 s. For the frequency waveform, as shown in Fig. 13 (c), Δf_m is reduced from 0.38 Hz to 0.22 Hz and Δt_{sf} is reduced from 6.4 s to 1.2 s.

Meanwhile, compared to the results of the case with the fault near the DG unit shown in Fig. 12 (a) – (c), it can be found that the proposed VI-FCLs can be used to suppress the fault current and transient oscillations in various cases with different fault locations.

Case III: Fault Occurs at the PCC

As shown in Fig. 10, the fault occurs at the PCC is studied. The effectiveness of VI-FCL during fault and in the post-fault procedure is discussed in detail in this test case. As same as Case I and II, the fault occurs at t = 36 s and lasts for 0.2 s. As shown in Fig. 14 (a), for DG branch #1, ΔI_m changes from 5.36 A to 1.16 A if activating the VI-FCLs, and Δt_{si} is reduced from 10.4 s to 6.1 s. Meanwhile, for DG branch #2, as shown in Fig. 14 (b), ΔI_m changes from 11.7 A to 4 A, and Δt_{si} reduces from 5.3 s to 4 s with VI-FCLs. It should be noted that the differences in the current and frequency waveforms for DG branch #1 and #2 are caused by different lengths of the power cables. For the frequency waveforms, as shown in Fig. 14 (c), large oscillations can be found without VI-FCLs. If activating the VI-FCLs, Δf_m is reduced from 0.33 Hz to 0.21 Hz, and the transient time Δt_{sf} is reduced from 6.5 s to 1.4 s.

Case IV: Multiple Fault Locations

As shown in Fig. 10, the system responses when multiple faults occur at different locations are shown in this case study. It is set that the faults occur at DG branch #1 and DG branch #2 simultaneously at t = 36 s and lasts for 0.2 s. In order to diversify the fault locations, the fault at DG branch #1 occurs near the DG unit, while the fault at DG branch #2 occurs near the PCC. As shown in Fig. 15 (a), for DG branch #1, ΔI_m changes from 30.9 A to 9.3 A with VI-FCLs activated, and Δt_{si} is reduced from 15.6 s to 4.7 s. Meanwhile, for DG branch #2, as shown in Fig. 15 (b), ΔI_m is reduced from 25.3 A to 7.1 A, and Δt_{si} reduces from 10.6 s to 3.8 s with VI-FCLs. For the system frequency, as shown in Fig. 15 (c), when activating the VI-FCLs, Δf_m is reduced from 0.94 Hz to 0.53 Hz, and the transient time Δt_{sf} is reduced from 13.8 s to 3.6 s.

Case V: Continuously Variable Load

The feasibility of the proposed method with continuously variable load is tested in this case study. In particular, the conventional impedance load is replaced by the variable load. The load current continuously changes during the whole simulation procedure, as shown in the current profile of the common load in normal condition in Fig. 16 (a). Meanwhile, as shown in Fig. 10, it is set that the fault at the DG branch #1 near the DG unit occurs at t = 36 s and lasts for 0.2 s. As

shown in Fig. 16 (b) – (d), when the fault occurs, compared to the value in normal condition, the maximum deviation of I_{rms1} is 52.5 A without VI-FCL, which is reduced to 16.4 A when the VI-FCL is activated. For DG branch #2, also compared to the value in normal condition, the maximum deviation of I_{rms2} is reduced from 15.6 A to 4.6 A with VI-FCL activated during the fault. At the same time, the maximum deviation of system frequency is reduced from 2.7 Hz to 2.0 Hz. It should be noted that since the load is continuously changed, the transient response time, i.e., Δt_{si} and Δt_{sf}, is not calculated. It can be also seen from Fig. 16 (d) that when VI-FCL is employed, the post-fault procedure is significantly improved with much lower oscillations.

Case VI: Rotating Machine Load

It should be pointed out that the proposed VI-FCL works with not only impedance load but also the other types of load. In this case study, a rotating machine load is employed as an example to test the feasibility of the proposed method in suppressing the amount of fault current. In particular, a three-phase asynchronous machine is used as the common load. The rated voltage and frequency are 110 V (rms) and 60 Hz, respectively. As shown in Fig. 10, it is set that the fault occurs at DG branch #1 near the DG unit at t = 36 s and lasts for 0.2 s.

It can be seen from Fig. 17 (a) that the maximum deviation of the torque ΔT_m is reduced from 15.6 Nm to 4.6 Nm when activating VI-FCL. Meanwhile, the transient time Δt_{sT} w/o VI-FCL is similar, which is approximately 0.6 s. For the rotor speed, as shown in Fig. 17 (b), its maximum deviation $\Delta\omega_m$ is reduced from 9.6 rad/s to 2.6 rad/s when activating VI-FCL, and the transient time $\Delta t_{s\omega}$ is reduced from 3.6 s to 1.7 s. Hence, it can be seen that the proposed method works for rotating machine load.

Case VII: Comparison with Conventional Current/Voltage Based Protection Schemes

Conventional protection schemes can be generally implemented by detecting the abnormal current or voltage. In order to identify the merits of the proposed VI-FCL based method, traditional current/voltage based protection schemes are implemented in this case study for comparison.

As shown in Fig. 10, it is set that the fault occurs at DG branch #1 near the DG unit at t = 36 s and lasts for 0.2 s. The responses with the conventional protection scheme based on current detection is shown in Fig. 18 (a) – (c). It can be seen that when I_{rms1} reaches its over-current threshold, the protective relay is activated to cut off the fault. Hence, I_{rms1} reduces to zero. Since the fault at DG branch #1 is isolated, the system returns to normal operation. Considering that DG branch #1 is cut off, the load is fed by DG branch #2 and #3. Therefore, I_{rms2} increases to 7.3 A. For the system frequency, it drops down to 59.84 Hz during the transient process and it gradually returns the rated value 60 Hz after the fault is isolated.

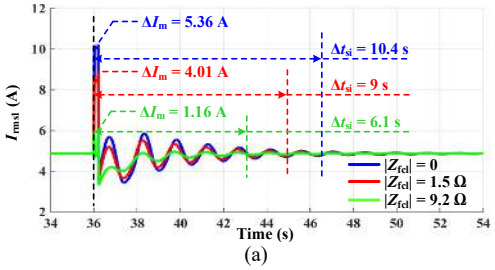
By setting the same fault condition, the responses with the conventional protection scheme based on voltage detection is shown in Fig. 19 (a) – (c). It can be seen that when V_{rms1} reduces to its low-voltage threshold, the protective relay is activated to cut off the fault and the interface inverter for DG #1 stops working. Hence, V_{rms1} reduces to zero. Meanwhile, since the fault is isolated, the system returns to normal operation. In particular, V_{rms2} reaches 149.5 V after the transient deviation induced by the fault, and the frequency is gradually returned from 59.84 Hz to the rated value 60 Hz.

It should be noted that although the conventional current/voltage based protection schemes can effectively isolate the fault and make the system return to normal operation. It must be noticed that the DG branch with fault is cut off. Even though it can be reconnected when the fault is cleared, unavoidable resynchronization algorithm should be implemented during reconnection. This resynchronization may involve some additional stability and power quality issues. The proposed VI-FCL based fault ride through method is implemented without interrupting the connectivity of DG units. Hence, no complicated resynchronization is needed.

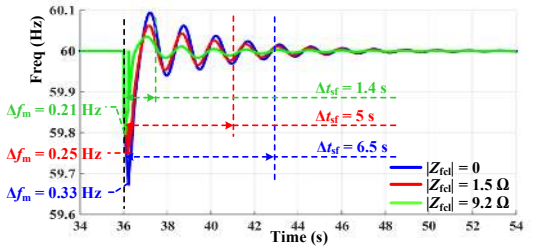
Case VIII: Real-Time Hardware-in-the-Loop Simulation Test

In order to further verify the feasibility of the proposed VI-FCL, real-time HIL test is conducted. In particular, a real-time simulation environment is implemented based on OPAL-RT platform, which can be regarded as a semi-hardware platform where the AC microgrids with DG interface inverters and line impedances are modeled in the real-time environment in OPAL-RT while real hardware controllers are used to test the proposed method. Meanwhile, the whole test procedure is done in real-time. The system configuration of the real-time HIL test platform is shown in Fig. 20.

Compared to the conventional off-line simulation test based on MATLAB/Simulink, the real-time HIL demonstration based on OPAL-RT features the enhanced test capability. Hence, the longer time test case can be verified. As shown in Fig. 10, during the whole test procedure, at t = 40 s, 80 s and 120 s, the fault occurs at different locations, and each fault lasts for 0.2 s. At t = 40 s, the fault near PCC occurs at DG branch #1, and at t = 80 s, the fault near DG unit occurs at DG branch #2. Finally, at t = 120 s, multiple faults occur simultaneously at DG branch #1 near PCC and DG branch #2 near DG unit. It can be seen from Fig. 21 (a) – (c) that with the proposed VI-FCLs, the fault current at different fault locations can be effectively suppressed. Meanwhile, the oscillation in the post-fault procedure can be significantly improved.



(a)



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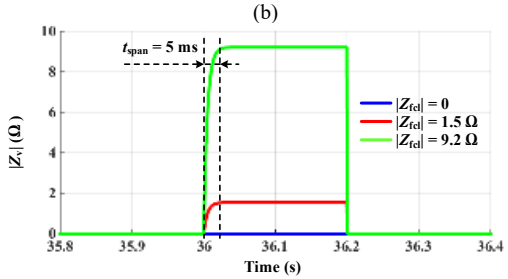
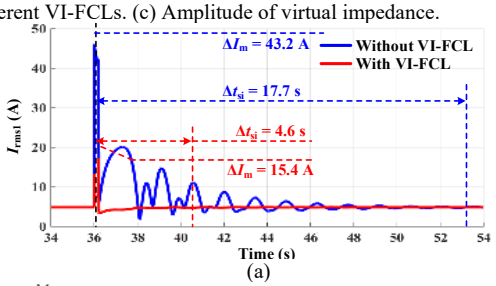


(c)

Fig. 11. Fault responses with different VI-FCLs.
(a) RMS current waveform with different VI-FCLs. (b) Frequency waveform with different VI-FCLs. (c) Amplitude of virtual impedance.



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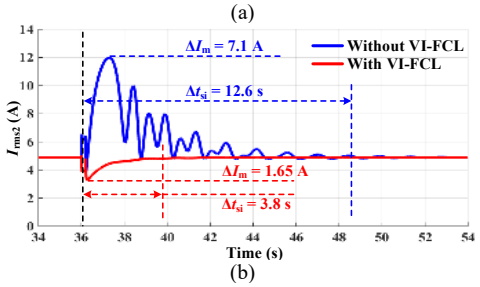

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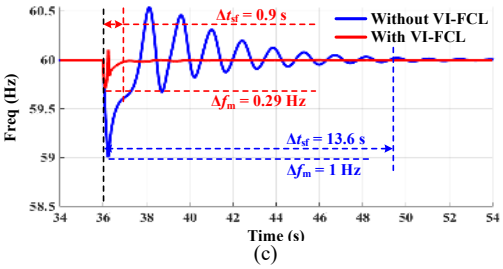
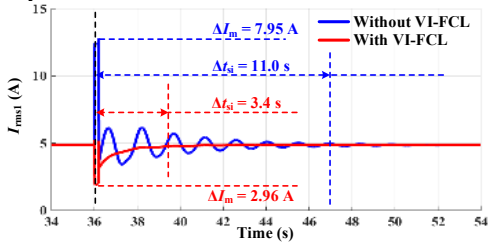
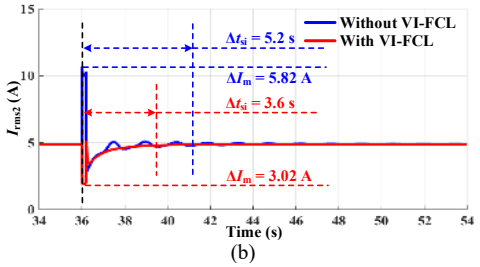


(c)

Fig. 12. Reponses with the fault occurring at the DG branch (near DG unit).
(a) RMS current waveform of DG #1. (b) RMS current waveform of DG #2. (c) Frequency waveform.



(a)



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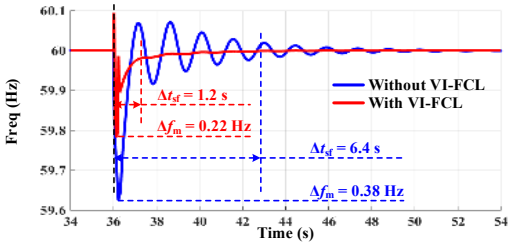
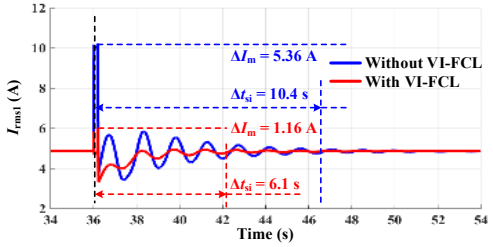


(c)

Fig. 13. Reponses with the fault occurring at the DG branch (near PCC).
(a) RMS current waveform of DG branch #1. (b) RMS current waveform of DG branch #2. (c) Frequency waveform.



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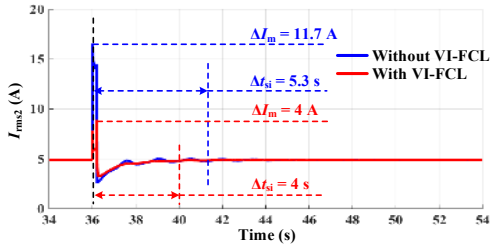

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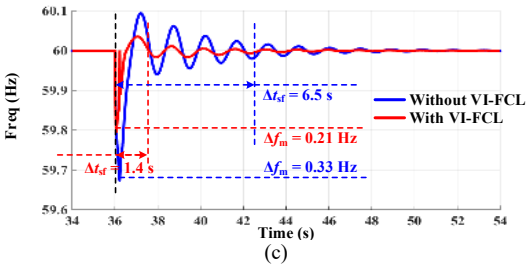
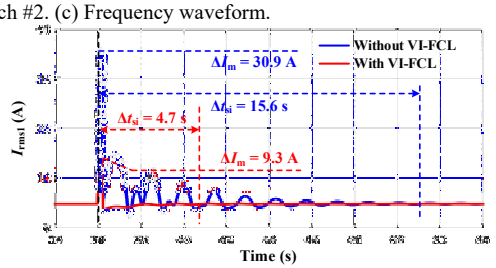


(c)

Fig. 14. Reponses with the fault occurring at the PCC.
(a) RMS current waveform of DG branch #1. (b) RMS current waveform of DG branch #2. (c) Frequency waveform.



(a)

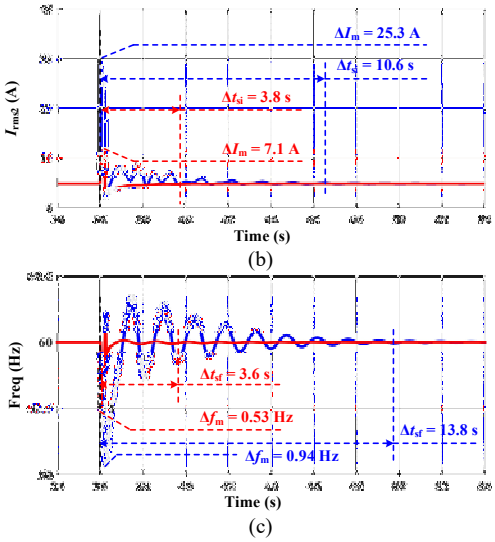


Fig. 15. Responses with the faults occurring in DG branch #1 and #2 simultaneously.
(a) RMS current waveform of DG branch #1. (b) RMS current waveform of DG branch #2. (c) Frequency waveform.

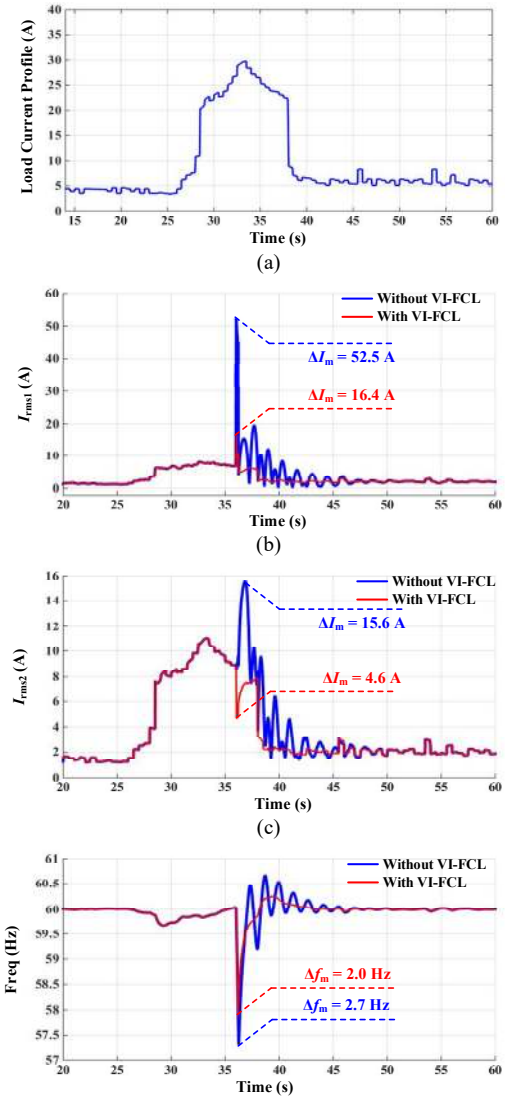


Fig. 16. Responses with continuously variable load.
(a) Current profile of the common load. (b) RMS current waveform of DG branch #1. (c) RMS current waveform of DG branch #2. (d) Frequency waveform.

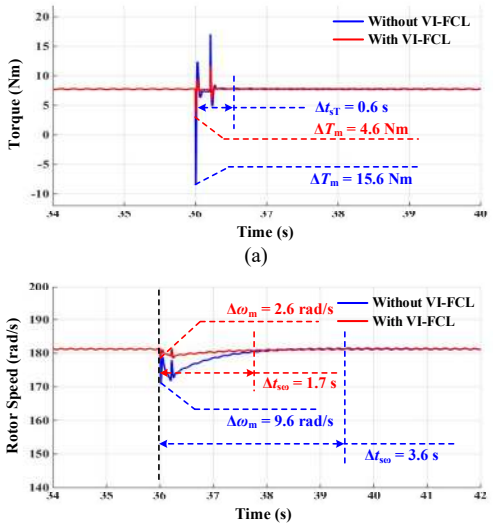


Fig. 17. Responses with rotating machine load.
(a) Torque waveform. (b) Rotor speed waveform.

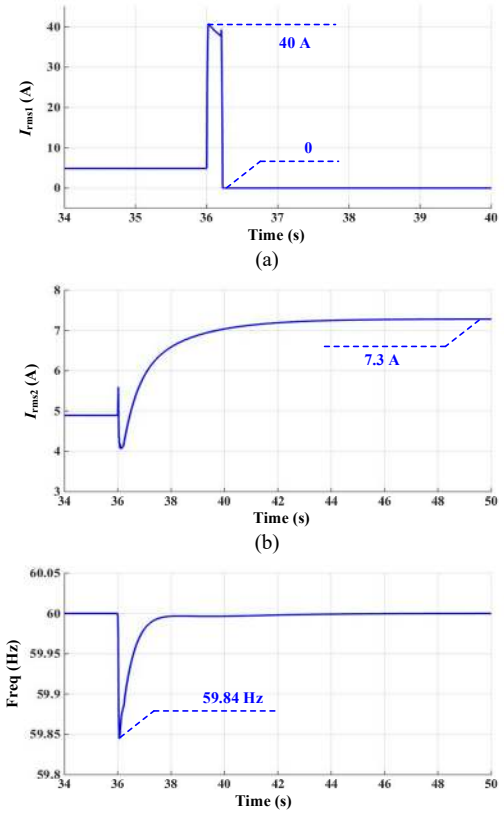
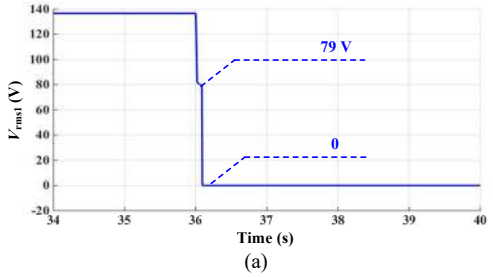
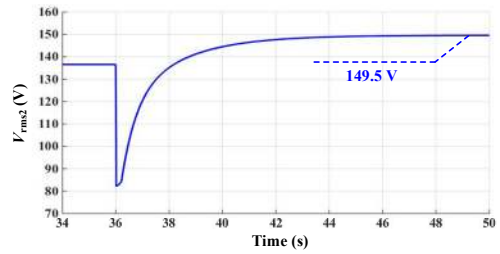
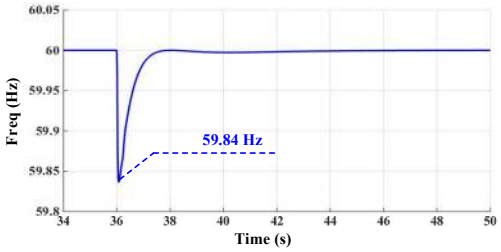


Fig. 18. Responses of conventional current based protection scheme.
(a) RMS current waveform of DG branch #1. (b) RMS current waveform of DG branch #2. (c) Frequency waveform.





(b)



(c)

Fig. 19. Responses of conventional voltage based protection scheme.
(a) RMS voltage waveform of DG branch #1. (b) RMS voltage waveform of DG branch #2. (c) Frequency waveform.

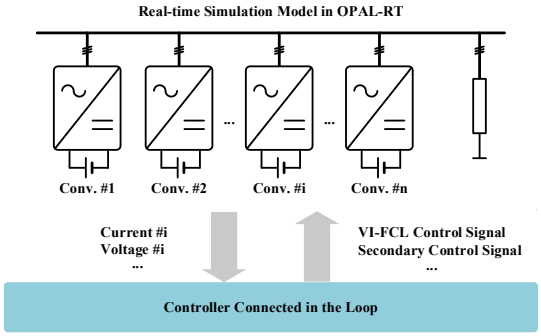
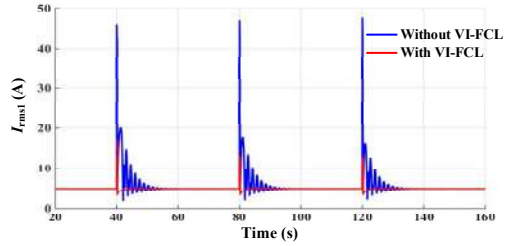
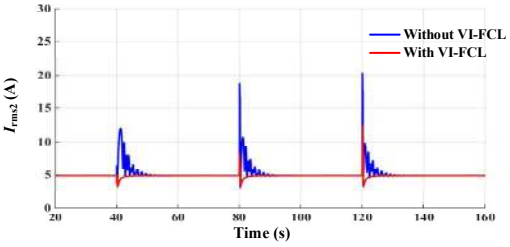


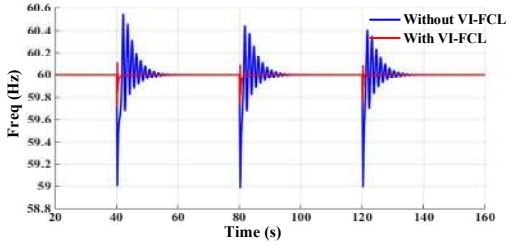
Fig. 20. Configuration of real-time HIL test platform.



(a)



(b)



(c)

Fig. 21. Responses of real-time HIL test.
(a) RMS voltage waveform of DG branch #1. (b) RMS voltage waveform of DG branch #2. (c) Frequency waveform.

V. Conclusion

In order to alleviate the impact of the large fault current in inverter dominated AC microgrids, VI-FCLs are proposed to suppress the amount of current flowing through the system and mitigate the oscillation during faults and in the post-fault restoration process. The VI-FCLs are embedded in the control diagram of each DG inverters. Hence, it is a low-cost approach that is implemented without additional hardware devices. Furthermore, the impedance model of AC microgrids during faults is derived with the consideration of VI-FCLs, and the impact of the parameters of VI-FCLs on system stability is analyzed. Meanwhile, it is demonstrated that by using the proposed VI-FCLs, the large fault current can be reduced and the oscillations for different fault locations can be significantly eliminated.

References

[1] S. Chowdhury and P. Crossley, *Microgrids and Active Distribution Networks*. Stevenage: The Institution of Engineering and Technology, 2009.

[2] A. O. Converse, "Seasonal Energy Storage in a Renewable Energy System," *Proc. IEEE*, vol. 100, no. 2, pp. 401–409, Feb. 2012.

[3] L. Che, M. E. Khodayar, and M. Shahidehpour, "Adaptive Protection System for Microgrids: Protection practices of a functional microgrid system.," *IEEE Electrif. Mag.*, vol. 2, no. 1, pp. 66–80, Mar. 2014.

[4] R. H. Lasseter, "MicroGrids," in *IEEE Power Engineering Society Winter Meeting. Conference Proceedings*, 2002, vol. 1, pp. 305–308.

[5] F. Blaabjerg, Z. Chen, and S. B. Kjaer, "Power Electronics as Efficient Interface in Dispersed Power Generation Syst.," *IEEE Trans. Power Electron.*, vol. 19, no. 5, pp. 1184–1194, 2004.

[6] J. M. Carrasco, L. G. Franquelo, J. T. Bialasiewicz, E. Galvan, R. C. P. Guisado, M. A. M. Prats, J. I. Leon, and N. Moreno-Alfonso, "Power-Electronic Systems for the Grid Integration of Renewable Energy Sources: A Survey," *IEEE Trans. Ind. Electron.*, vol. 53, no. 4, pp. 1002–1016, 2006.

[7] J. Rajagopalan, K. Xing, Y. Guo, F. C. Lee, and B. Manners, "Modeling and Dynamic Analysis of Paralleled DC/DC Converters with Master-Slave Current Sharing Control," in *IEEE Applied Power Electronics Conference and Exposition,* 1996, vol. 2, pp. 678–684.

[8] T.-F. Wu, Y.-K. Chen, and Y.-H. Huang, "3C Strategy for Inverters in Parallel Operation Achieving an Equal Current Distribution," *IEEE Trans. Ind. Electron.*, vol. 47, no. 2, pp. 273–281, Apr. 2000.

[9] X. Sun, Y.-S. Lee, and D. Xu, "Modeling, Analysis, and Implementation of Parallel Multi-Inverter Systems with Instantaneous Average-Current-Sharing Scheme," *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 844–856, May 2003.

[10] Y. W. Li and C.-N. Kao, "An Accurate Power Control Strategy for Power-Electronics-Interfaced Distributed Generation Units Operating in a Low-Voltage Multibus Microgrid," *IEEE Trans. Power Electron.*, vol. 24, no. 12, pp. 2977–2988, Dec. 2009.

[11] N. Pogaku, M. Prodanovic, and T. C. Green, "Modeling, Analysis and Testing of Autonomous Operation of an Inverter-Based Microgrid," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 613–625, 2007.

[12] Q.-C. Zhong, "Robust Droop Controller for Accurate Proportional Load Sharing Among Inverters Operated in Parallel," *IEEE Trans. Ind. Electron.*, vol. 60, no. 4, pp. 1281–1290, 2013.

[13] J. M. Guerrero, M. Castilla, J. C. Vasquez, J. Matas, and L. G. de Vicuna, "Control Strategy for Flexible Microgrid Based on Parallel Line-Interactive UPS Systems," *IEEE Trans. Ind. Electron.*, vol. 56, no. 3, pp. 726–736, 2009.

[14] J. M. Guerrero, J. C. Vasquez, J. Matas, L. G. de Vicuna, and M. Castilla, "Hierarchical Control of Droop-Controlled AC and DC Microgrids-A General Approach Toward Standardization," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 158–172, 2011.

[15] A. H. Etemadi and R. Iravani, "Overcurrent and Overload Protection of Directly Voltage-Controlled Distributed Resources in a Microgrid," *IEEE Trans. Ind. Electron.*, vol. 60, no. 12, pp. 5629–5638, Dec. 2013.

[16] M. A. Zamani, A. Yazdani, and T. S. Sidhu, "A Control Strategy for Enhanced Operation of Inverter-Based Microgrids Under Transient

Disturbances and Network Faults," *IEEE Trans. Power Deliv.*, vol. 27, no. 4, pp. 1737–1747, Oct. 2012.

[17] C. A. Plet, M. Graovac, T. C. Green, and R. Iravani, "Fault Response of Grid-Connected Inverter Dominated Networks," in *IEEE Power and Energy Society General Meeting*, 2010, pp. 1–8.

[18] J. Bloemink and M. R. Iravani, "Control of a Multiple Source Microgrid With Built-in Islanding Detection and Current Limiting," *IEEE Trans. Power Deliv.*, vol. 27, no. 4, pp. 2122–2132, Oct. 2012.

[19] E. Sortomme, S. S. Venkata, and J. Mitra, "Microgrid Protection Using Communication-Assisted Digital Relays," *IEEE Trans. Power Deliv.*, vol. 25, no. 4, pp. 2789–2796, Oct. 2010.

[20] "Fault Current Limiters - U.S. Department of Energy," 2009. [Online]. Available: http://energy.gov/sites/prod/files/oeprod/DocumentsandMedia/hts_fcl_110609.pdf.

[21] Y. W. Li, D. M. Vilathgamuwa, P. C. Loh, and F. Blaabjerg, "A Dual-Functional Medium Voltage Level DVR to Limit Downstream Fault Currents," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1330–1340, Jul. 2007.

[22] D. M. Vilathgamuwa, P. C. Loh, and Y. Li, "Protection of Microgrids During Utility Voltage Sags," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1427–1436, Oct. 2006.

[23] M. Hojo, Y. Fujimura, T. Ohnishi, and T. Funabashi, "An Operating Mode of Voltage Source Inverter for Fault Current Limitation," in *Universities Power Engineering Conference*, 2006, vol. 2, pp. 598–602.

[24] T. Ghanbari and E. Farjah, "Unidirectional Fault Current Limiter: An Efficient Interface Between the Microgrid and Main Network," *IEEE Trans. Power Syst.*, vol. 28, no. 2, pp. 1591–1598, May 2013.

[25] G. Didier and J. Lévêque, "Influence of Fault Type on the Optimal Location of Superconducting Fault Current Limiter in Electrical Power Grid," *Int. J. Electr. Power Energy Syst.*, vol. 56, pp. 279–285, 2014.

[26] J.-S. Hwang, U. A. Khan, W.-J. Shin, J.-K. Seong, J.-G. Lee, Y.-H. Kim, and B.-W. Lee, "Validity Analysis on the Positioning of Superconducting Fault Current Limiter in Neighboring AC and DC Microgrid," *IEEE Trans. Appl. Supercond.*, vol. 23, no. 3, Jun. 2013.

[27] W.-S. Moon, J.-N. Won, J.-S. Huh, and J.-C. Kim, "A Study on the Application of a Superconducting Fault Current Limiter for Energy Storage Protection in a Power Distribution System," *IEEE Trans. Appl. Supercond.*, vol. 23, no. 3, Jun. 2013.

[28] W. K. A. Najy, H. H. Zeineldin, and W. L. Woon, "Optimal Protection Coordination for Microgrids With Grid-Connected and Islanded Capability," *IEEE Trans. Ind. Electron.*, vol. 60, no. 4, pp. 1668–1677, 2013.

[29] J. M. Guerrero, L. GarciadeVicuna, J. Matas, M. Castilla, and J. Miret, "Output Impedance Design of Parallel-Connected UPS Inverters With Wireless Load-Sharing Control," *IEEE Trans. Ind. Electron.*, vol. 52, no. 4, pp. 1126–1135, 2005.

[30] J. C. Vasquez, J. M. Guerrero, M. Savaghebi, J. Eloy-Garcia, and R. Teodorescu, "Modeling, Analysis, and Design of Stationary-Reference-Frame Droop-Controlled Parallel Three-Phase Voltage Source Inverters," *IEEE Trans. Ind. Electron.*, vol. 60, no. 4, pp. 1271–1280, Apr. 2013.

[31] J. He, Y. W. Li, D. Bosnjak, and B. Harris, "Investigation and Active Damping of Multiple Resonances in a Parallel-Inverter-Based Microgrid," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 234–246, Jan. 2013.

[32] J. He and Y. W. Li, "Hybrid Voltage and Current Control Approach for DG-Grid Interfacing Converters With LCL filters," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1797–1809, May 2013.

[33] V. Blasko and V. Kaura, "A New Mathematical Model and Control of a Three-Phase AC-DC Voltage Source Converter," *IEEE Trans. Power Electron.*, vol. 12, no. 1, pp. 116–123, 1997.

[34] "Industrial/Ph.D. Course: AC Microgrids in Theory and Practice." [Online]. Available: https://building-microgrid.lbl.gov/sites/all/files/ACMGCourse.pdf.

[35] R. Teodorescu, M. Liserre, and P. Rodriguez, *Grid Converters for Photovoltaic and Wind Power Syst.* Wiley, 2011.

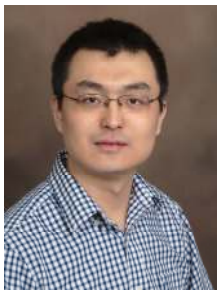
[36] R. Teodorescu, F. Blaabjerg, M. Liserre, and P. C. Loh, "Proportional-Resonant Controllers and Filters for Grid-Connected Voltage-Source Converters," *IEE Proc. Electr. Power Appl.*, vol. 153, no. 5, pp. 750–762, 2006.

[37] D. N. Zmood and D. G. Holmes, "Stationary Frame Current Regulation of PWM Inverters with Zero Steady-State Error," *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 814–822, May 2003.

[38] E. Twining and D. G. Holmes, "Grid Current Regulation of a Three-Phase Voltage Source Inverter with an LCL Input Filter," *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 888–895, May 2003.

[39] A. G. Yepes, F. D. Freijedo, J. Doval-Gandoy, Ó. López, J. Malvar, and P. Fernandez-Comesaña, "Effects of Discretization Methods on the Performance of Resonant Controllers," *IEEE Trans. Power Electron.*, vol. 25, no. 7, pp. 1692–1712, Jul. 2010.

[40] A. Vidal, F. D. Freijedo, A. G. Yepes, P. Fernandez-Comesana, J. Malvar, Ó. Lopez, and J. Doval-Gandoy, "Assessment and Optimization of the Transient Response of Proportional-Resonant Current Controllers for Distributed Power Generation Systems," *IEEE Trans. Ind. Electron.*, vol. 60, no. 4, pp. 1367–1383, Apr. 2013.



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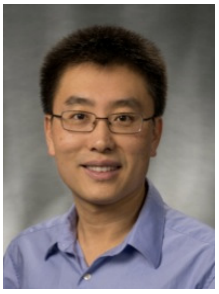

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