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Lu, Xiaonan; Sun, Kai; Huang, Lipei; Guerrero, Josep M.; Vasquez, Juan Carlos; Xing, Yan

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Virtual Impedance Based Stability Improvement for DC Microgrids with Constant Power Loads

Xiaonan Lu
Department of Electrical Engineering & Computer Science
University of Tennessee
Knoxville, TN, US
Email: xlu13@utk.edu

Kai Sun, Lipei Huang
Department of Electrical Engineering
Tsinghua University
Beijing, China

Josep M. Guerrero, Juan C. Vasquez
Department of Energy Technology
Aalborg University
Aalborg, Denmark

Yan Xing
Jiangsu Key Lab of New Energy and Power Conversion
Nanjing University of Aeronautics and Astronautics
Nanjing, China

***Abstract*—DC microgrid provides an efficient way to integrate different kinds of renewable energy sources with DC couplings. In this paper, in order to improve the stability of DC microgrids with constant power loads (CPLs), a virtual impedance based method is proposed. The CPLs have inherent instability issues induced by negative incremental impedances. This negative impedance makes the system poorly damped and the stability is thereby degraded. To enhance the system stability, virtual impedance based stabilizer comprised of series-connected inductance and resistance is employed. In particular, two types of stabilizers are used. Type I stabilizer locates at the output capacitor branch, and Type II stabilizer locates at the output inductance branch. Meanwhile, considering that the parallel interfacing converters are commonly in parallel in a microgrid, droop control is taken into account here. To validate the stability with the above stabilizers in a DC microgrid with parallel interfacing converters and CPL, the impedance matching approach is employed. The output impedance of the source converter and input impedance of the load are calculated respectively, and the influence of droop control, negative incremental impedance of CPL, proposed stabilizers are considered in the calculation of the impedance. It is demonstrated that with the proposed stabilizers, the instable poles can be moved to the stable region in the frequency domain. Simulation model with three interfacing converters is implemented based on MATLAB/Simulink to verify the proposed method.**

I. INTRODUCTION

With the increasing penetration of renewable energy into modern electric grid, the concept of microgrid was proposed several years ago and has been intensively studied recently [1]. Considering the AC nature of the conventional power system, most of the research is focused on AC microgrids [2]-[5]. In order to integrate various renewable energy sources with dc couplings, the solution of dc microgrids has become an attracting approach [6]-[11]. In both AC and DC microgrid, the renewable energy sources are connected to the common bus by using the interfacing converters. Considering the distributed configuration of the system, the power electronics interfacing converters are usually connected in parallel. In order to obtain proper load power sharing among different sources, droop control as a decentralized method is commonly employed in the control diagram of the interfacing converters [1]-[8].

Stability problems should be noticed in order to enhance the performance of a dc microgrid. Especially in the system with constant-power loads (CPLs), the stability issues are required to be further studied [12]-[14]. In a microgrid, the CPLs, also known as active loads, enable the power conditioning at the load side. Different from the passive loads, e.g. incandescent lighting and resistive heaters, the CPLs consume constant amount of power regardless what the input voltage is [14]. The impact of CPLs on the system stability is induced by its negative incremental impedance. The negative impedance makes the system poorly damped and can employ unstable poles into the control system [12]-[14]. The existing methods to deal with the above problem are mainly focused on single interfacing converter. However, in a practical microgrid, multiple interfacing converters usually coexist and are connected in parallel. Hence, it is necessary to extend the research on CPL and its damping method to the multiple converter system. Meanwhile, the commonly used droop control should be taken into account when discussing the stabilization of the microgrid with CPLs.

Virtual impedances are commonly employed in the control diagram of the interfacing converters to achieve the functionalities of matching the output impedance at the base or harmonic frequencies [15] and resonance damping [16]. In this paper, the virtual impedance based stabilization of dc microgrids with CPLs is proposed. The virtual impedance used here is comprised of series-connected resistance and inductance. Two types of stabilizers are employed. One is based on capacitor voltage feedback, and the other is based on inductance current feedback. The detailed model of the control system, including droop control for load power sharing and inherent negative incremental impedance of

CPL, are studied. The output impedance of interfacing converter (Z_o) and the load impedance of CPL (Z_{load}) are calculated. By using the judging principle of impedance matching [17], the stability of the control system is analyzed. Particularly, the dominant poles of $(1+Z_o/Z_{load})^{-1}$ are obtained and tested. If and only if all of the poles are located on the left half of s plane, the system is stable. The unstable poles in the s domain can be found without the virtual impedance based stabilization. After activating the proposed virtual impedance based method, the unstable poles are forced to move into the stable region. Hence, the system stability of dc microgrid with CPL can be guaranteed.

II. Modeling of the System with the Proposed Stabilizers Based on Virtual Impedance

The incremental impedance of the CPL can be calculated as follows [12]:

$$\frac{\partial v_{\text{load}}}{\partial i_{\text{load}}}\Big|_{(V_{\text{load}},I_{\text{load}})} = \frac{\partial}{\partial i_{\text{load}}}\left(\frac{P_{\text{load}}}{i_{\text{load}}}\right)\Big|_{(V_{\text{load}},I_{\text{load}})} = -\frac{V_{\text{load}}}{I_{\text{load}}} < 0 \tag{1}$$

where v_{load}, i_{load} and p_{load} are the load voltage, current and power, respectively.

It is seen from (1) that the CPL has negative incremental impedance, which will make the system poorly damped and influence the system stability.

The system configuration and the control diagram for parallel interfacing converters are shown in Fig. 1. First, the system without the stabilizers is analyzed as follows. For converter #i (i = 1, 2, …, n), it is derived that

$$V_{\text{pi}} = sLI_{\text{Li}} + I_{\text{Li}}r_{\text{L}} + V_{\text{oi}},\ sCV_{\text{oi}} = I_{\text{Li}} - I_{\text{oi}} \tag{2}$$

$$I_{\text{Li}}^{*} = G_{\text{piv}}\cdot(V_{\text{oi}}^{*} - V_{\text{oi}} - m_{\text{i}}G_{\text{lpf}}P_{\text{oi}}),\ V_{\text{pi}} = G_{\text{pic}}\cdot(I_{\text{Li}}^{*} - I_{\text{Li}}) \tag{3}$$

where G_{piv} and G_{pic} are the PI controllers of the capacitor voltage and inductance current, V_{pi} is the inverter output voltage, V_{oi}^{*} and I_{Li}^{*} are the reference values of capacitor voltage and inductance current, m_{i} is the droop coefficient, and G_{lpf} is the low-pass filter (LPF) used in droop control.

Perturbing (2), the small signal model is derived as follows:

$$\hat{V}_{\text{pi}} = sL\hat{I}_{\text{Li}} + \hat{I}_{\text{Li}}r_{\text{L}} + \hat{V}_{\text{oi}},\ sC\hat{V}_{\text{oi}} = \hat{I}_{\text{Li}} - \hat{I}_{\text{oi}} \tag{4}$$

Meanwhile, for the output power of the interfacing converter, the following relationship and its small signal expression can be reached:

$$p_{\text{oi}} = v_{\text{oi}}\cdot i_{\text{oi}} \tag{5}$$

$$\hat{p}_{\text{oi}} = V_{\text{oi}}\cdot\hat{i}_{\text{oi}} + I_{\text{oi}}\cdot\hat{v}_{\text{oi}} \tag{6}$$

Converting (6) into the frequency domain and then combining the result and the perturbed results of (3), it is obtained:

$$\hat{I}_{\text{Li}}^{*} = -G_{\text{piv}}\cdot(\hat{V}_{\text{oi}} + m_{\text{i}}G_{\text{lpf}}V_{\text{oi}}\hat{I}_{\text{oi}} + m_{\text{i}}G_{\text{lpf}}I_{\text{oi}}\hat{V}_{\text{oi}}),\ \hat{V}_{\text{pi}} = G_{\text{pic}}\cdot(\hat{I}_{\text{Li}}^{*} - \hat{I}_{\text{Li}}) \tag{7}$$

Combining (4) and (7), the output impedance of converter #i can be calculated as

$$Z_{\text{oi}} = \frac{G_{\text{pic}}(1 + m_{\text{i}}G_{\text{piv}}G_{\text{lpf}}V_{\text{oi}}) + sL + r_{\text{L}}}{1 + sC(sL + r_{\text{L}}) + sCG_{\text{pic}} + G_{\text{pic}}G_{\text{piv}}(1 + m_{\text{i}}G_{\text{lpf}}I_{\text{oi}})} \tag{8}$$

Since parallel interfacing converters are taken into account, the output impedance of each converter can be merged. Assuming that the parameters of each converter are the same, it is derived that the equivalent output impedance of the parallel interfacing converters is

$$Z_{\text{oeq}} = \frac{Z_{\text{oi}}}{\text{n}} = \frac{G_{\text{pic}}(1 + m_{\text{i}}G_{\text{piv}}G_{\text{lpf}}V_{\text{oi}}) + sL + r_{\text{L}}}{\text{n}\cdot[1 + sC(sL + r_{\text{L}}) + sCG_{\text{pic}} + G_{\text{pic}}G_{\text{piv}}(1 + m_{\text{i}}G_{\text{lpf}}I_{\text{oi}})]} \tag{9}$$

The above is the derivation for the converter side. For the load side, considering the constant power nature, the incremental impedance is shown in (1), namely

$$Z_{\text{load}} = -\frac{V_{\text{load}}}{I_{\text{load}}} = -\frac{V_{\text{oi}}}{\text{n}I_{\text{oi}}} \tag{10}$$

In order to test the system stability, the principle of impedance matching is employed. Particularly, all of the dominant poles of $(1+Z_{\text{oeq}}/Z_{\text{load}})^{-1}$ should be located in the stable region [17]. By using the Tustin bilinear transform, (9) and (10) can be discretized from s domain to z domain, and the dominant poles of $(1+Z_{\text{oeq}}/Z_{\text{load}})^{-1}$ can be reached. Due to the influence of negative incremental impedance, the unstable dominant poles appear when no damping method is employed. In the certain system which is under test, the unstable poles p_1 and p_2 are 0.96 ± j0.32 ($|p_1| = |p_2| = 1.012 > 1$), which locate outside the unit circle.

III. Proposed Virtual Impedance Based Stabilizer

In order to make the unstable poles move into the stable region, the virtual impedance based stabilizer is proposed. The virtual impedance used here is comprised of series-connected virtual resistance and inductance. Particularly, two types of stabilizers are employed, as shown in Fig. 1. Type I stabilizer is realized by capacitor voltage feedback, and Type II stabilizer is realized by inductance current feedback. The effect of the virtual impedance based stabilizer on system stability is analyzed below.

When considering the two types of virtual impedance based stabilizers in the control diagram in Fig. 1, (3) is modified as

$$\begin{aligned} I_{\text{Li}}^{*} &= G_{\text{piv}}\cdot(V_{\text{oi}}^{*} - V_{\text{oi}} - m_{\text{i}}G_{\text{lpf}}P_{\text{oi}}) \\ V_{\text{pi}} &= G_{\text{pic}}\cdot(I_{\text{Li}}^{*} - I_{\text{Li}}) - k_1\cdot G_{\text{dc}}Z_{\text{dc}}V_{\text{oi}} - k_2\cdot Z_{\text{dc}}I_{\text{Li}} \end{aligned} \tag{11}$$

where k_1 and k_2 represent the type of stabilizer, and the value of (k_1, k_2) can be only (1, 0) or (0, 1). When k_1 equals 1 and k_2 equals 0, Type I stabilizer is selected. When k_1 equals 0 and k_2 equals 1, Type II stabilizer is selected.

Meanwhile, G_{dc} and Z_{dc} are shown as:

$$G_{\text{dc}} = \frac{I_{\text{Ci}}}{V_{\text{oi}}} = sC,\ Z_{\text{dc}} = sL_{\text{dc}} + R_{\text{dc}} \tag{12}$$

where L_{dc} is the virtual inductance, and the R_{dc} is the virtual resistance.

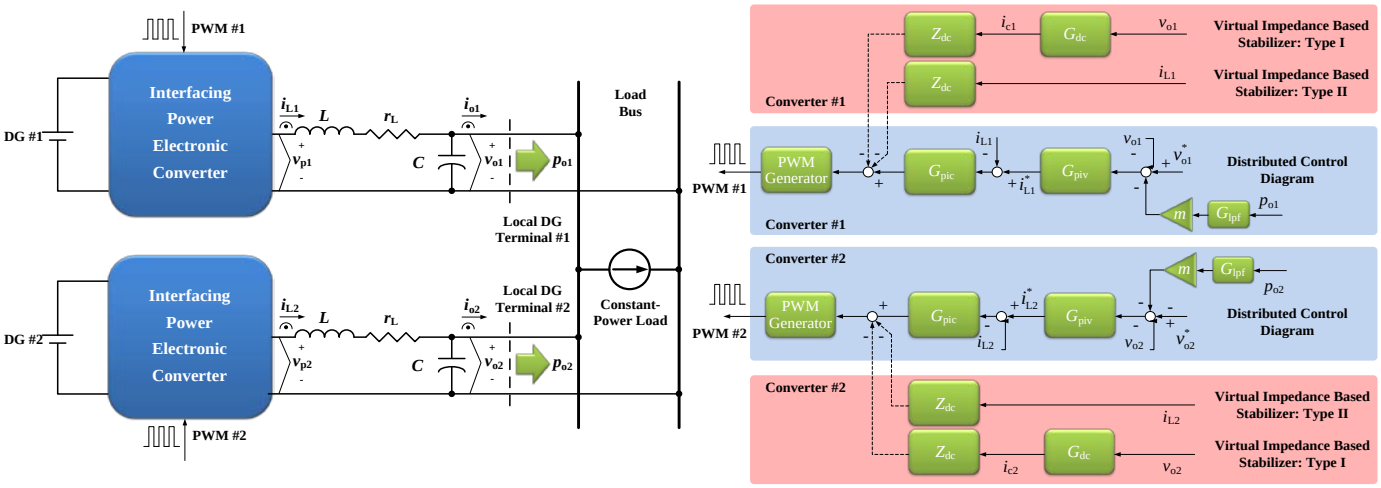

Fig. 1. System configuration and control diagram for parallel interfacing converters considering the virtual impedance based stabilizers.

Perturbing (11), it yields

$$\hat{I}_{\mathrm{Li}}^{*} = -G_{\mathrm{piv}} \cdot (\hat{V}_{\mathrm{oi}} + m_{\mathrm{i}} G_{\mathrm{lpf}} V_{\mathrm{oi}} \hat{I}_{\mathrm{oi}} + m_{\mathrm{i}} G_{\mathrm{lpf}} I_{\mathrm{oi}} \hat{V}_{\mathrm{oi}}) \qquad (13)$$

$$\hat{V}_{\mathrm{pi}} = G_{\mathrm{pic}} \cdot (\hat{I}_{\mathrm{Li}}^{*} - \hat{I}_{\mathrm{Li}}) - k_1 \cdot G_{\mathrm{dc}} Z_{\mathrm{dc}} \hat{V}_{\mathrm{oi}} - k_2 \cdot Z_{\mathrm{dc}} \hat{I}_{\mathrm{Li}}$$

Combining (4) and (13), it is derived that

$$Z_{\mathrm{oi}}^{'} = \frac{G_{\mathrm{pic}}(1 + m_{\mathrm{i}} G_{\mathrm{piv}} G_{\mathrm{lpf}} V_{\mathrm{oi}}) + sL + r_{\mathrm{L}} + k_2 Z_{\mathrm{dc}}}{1 + sC(sL + r_{\mathrm{L}}) + sCG_{\mathrm{pic}} + G_{\mathrm{pic}} G_{\mathrm{piv}}(1 + m_{\mathrm{i}} G_{\mathrm{lpf}} I_{\mathrm{oi}}) + (k_1 + k_2) G_{\mathrm{dc}} Z_{\mathrm{dc}}}$$

Similar to the analysis in Section II, if merging the output impedance of the parallel interfacing converters and noticing that $k_1 + k_2 \equiv 1$,

$$Z_{\mathrm{oeq}}^{'} = \frac{G_{\mathrm{pic}}(1 + m_{\mathrm{i}} G_{\mathrm{piv}} G_{\mathrm{lpf}} V_{\mathrm{oi}}) + sL + r_{\mathrm{L}} + k_2 Z_{\mathrm{dc}}}{\mathrm{n} \cdot [1 + sC(sL + r_{\mathrm{L}}) + sCG_{\mathrm{pic}} + G_{\mathrm{pic}} G_{\mathrm{piv}}(1 + m_{\mathrm{i}} G_{\mathrm{lpf}} I_{\mathrm{oi}}) + (k_1 + k_2) G_{\mathrm{dc}} Z_{\mathrm{dc}}]}$$

Hence, by discretizing the transfer functions, the dominant poles of $(1+Z'_{\mathrm{oeq}}/Z_{\mathrm{load}})^{-1}$ can be obtained. The system parameters are shown in Table I. Assuming three interfacing converters are used, by using the principle of impedance matching, the stability of the control system with virtual impedance based stabilizer is verified. As shown in Fig. 2, when changing the value of the virtual inductance and resistance, the dominant poles are gradually moved to the stable region.

TABLE I
System Parameters

Item	Symbol	Value	Unit
Input Voltage	v_{in}	200	V
Reference of Output Voltage	v_{oref}	600	V
Output Inductance	L	5	mH
Parasitic Resistance of Output Inductance	r_{L}	0.06	Ω
Output capacitor	C	20	μF
Number of Converters	n	3	-
Sampling Time	T_{s}	100	μs

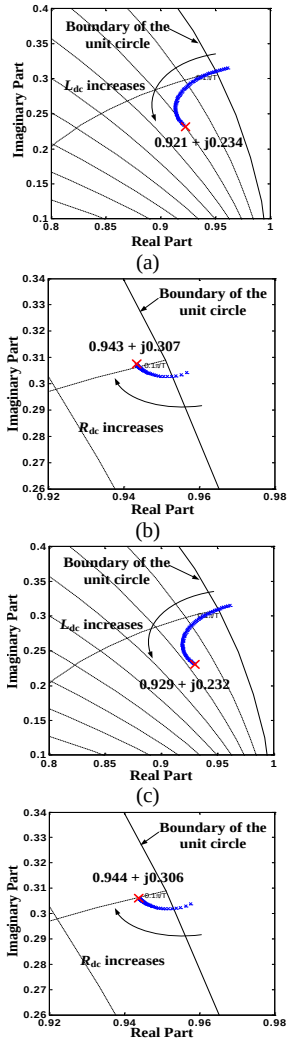

Fig. 2. Closed-loop dominant poles of $(1+Z'_{\mathrm{oeq}}/Z_{\mathrm{load}})^{-1}$ with Type I/II virtual impedance based stabilizers.
(a) R_{dc}=2 Ω, L_{dc}=0.5~6 mH (original result). (b) R_{dc}=2 Ω, L_{dc}=0.5~6 mH (zoom-in result). (c) R_{dc}=0~12 Ω, L_{dc}=6 mH (original result). (d) R_{dc}=0~12 Ω, L_{dc}=6 mH (zoom-in result).

IV. Simulation Results

Simulation tests based on MATLAB/Simulink are performed to validate the proposed stabilizer. Here, the CPL is shared by the parallel interfacing converters.

Case I: Stabilizer activation

Take Converter #1 as an example. For Type I stabilizer, the waveform of dc output voltage is shown in Fig. 3 (a). During the period of 20 ~ 40 s, the stabilizer is activated. It is shown that before t = 20 s, the dc voltage is unstable. When the stabilizer becomes active, the dc voltage keeps stable and maintains at its reference value 600 V. At t = 40 s, since the stabilizer becomes inactive, the dc voltage turns back to the unstable status. For Type II stabilizer, the waveform of dc output voltage is shown in Fig. 3 (b). It is also seen that the system stability can be guaranteed by turning on the virtual impedance based stabilizer.

Case II: Load peak

The performance of stabilizer is tested during load peak. Here, two interfacing converters are employed. During the period of 20 ~ 40 s, the power of the CPL is changed from 1000 W to 2000 W. Take Converter #1 as an example. By keeping Type I stabilizer active, the output power waveform is shown in Fig. 4 (a). Since droop control is used, the load power is equally shared and the output power of Converter #1 is changed from 500 W to 1000 W, which is half of the load power. Meanwhile, the dc output voltage waveforms are shown in Fig. 4 (b). It is shown that the dc voltage deviation is produced by using droop control. During the load peak, the dc voltage deviation increases from 2.9 V to 6.2 V. Similar results for Type II stabilizer can be found in Fig. 4 (c) and (d). It is seen that by using Type I/II stabilizers, the transient stability of the parallel converter system with CPLs can be ensured during load peaks.

Case III: Plug-and-play of the converter interfaces

The responses for plug-and-play are also tested to validate the performance of the proposed two types of stabilizers. Three parallel interfacing converters are used here. In Fig. 5 (a) – (c), Type I stabilizer keeps in use during the whole process. Before t = 20 s, only Converter #1 generates power for the load. At t = 20 s and 40 s, Converter #2 and #3 start sequentially. It is seen that the output power of Converter #1 decreases since the load power is shared by more converters. At the same time, the plug-and-play performance of the converter system with Type II stabilizer is also tested, as shown in Fig. 5 (d) – (f). It is demonstrated that by using Type I/II stabilizers, the system stability during the plug-and-play process can be maintained. The above results in Fig. 5 validate the effectiveness of Type I and Type II stabilizers during dynamic connecting process. Similar results are shown in Fig. 6 to test the performance of two types of stabilizers in the dynamic disconnecting process. It is also seen that with the proposed stabilizers activated, the system stability can be guaranteed.

V. Conclusion

In this paper, two types of virtual impedance based stabilizers are proposed to enhance the stability of dc microgrids with CPLs. Particularly, Type I stabilizer is achieved based on capacitor voltage feedback, and Type II stabilizer is achieved based on inductance current feedback. Since the interfacing converters in dc microgrids are connected in parallel, droop control for proper output power sharing is taken into account. Meanwhile, the principle of impedance matching is employed to test the stability of the parallel inverter system with CPLs. By using the above stabilizers, the instable poles of $(1+Z'_{oeq}/Z_{load})^{-1}$ induced by the negative incremental impedance of the CPL are forced to move into the stable region. Hence, the system stability can be enhanced.

Acknowledgment

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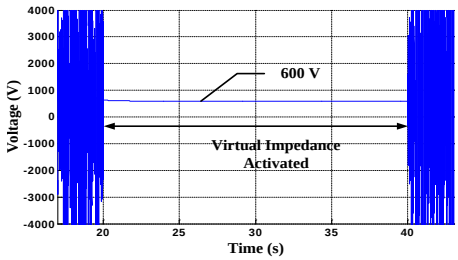
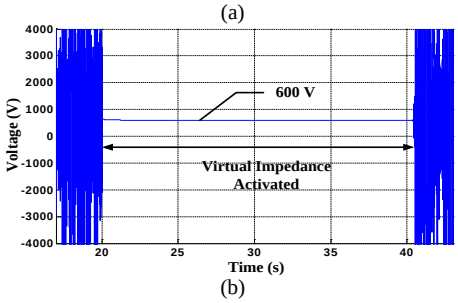
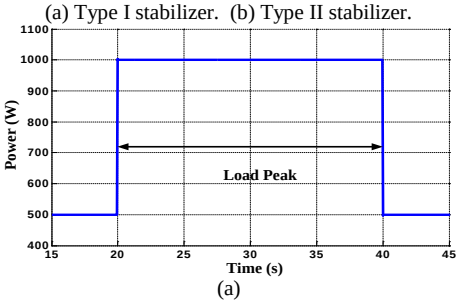


(a)



(b)

Fig. 3. Test of stabilizer activation.
(a) Type I stabilizer. (b) Type II stabilizer.



(a)

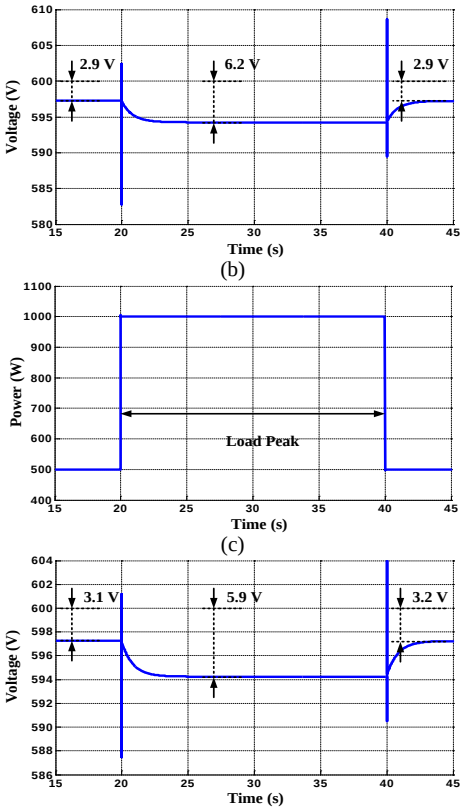
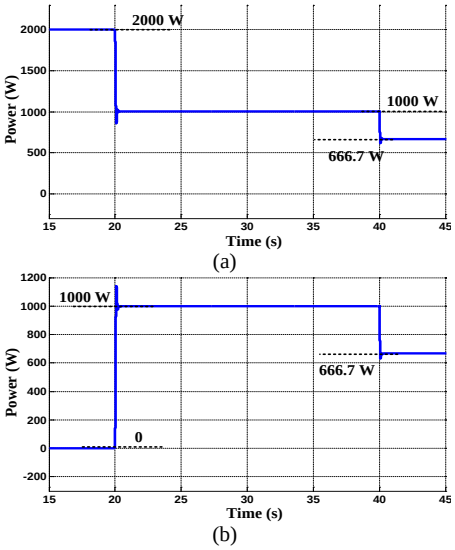


Fig. 4. Test of load peak.
(a) Output power of converter #1 with Type I stabilizer.
(b) DC voltage with Type I stabilizer.
(c) Output power of converter #1 with Type II stabilizer.
(d) DC voltage with Type II stabilizer.



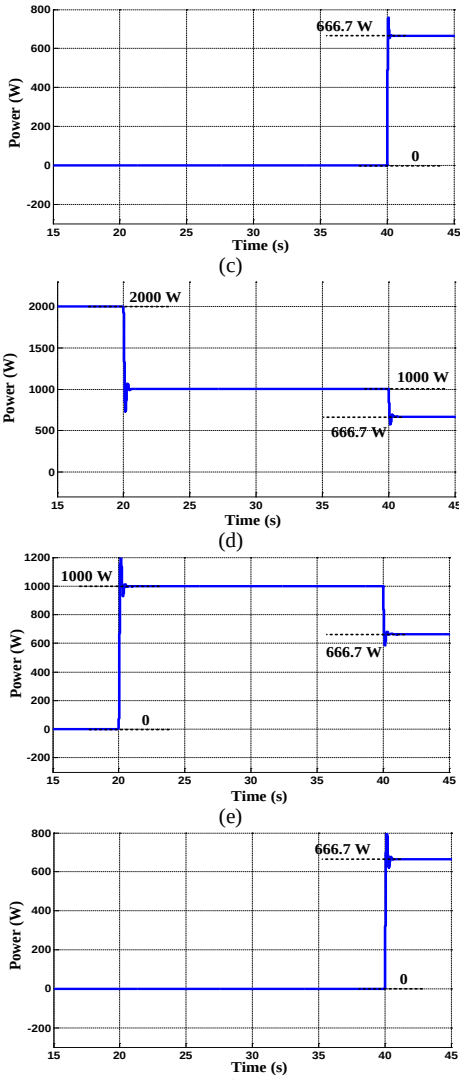
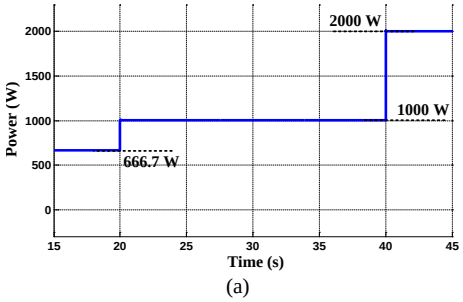
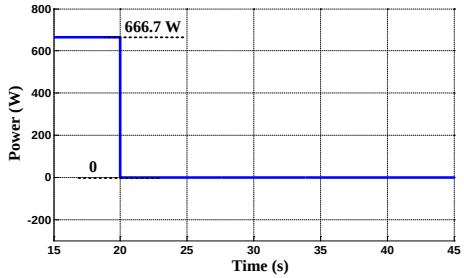
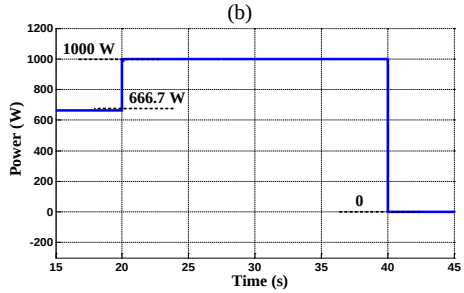


Fig. 5. Test of plug-and-play for dynamic connecting.
(a) Output power of converter #1 with Type I stabilizer.
(b) Output power of converter #1 with Type I stabilizer.
(c) Output power of converter #1 with Type I stabilizer.
(d) Output power of converter #1 with Type II stabilizer.
(e) Output power of converter #1 with Type II stabilizer.
(f) Output power of converter #1 with Type II stabilizer.

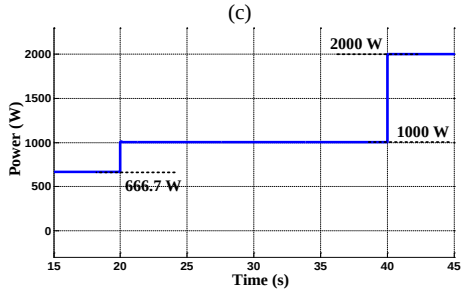




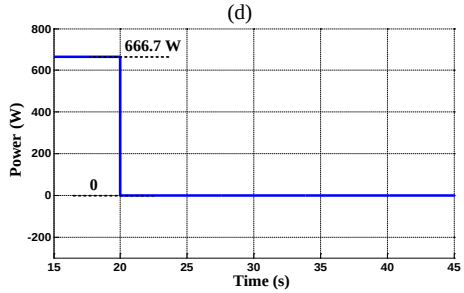
(b)



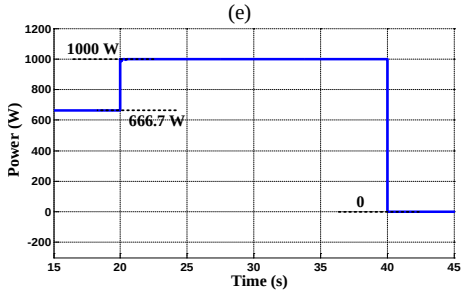
(c)



(d)



(e)



(f)

Fig. 6. Test of plug-and-play for dynamic disconnecting.
(a) Output power of converter #1 with Type I stabilizer.
(b) Output power of converter #1 with Type I stabilizer.
(c) Output power of converter #1 with Type I stabilizer.
(d) Output power of converter #1 with Type II stabilizer.
(e) Output power of converter #1 with Type II stabilizer.
(f) Output power of converter #1 with Type II stabilizer.

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