VLSI Design and Implementation of Low Power PB-CAM: A Tutorial and Survey

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Abstract

Background: A CAM is a fully parallel operating device. For high speed data searching functions CAM provides very efficient hardware architecture[1]. **Statistical Analysis:** This paper presents novel developments in the recent design of high capacity Content Addressable Memory (CAM) and Pre-computational Based CAM (PB-CAM). A graphical analysis has been shown between PB-CAM using static parameter circuit and proposed parameter circuit for power, delay and power-delay product in 90nm CMOS technology. **Findings:** There are many techniques made for designing a CAM by taking in mind to get low-power, low-noise, high-speed, less hardware cost and less data comparisons and with minimum number of transistors and gates. There are, Traditional Dynamic CAM architecture, Ones-Count PB-CAM, Parity function PB-CAM, Remainder function PB-CAM, Block-XOR PB-CAM and Master–Slave Match Line (MSML) design. In this paper we have compared 9T and 7T CAM cell operations. Static parameter circuit is compared with proposed parameter comparison circuit for power-delay product in 45nm CMOS technology. **Applications:** CAM function can be used in broader applications, such as data compression, LAN bridges, data comparison, switches, Lookup tables, Asynchronous Transfer Mode (ATM) switches, databases, communication devices, communication networks, tag directories and high speed Ethernet etc.

Keywords: Block-XOR, CAM, Master-Slave, Match-Line, Ones-Count, PB-CAM, Parity, Remainder

1. Introduction

A Content Addressable Memory (CAM) operates in parallel, to achieve high-speed data searching operations[1]. CAM provides highly reliable hardware architecture. CAM is a special kind of memory. CAM's are hardware data search intensive and comparison engines are faster than that of algorithmic designs for search-intensive and comparison applications. CAM is a functional type memory which has hoarded data in large amounts to comparing with input data and synchronized data of comparison is sent to the output.

CAM operation can be used in a vast area of applications; those are data compression, databases[2], LAN bridges, switches, communication networks, lookup tables, tag directories, associative computing etc. In high-speed networks, those are Asynchronous Transfer Mode (ATM) switch and Gigabit Ethernet; very fast lookup tables need to full-fill the requirements of these applications[3-7].

For achieving the reliable data comparison and searching techniques, CAM design for data searching and comparison circuit is implemented in parallel. In simultaneous comparisons, whole valid hoarded data in CAM is simultaneously compared with CAM input word data. Therefore, for more number of comparisons in parallel the power consumption is more and also the circuit requires much hardware cost. So to overcome these problems, one of the efficient techniques is a fully parallel CAM[8-10] circuit designed by dynamic CMOS logic. Even though the dynamic CMOS design gains the need of a low-cost and low-power CAM, but dynamic CMOS is also had problems like charge sharing, noise margin, etc. CAM in generally designed by a huge number of CAM word cells, every cell in the CAM is designed with the architecture comparison and with the data bit storage. The number of

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CAM cells required by the traditional CAM is 9 transistors (9T) in CMOS standard dynamic traditional CAM design. The functional architecture of CAM is shown in Figure 1.

Hence, the area required for 9 transistors (9T) is more. While compared with the memory cells like Static RAM (SRAM) and Dynamic RAM (DRAM) the density of CAM memory is relatively low. Due to this low-density memory, applications of CAM are limited. Even though researchers introduced new CAM word cells of having < 9T, to design these circuits, special design manufacturing technology is required. In addition to this, XOR gates of having Pass Transistor Logic (PTL) adopted by comparison of word circuits in dynamic traditional CAM cells. So while comparing with the gates like NAND and NOR, the XOR gates require more power consumption.
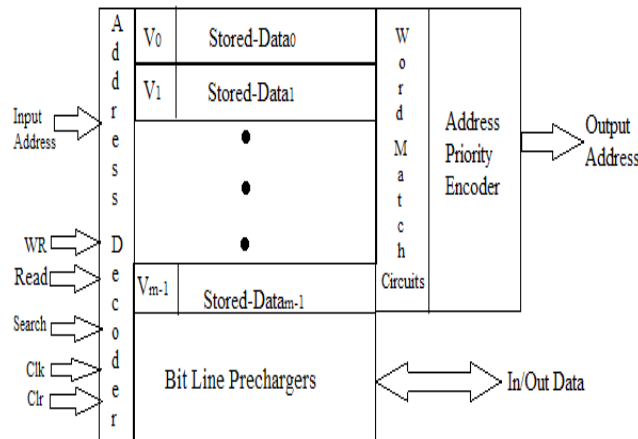

Figure 1. CAM functional block diagram[1].

In the portable systems, one of the key factors is low-voltage operation. In the comparison circuit, the dynamic traditional CAM cell uses XOR gate of PTL-type; CAM cell operating voltage cannot be reduced efficiently. Some low-voltage and low-power CAM ICs were introduced in the previous literature. Even though, most of the CAM designs[11-16] seeks high hardware cost, and also they were not reliable in the case of low-power, low-noise and low-cost system designs.

Pre-computation Based CAM (PB-CAM) method gains low-power, low-voltage and low-cost. C. S. Lin et al. introduced a PB-CAM architecture concept explained with the help of Figure 2. By this Pre-Computation process, PB-CAM design eliminates most of the data comparison and searching operations, to overcome the power consumption in majority parts in the parallel data

comparison and searching process. And also with this PB-CAM word circuit design only requires transistors are of seven (7T) and of NAND logic comparison cells. So XOR gates do not use by the PB-CAM, thus, it is simpler than in the previous literature those CMOS designs mentioned. So, for the 7 transistor PB-CAM cell, power consumption, and hardware cost are reduced. And also, while comparing PB-CAM with traditional CAM; the operating voltage which is used by the PB-CAM cell is less than the operating voltage used by the dynamic traditional CAM cell. To overcome problems in the dynamic traditional circuit of CAM, like charge shared by CAM circuit and also noise margin of it, CAM design by using ones count for the extraction of a parameter includes pseudo-nMOS static logic design.

2. PB-CAM Design Concept

As shown in Figure 1, CAM architecture generally contains address decoders with data memory, address priority encoder, word match circuit, bit-line pre-charger, and valid bit field. Valid bit field and data memory are the memories to organize traditional dynamic CAM. Where, the availability of hoarded data indicated by a valid bit field. In the operation of searching data, input data of CAM is compared parallel with all the valid hoarded data in CAM, and if the match is found during comparison then the respective address is sent to the output. Because of these large numbers of comparisons with input and hoarded data the power consumption is more. Hence by reducing the number of comparisons, the power consumption can be reduced. Based on this reason a new architecture is designed by Chi-Sheng Lin for low power CAM is called PB-CAM. In this PB-CAM architecture, the main blocks are Data-Memory (DM), Parameter-Memory (PM) and Parameter-Extractor (PE). The memory organization of the PB-CAM is shown in Figure 2. In the data-writing process, the PE extracts the parameter of input data and stores the parameter and its respected input into the PM and DM respectively.

In the data searching function, the comparison operation of data is separated into two comparison process, for the purpose of reducing a lot of comparisons. In the first comparison process, Parameter extractor extracts the parameter of input data which is then compared with the entire parameters hoarded in the parameter memory simultaneously using parameter comparison circuits. If comparison mismatches then the data related to this

hoarded parameter concurrently mismatches the input data otherwise the data related to this hoarded parameter is yet to be identified. Thus, the input data is only compared with those unidentified data in second comparison process to identify the match.

Based on these two comparison process (process-one and process-two), if the majority of the data input parameter mismatch with hoarded parameter, then in 2nd comparison number of comparisons mostly reduced. The parameter comparison circuit functions like filtering; in 1st comparison it filters most of the unmatched data and then in 2nd comparison reduces the majority of comparisons. In this paper, the pre-computation operation is called as parameter comparison process. Even though to identify any match, searching operation of data uses two comparison techniques. To increase the speed of data searching two comparison processes simultaneously performed. Parameter extractor consumes more power in introduced PB-CAM word cell. Figure 2 shows memory organized by introduced PB-CAM design by C.S Lin et al.

The power consumption of the parameter extractor circuit is high comparing with the other circuits in PB-CAM. Because the number of comparisons increases then power consumption also increases. So to overcome this problem the PB-CAM architecture needs to identify the number of unidentified information remains after the comparison operation of the parameter.

While comparing with traditional dynamic CAM cell circuit, PB-CAM word circuit need extra power consumption and extra hardware cost for both parameter comparison circuit and parameter memory. Therefore, the design idea of PB-CAM is to filter the unmatched data in the parameter comparison with the shortest bit length of the parameter. Some approaches like Block-XOR approach, Ones count approach, parity approach, and remainder approach are used in the extraction of parameter circuit of introduced PB-CAM word cell.

3. Literature Review

C. S. Lin et al, endeavor to adapt to the known CAM procedures in order to gain for a high-speed, small-area and low-power which is appropriate for VLSI implementation. The author demonstrated ones-count PB-CAM structure, which is apt for VLSI implementation by using a pseudo-nMOS static structure in CMOS technology. This leads to research on the design of ATM networks, sorting networks, low-power digital circuits, content-

addressable memories and analog to digital converters. In the year 2002, from the Macronix Foundation Golden Silicon Award was received by Mr. Lin.
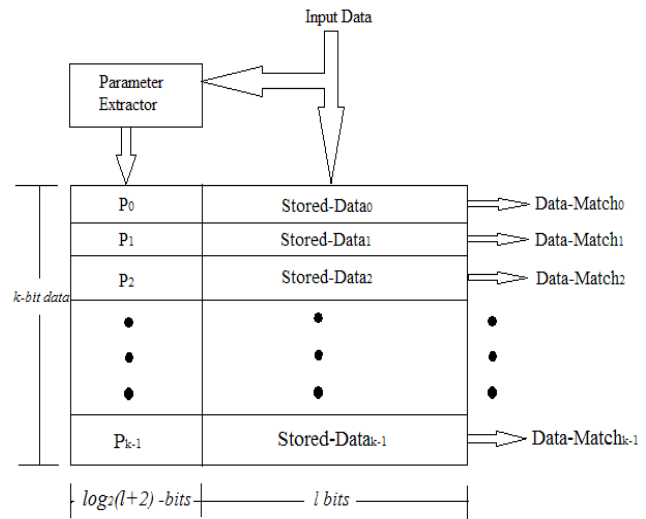

Figure 2. The PB-CAM architecture and memory organization[1].

Ones count approach in PB-CAM; by using ones count (counting no. of ones) method, it not only filters the huge collection of unidentified data with having small bit of length and also PB-CAM by using ones count approach reduces the transistors of nine (9T) from traditional CAM architecture to transistors of seven (7T). In one's count method, for l-bit word length, $l+1$ number of one's count (0 to l). In ones count approach, to extract the parameter by using parameter extractor circuit minimum required parameter length is $\log_2(l+2)$, and it showed in Figure 2. In this PB-CAM word cell design, CAM size is measured with n bits by m words. In comparison process-two, a number of data comparisons on an average is $k/(l+1)$, then the number of ones count are $l+1$ kinds, and also at a time only one kind of ones count is matched with input data in parameter comparison. If one parameter ones count is not matched with input data, in the parameter comparison, then it is treated as unidentified data. To explain this, suppose a 30 bits by 128 words CAM size, if this 013524876916 (Hexadecimal) is the input data, then the respected input of parameter extraction design by ones count approach is 15 (here the input data is first converted into binary data and then the number of ones which are present in the binary data is the data input of parameter extractor). Therefore, input data's parameter is not equal to 15, then the data which

was hoarded by the parameter mismatches with the input data. In the 30bits by 128 words CAM size the range of a parameter is varies 0 to 30 and in this range, one value is unidentified in which value of the parameter is 15, in second comparison average comparison data equals to 128/31 i.e. 4.

To express the comparison processes one and two in PB-CAM word cell, having CAM size of k words by l bits, the comparison process one takes $k \times \lceil log(l+2) \rceil$ comparisons of CAM cell, the comparison process-two takes $(k \times l)/(l+1)$ comparisons of CAM cell. Therefore, $k \times \lceil log(l+2) \rceil + (k \times l)/(l+1)$ gives the total CAM cell comparisons, which was less than the value of $k \times (\lceil log(l+2) \rceil + 1)$. The number of CAM word comparisons of traditional CAM circuit takes $k \times l$ and it is $k \times (\lceil log(l+2) \rceil + 1) \leq k \times l$ for $l > 3$, therefore, the traditional CAM cell comparison consumes much power than the ones count based PB-CAM word architecture.

Circuit designing of parameter extraction in ones count PB-CAM as follows, for n bit input data, the circuit element takes $\lceil l/3 \rceil$ full-adders for generating parallel partial additions of n bit input data in the first stage, and then the outputs of the first stage $\lceil l/3 \rceil$ sum signals for the right side link and $\lceil l/3 \rceil$ carry signals to the lift side link in parallel. Therefore, the parameter extraction architecture is built according to this definition. To explain the brief idea about parameter extractor Figure 3 shows 15-bit parameter extractions by using the ones count function.

Mathematical Analysis of ones count PB-CAM, for input data length of 14-bit, then the total input of CAM data consists of 2^{14} numbers, and to the respective parameter in the ones count function, the total input data related is $^{n}c_{r}$, i.e. $^{14}c_{r}$, where r is a kind of parameter in ones count function (range is 0 to 14) and n is number of bits for each. From the probability equations

$$^{n}c_{r} = \frac{n!}{(n-r)!(r!)}, \text{ for example, } ^{14}c_{2} = 91.$$

The average probability can be as shown in the following expression,

$$\text{Average probability} = \frac{^{14}c_{r}}{2^{14}}.$$
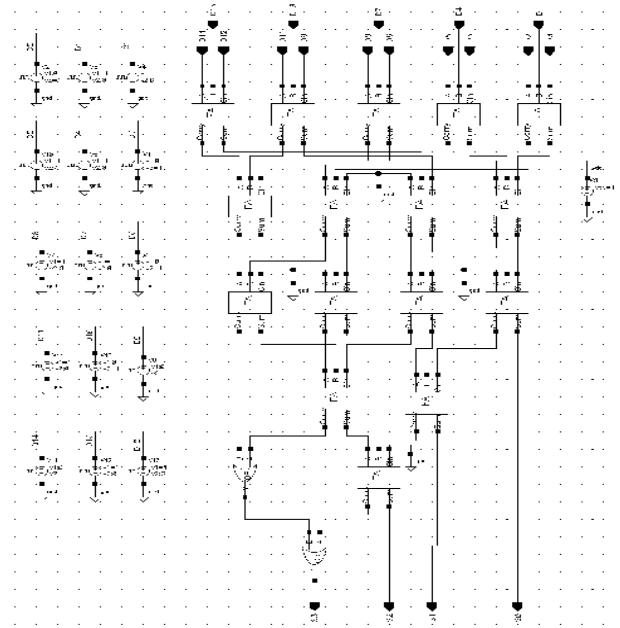

Figure 3. 15-bit parameter extractor using ones-count function circuit in 90 nm CMOS technology.

The Table 1 is introduced by C. S. Lin et al. which lists the comparison between the parameter, the whole data related to the respective parameter and average probability of input data having 14-bit of length.

Table 1. Average Probabilities and total number of data related with same parameters by using ones-count parameter extractor function[1]

Parameter		Total number of data related with respective parameter	The average probability
1111	15	Valid bit	
1110	14	1	0.01%
1101	13	14	0.09%
1100	12	91	0.56%
1011	11	364	2.22%
1010	10	1001	6.11%
1001	9	2002	12.22%
1000	8	3003	18.33%
0111	7	3432	20.95%
0110	6	3003	18.33%
0101	5	2002	12.22%
0100	4	1001	6.11%
0011	3	364	2.22%

0010	2	91	0.56%
0001	1	14	0.09%
0000	0	1	0.01%

Jui-Chuan Chang et al. presented the MOS design of parameter extractor based content-addressable memories and the design of digital circuits having low-power.

B. D. Liu et al. presented the research on including physical design of VLSI circuits and also testing for them,   System-on-Chip (SoC) integration, verification and implementing fuzzy-neural type networks and signal processors for video by using VLSI technology. This low power of pre-computation based fully parallel CAM novel VLSI architecture achieved low-cost, high-speed, low-power, noise-less and low-voltage by using ones count function for parameter extraction. This CAM system works based upon pre-computation and it reduces power dissipation, operating voltage, and also reduces the number of transistors of the CAM word cell. PB-CAM word includes pseudo-nMOS static circuit implementation for efficient CAM. Design fabricated by single poly quadruple metal with TSMC 0.35-μm CMOS process. CAM size of 30 bits by 128 words, the results indicate that PB-CAM architecture can work up to a range of 100 MHz with power consumption at supply voltage 3.3-V is 33 mW at and under supply voltage 1.5-V it works up to the range of 30 MHz.
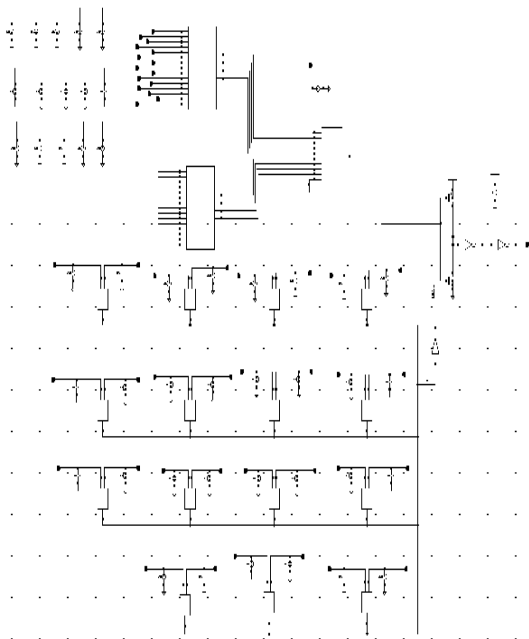

Figure 4. PB-CAM with ones-count Parameter Extractor.

Ones-count PB-CAM is shown in Figure 4. This consists of 7-transistor CAM cell, parameter extractor, and parameter comparison circuit. The operation of CAM is shown in Figure 2. Figure 5 illustrates the input/output response of the PB-CAM using ones-count parameter extractor.

S-J Ruan et al.[2], presented the research in the field of design of low-power PB-CAM. CAM is effectively included in most of the application areas, such as data compression, databases, LAN bridges, switches, communication networks, tag-directories, associative computing lookup based tables and etc. In high-speed networks, those are Asynchronous Transfer Mode (ATM) switch due to improving its application performance and by comparison process in parallel to reduce searching time. It significantly increases the power dissipation. S. J. Ruan introduced a Block-XOR function in the extraction of PB-CAM parameter for improving efficient low-power design architecture. By the analysis in mathematical, shows this approach efficiently minimize comparison operations of data by 50% on an average by the comparison of ones count function PB-CAM architecture for inputs of having 32-bit of length, found that the power dissipation in TSMC 0.35 μm CMOS logic by means of Synopsys Nanosim. These experiment results tell PB-CAM of having Block-XOR approach achieved on an average 32% in power performance minimization and 30% in minimization of power, with the comparison of ones-count PB-CAM architecture. The main aim of this research paper is that it gives a theory as well as proofs to verify the Block-XOR pre-computation-based CAM architecture, which achieves better power minimization of having no need of a special kind of CAM cell design. It tells that Block XOR approach is more adaptive and flexible for CAM designs.

Yen-Jen Chang (M'02)[3], presented the research work on VLSI design implementation include digital ICs design, microprocessor and computer architecture, the design of low-power memory, the design of the system on chip and embedded system.

Tung-Chi Wu[3] presented the research on low-power VLSI design, computer-aided manufacturing and SRAM of having low-power and also embedded system.

In the efficient fast lookup applications CAM can be efficiently used. In CAM memory, parallel data comparison process costs high power consumption. T. C. Wu presented a novel design of CAM word circuit, which adopts the Master-Slave Match Line (MSML), which

aims to merge the minimization technique of charge refill and the architecture of master-slave to minimize the CAM power consumed in Match Lines (MLs). This design includes multiple Slave-MLs (SMLs) and single Master-ML (MML) to operate search function, but in the case of previous CAM word architecture, only one ML is used. The ML power dissipation can be minimized efficiently by sharing the unmatched SML with the MML charge, so this CAM design can reduce the MML charge refill swing. Theoretically, compared with the conventional NOR-type CAM architecture, the power saved by the ML is $\geq 50\%$ and also independent of the match case and search pattern. The simulated results show the ML energy dissipation by the range of 7% to 57% by using the MSML of having good configuration, which leads to increase the word size. In addition to it, a newly modified CAM cell design to facilitate the match performance of MSML, which leads to MSML-hp design, which can even better result in 28% and 69% energy-delay product improvement compared with the traditional CAM and original MSML architecture designs in the 128-bit CAM word size case.
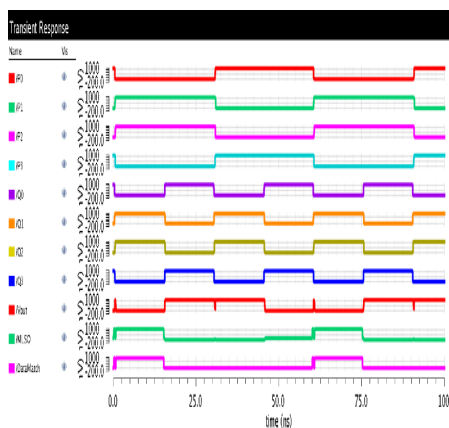

Figure 5. Transient response of ones-count PB-CAM.

C. C. Wang[4], presented the research work include low-power, low-leakage and high-speed memory designs in the field of VLSI.

J. S. Wang[4], presented the research work on the design of VLSI high speed and low power analog ICs, digital ICs and systems, CMOS image sensing devices, and design of SOC and IP.

C. W. Yeh[4], reckoned about a new VLSI architecture by using CMOS technology to design CAM architecture for IP address look-up tables of having faster performance with Match-Line scheme having AND-type and via novel CAM architecture design called Ternary CAM (TCAM)

design for solving key equation in order to reduce the consumption of power and hardware. TCAM (Ternary Content Addressable Memory) is one of the major important memory components for most of the applications. The challenges to TCAM, while designing was considered as rapidly increasing routing-table size with low-power dissipation and high-speed search engines. C. Yeh presented that for IP address lookup based table's high efficient and lower power TCAM. In this tree AND-type ML (match-line) scheme is one technique for the high-speed search operation. The other technique for low-power was SSL (Segmented Search-Line) scheme.

Y. T. Pai et al.[5], reckoned about CMOS comparison circuit for lower power PB-CAM and implemented CMOS logic gates instead of the conventional circuit design to eliminate power consumption occurred by short circuit current. Estimated power consumption by Synopsys Nanoism by using TSMC 0.18 tech-file. PMOS and NMOS width ratio were set to 3:1. This ratio can efficiently decrease both fall and rise times, by decreasing the time delay for every comparison cycle. This PB-CAM architecture saves on an average 50.2% power consumption while compared with pseudo-nMOS static CAM architecture.

A. T. Do et al.[6] presented the work on Very Large Scale Integration systems. Introduced a parity-bit CAM and it overcomes 39% sensing delay and comparing with area and power cost of the system it consumes even less than 1%. Presented gated power effective technique to decrease the average and peak power dissipation and increased the ability of a system to cope with errors and variations in the process during execution time. The overall power consumed by the circuit is reduced by employing the feedback loop auto control power-supply to the elements under comparison and average power is reduced to 64% compared with the Ones-Count approach. And also, this approach can work at a 0.5v supply voltage. Figure 6 shows the conceptual view of One's count PB CAM and Parity-bit based CAM cell.

The operation of 9-Transistor (9T) CAM cell as shown in Table 2.

Table 2. Operation of 9T CAM cell[1]

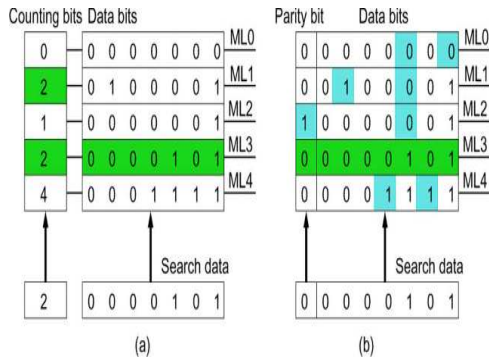| BLi	Qi	~BLi	CAM cell
0	0	1	Floating
0	**1**	**1**	**0**
1	0	0	0
1	1	0	Floating

Figure 6. (a) Ones count PB-CAM and (b) Parity-bit based CAM conceptual view[6].

The operation of 7-Transistor (7T) PB-CAM cell as shown in Table 3.

Table 3. Operation of 7T PB-CAM cell[1]

BLi	Qi	PB-CAM cell
0	0	Floating
0	**1**	**Floating**
1	0	0
1	1	Floating

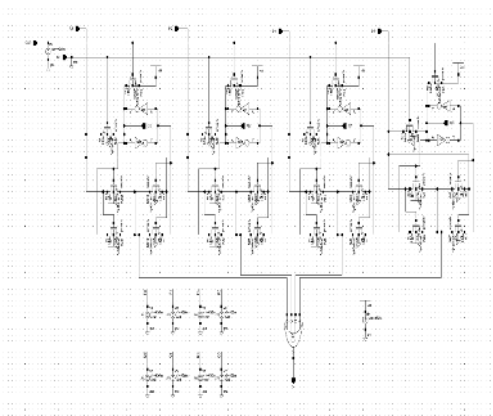Figure 7 shows static parameter comparison circuit, it is used to compare the parameters of the input data and parameters of the stored data simultaneously.

Figure 7. Static parameter comparison circuit with 45nm CMOS technology.

4. Proposed Parameter Comparison Circuit

The parameter comparison circuit is used to compare the parameters from the hoarded parameter memory and new input extracted parameter. In PB-CAM the param-eter comparison circuit a plays a major roll. For example, if any user wants to communicate with the router for accessing the information the device first send a request to the router, then router compare that request with already hoarded data in it and gives acknowledgment to that user. For this comparison operation, we need fast comparing circuits with low-power consumption. The proposed parameter comparison circuit shown in Figure 8 is high speed and less power consumption than tradi-tional parameter comparison circuits.
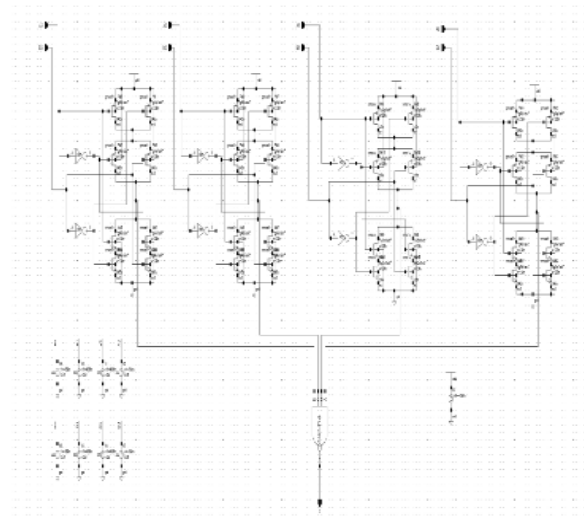

Figure 8. Proposed parameter comparison circuit with 45 nm CMOS technology.

Figure 9 shows the output of proposed parameter extractor circuit using 45 nm CMOS technology, this parameter has been used to reduce the comparisons and ultimately increasing of speed.
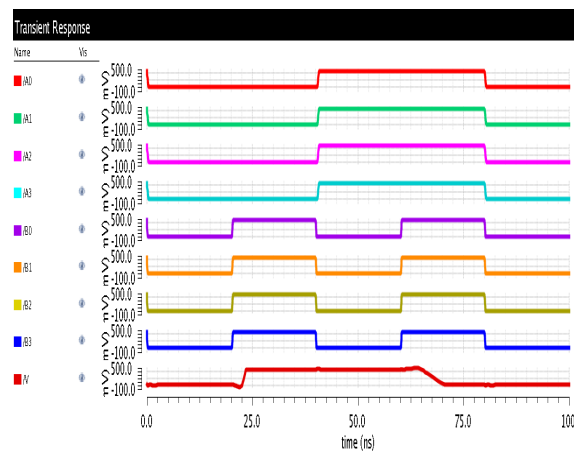

Figure 9. Transient response of proposed parameter comparison circuit.

Figure 10 shows Power-Delay product comparison for static parameter comparison circuit and proposed parameter comparison circuit using 45 nm CMOS technology[1].
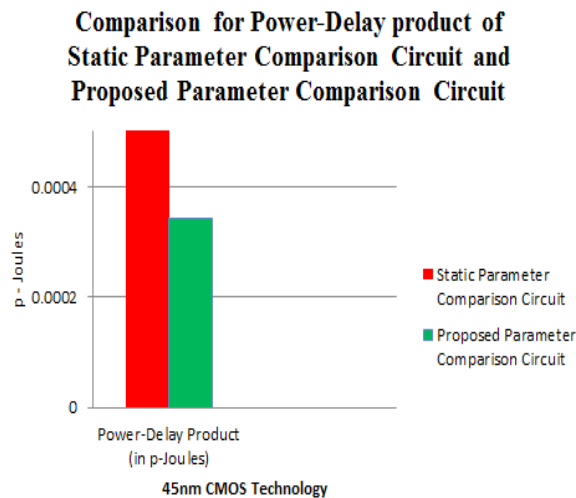

Figure 10. Power-Delay product comparison.

Figure 11 Power, delay, and power-delay product comparison for PB-CAM represents using static parameter comparison circuit and proposed parameter comparison circuit with 90nm CMOS technology[1].
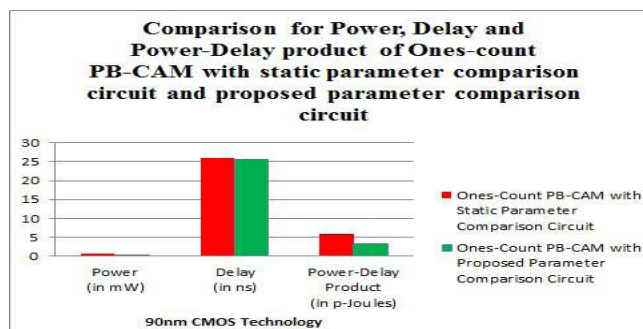

Figure 11. Power, delay, and power-delay product comparison for PB-CAM.

5. Conclusion

In this paper, we surveyed novel developments in the recent design of high-capacity CAM, PB-CAM, Parameter Extractor (PE) and Parameter comparison circuits. There are many techniques are made for design CAM, PB-CAM, and Parameter Extractor blocks by keeping the aim to achieve lesser power consumption, low-noise, high-speed, less hardware cost and fewer data comparisons and with minimum hardware requirements. In this paper, we

discussed traditional dynamic CAM architecture, Ones-Count PB-CAM, parity function PB-CAM, Block-XOR PB-CAM, and Master–Slave Match Line (MSML) design and also discussed the mathematical analysis of one's count parameter extractor in PB-CAM and parameter comparisons in one's count method.

The ones count PB-CAM fabricated by TSMC 350 nm single poly quadruple metal CMOS logic and with 30 bits by 128 words CAM, and this PB-CAM circuit works up to 100 MHz with 33 mW power-consumption at 3.3 V supply and works up to 30 MHz at 1.5 V supply[1]. Comparing with ones count approach, Block-XOR approach for PB-CAM reduces a total number of comparisons by 50% on an average for inputs of 32 bit long[2]. Parity bit CAM leads to a reduction of sensing delay by 39% and also effectively gated power technique for reduction of average and peak power consumption.

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