Text Book

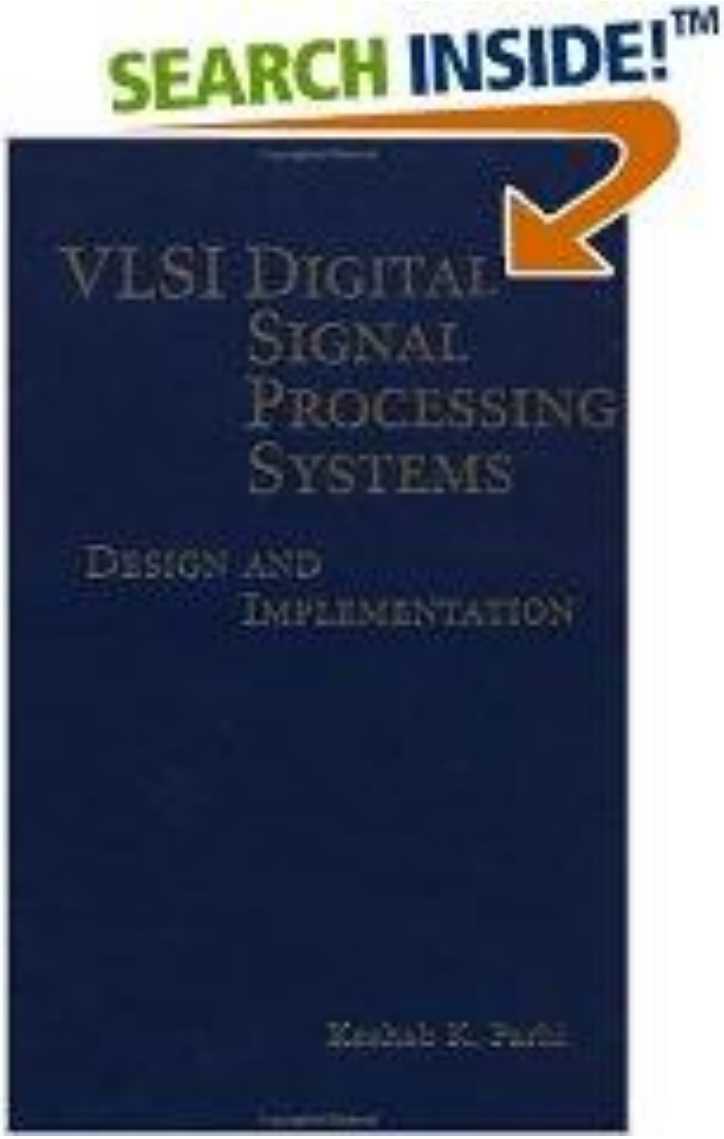
VLSI Digital Signal Processing Systems Design and Implementation

Keshab K. Parhi, ***Ph. D.***

Department of Electrical and Computer Engineering

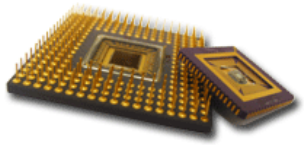
University of Minnesota, MN 55455

Text Book (2/2)


SEARCH INSIDE!™
VLSI DIGITAL SIGNAL PROCESSING SYSTEMS
DESIGN AND IMPLEMENTATION

Prof. Parhi's Education

- *B. Tech. (Honors) degree from the Indian Institute of Technology, Kharagpur (India), in 1982.*
- *M.S.E.E. degree from the EE Department, University of Pennsylvania, Philadelphia, in 1984.*
- *Ph.D. degree from the EECS Department, University of California, Berkeley, in 1988.*

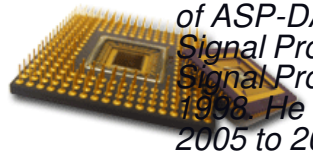


Prof. Parhi's Brief Biography

- *Keshab Parhi has been with the Department of Electrical & Computer Engineering at the University of Minnesota, Minneapolis, since 1988, where he was an Assistant Professor from Oct. 1988-June 1992, Associate Professor from July 1992-June 1995, and has been a Professor since July 1995. Since 2000, He has held the permanent title of "Distinguished McKnight University Professor" awarded by the Graduate School of the University. Since 1997, he has held the title of "Edgar F. Johnson Professor" awarded by the College of Science and Engineering. From July 2008 till August 2011, he served as the Director of Graduate Studies of the Electrical Engineering program. He has held short term positions in several industries such as IBM T.J. Watson Research Center (Yorktown Heights, NY), AT&T Bell Laboratories (Holmdel, NJ), NEC Corporation (Miyamae-Ku, Kawasaki, Japan), where he was a National Science Foundation Japan Fellow, Broadcom Corp., Irvine, CA, and Medtronic Corp., Minneapolis, MN. He has been a visiting Professor at Delft University (The Netherlands) and Lund University (Sweden).*

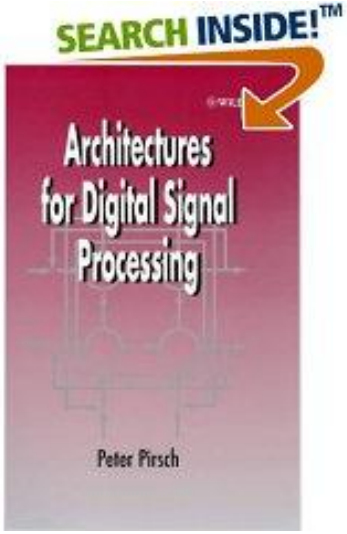
  His research addresses VLSI architecture design and implementation of signal processing, communications and biomedical systems, error control coders and cryptography architectures, high-speed transceivers, stochastic computing, secure computing, and molecular/DNA computing. He is also working on intelligent classification of biomedical signals and images, for applications such as seizure prediction and detection, schizophrenia classification, biomarkers for mental disorders, brain connectivity, and screening of fundus and optical coherence tomography (OCT) images for ophthalmic abnormalities. He has published over 550 papers, has authored the text book VLSI Digital Signal Processing Systems: Design and Implementation (Wiley, 1999), and is the co-editor (with Takao Nishitani) of the reference book "Digital Signal Processing for Multimedia Systems" (CRC Press, March 1999). He has coauthored the research monographsPipelined Adaptive Digital Filters (with Naresh Shanbhag, 1994), Digit-Serial Computation (with Richard Hartley, 1995) and Pipelined Lattice and Wave Digital Recursive Filters (with Jin-Gyun Chung, 1996), all published by Springer.

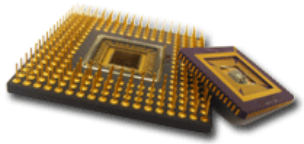
  Dr. Parhi is the recipient of numerous awards including the 2013 Distinguished Alumnus Award from IIT, Kharagpur, India, 2013 Graduate/Professional Teaching Award from the University of Minnesota, 2012 Charles A. Desoer Technical Achievement award from the IEEE Circuits and Systems Society, the 2004 F. E. Terman award from the American Society of Engineering Education, the 2003 IEEE Kiyo Tomiyasu Technical Field Award, the 2001 IEEE W. R. G. Baker prize paper award, and a Golden Jubilee medal from the IEEE Circuits and Systems Society in 2000. He has served on the editorial boards of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS —PART I and PART II, VLSI Systems, Signal Processing, Signal Processing Letters,and Signal Processing Magazine, and served as the Editor-in-Chief of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS —PART I (2004-2005 term), and currently serves on the Editorial Board of the Springer Journal of Signal Processing Systems (JSPS). He has served on technical program committees of IEEE Conferences such as ASAP, ICASSP, ISCAS, Computer Arithmetic Symp., Great Lakes Symp. on VLSI, workshop on VLSI Signal Processing, SiPS, Workshop on VLSI in Communications, and of ASP-DAC, IECS and IWISP conferences. He has served as technical program cochair of the 1995 IEEE VLSI Signal Processing workshop and the 1996 ASAP conference, and as the general chair of the 2002 IEEE Workshop on Signal Processing Systems. He was a distinguished lecturer for the IEEE Circuits and Systems society during 1996-1998. He served as an elected member of the Board of Governors of the IEEE Circuits and Systems society from 2005 to 2007. He is a Fellow of IEEE (1996).



Reference Book

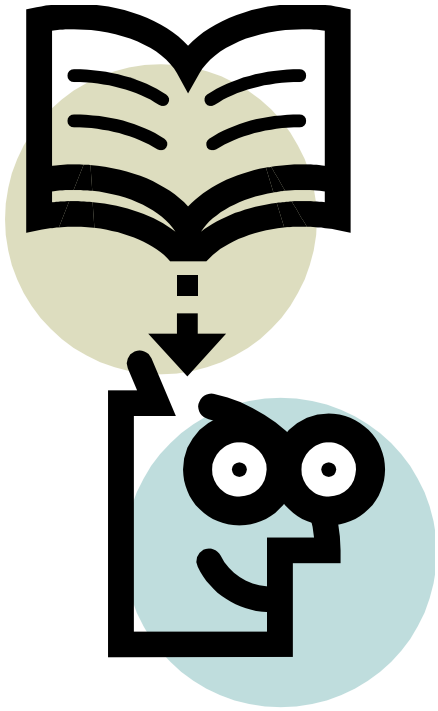
- Peter Pirsch, ***Architectures for Digital Signal Processing.*** Chichester, John Wiley & Sons, 1998.
- Mahesh Mehendale and Sunil D. Sherlekar, ***VLSI Systhesis of DSP Kernels: Algorithms and Architectural Transformations.*** Boston, Kluwer Academic Publishers, 2001.
- S. Y. Kung, ***VLSI Array Processor.*** Englewood Cliffs, NJ: Prentice-Hall, 1988.
- Handout.

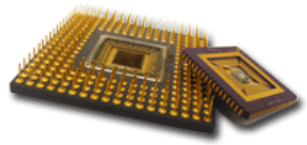




Lecture Goal

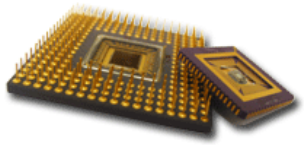
- Introduce the **various DSP-related algorithms and architectures** for the **VLSI-DSP system designs**
- Graduate students for one semester





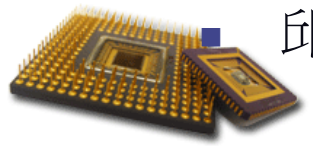
Lecture Outline

- Lecture 1 Introduction to Digital Signal Processing Systems
- Lecture 2 Iteration Round
- Lecture 3 Pipelining and Parallel Processing
- Lecture 4 Retiming
- Lecture 5 Unfolding
- Lecture 6 Folding
- Lecture 7 Algorithmic Strength Reduction in Filters and Transforms
- Lecture 8 Pipelined and Parallel Recursive and Adaptive Filters
- Lecture 9 Low-Power Design
- Lecture 10 Programmable Digital Signal Processors
- Lecture 11 Introduction to 3D Graphics Processing Flow
- Lecture 12 Introduction to GPU Hardware
- Lecture 13 Geometry Subsystem Design



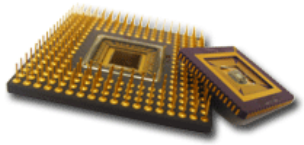
授課方式 & 評分標準

- 教授授課
- 評分標準
  - 期中報告: 30%
  - 期末計畫: 50% (請選擇一個比賽參加)
  - 作業: 20%
  - 出席: 0.25N% (表示全學期點名共N次, 每次點名均出席加0.25N分, 一次曠課加0.25(N-1)分,兩次曠課加0.25(N-2)分,... 點名施主均沒有出席則不加分)。
  - ----------
  - 總和: (100+0.25N)%
- Material Web-Site:
  - http://viplab.cs.nctu.edu.tw/course/VLSI-DSP2015_Fall.htm
- Teaching Assistant:
  - 邱敬捷 (e-mail: ccchiu(at)viplab.cs.nctu.edu.tw 分機: 59283)



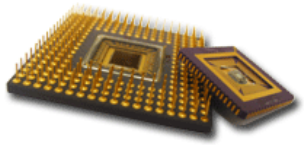
期中報告

- 研讀期刊論文並報告
- 研讀課本章節並報告
- 其它方式（須與老師討論過）



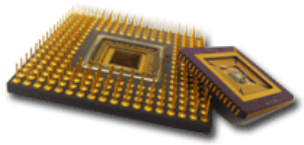
期末計畫

- Team Work
- 演算法或架構的改良或論文創作。
- 創意發揮使用IoT平臺，並參與比賽。



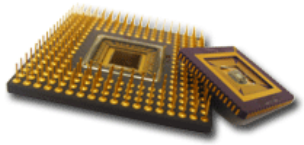
VLSI Signal Processing System Design Spectrum (1/2)

- Computer arithmetic
  - Adder
  - Multiplier
  - Inverse square root
  - Division
- Digital filter
  - Multidimensional filter
  - Symmetry filter
- Adaptive digital filter
  - LMS/DLMS (Delay LMS) based
  - RLS based
- Transform
  - Multiplier-accumulator based
  - Recursive-filter based
  - ROM-based: DA, CORDIC
  - Butterfly based
- Processor
  - General purposed processor
  - DSP processor
  - Reconfigurable computing processor
- 3D Graphics
  - Geometry transformation
  - Rasterization/Rendering
  - Z-buffer compression
  - Texture compression
- Ear-Aid System
  - Adaptive algorithm
  - Filter bank
- System Security



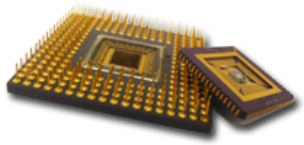
VLSI Signal Processing System Design Spectrum (2/2)

- MIMO Detection
  - Grouped Detection
  - VBLAST
  - K-Best
- Biomedical Computation
  - ICA
  - PCA
  - HRV
- ADC
  - SAR ADC
  - Pipeline ADC
  - Sigma-Delta
- PLL
- Image Processing
  - Pattern Recognition
  - Median Filter
  - Image Reconstruction
  - Image Projection
- Video Processing
  - Compression
  - Block Matching
  - Deblocking filter
- Non-numerical operation
  - Error control coding
    - Viterbi Decoder
    - Turbo Code
  - Polynomial computation
  - Dynamic programmable



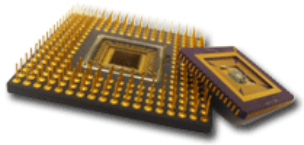
Homework

- Homework is not “Teamwork”!!
- You can discuss with each other but not “COPY”!!
- Don’t miss hard deadline for each homework!!



My Lab: VLSI Information Processing (VIP) Research Lab

- His research interests are in VLSI algorithms, architectures, and chips for digital signal processing (DSP) and biomedical signal processing. This includes the design of low-power/high-performance/cost-effective 3-D graphics processing system, adaptive/learning systems, computer arithmetic, multidimensional filters, transforms and IoT applications. He has published more than 50 journal and conference papers in these areas.



VIP Research Lab (2014)

Intel Taiwan 英特爾台灣電子報
2014 第四季

英特爾全國大專院校
智慧系統設計 學生創意 應用無限

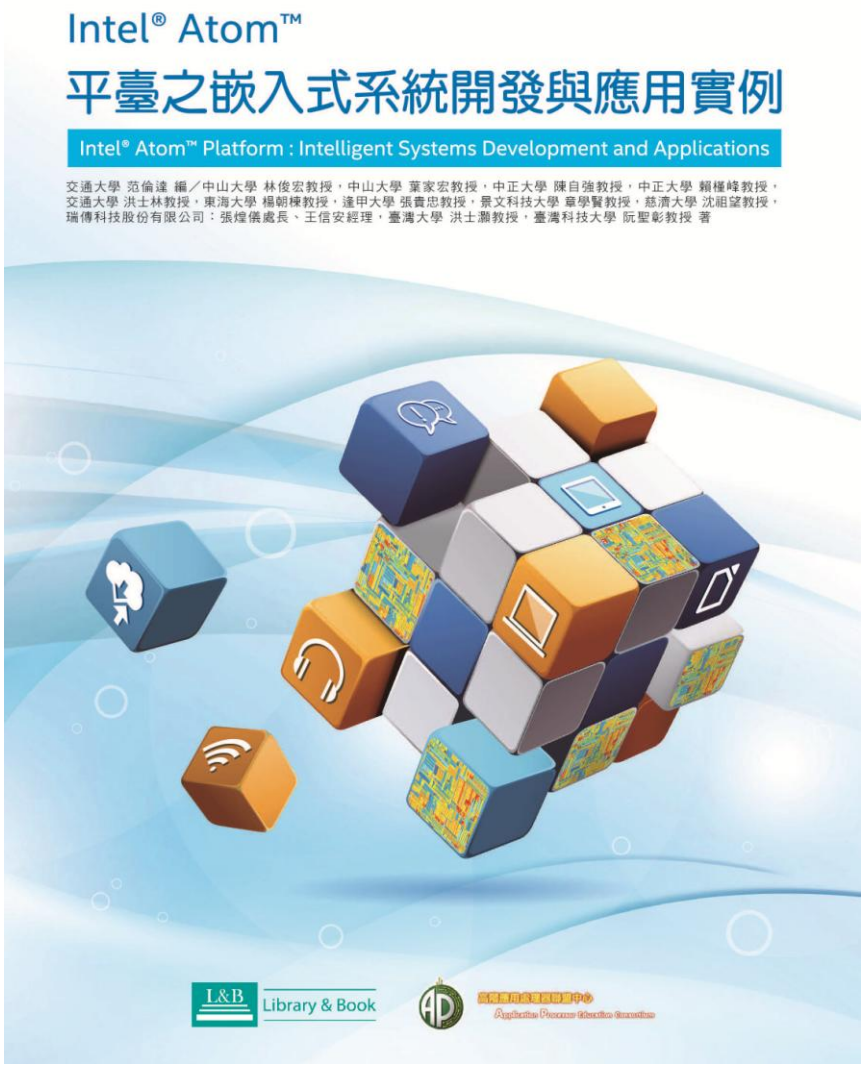
結合現代智慧型手機與 RFID、車門遙控開關，南開科技大學車輛與機電產業碩士班學生林育存、楊宗明及陳柏翔設計出汽車智慧防盜系統，也就是「手機即汽車搖控器」，讓汽車防盜更便利。

南開科技大學車輛與機電產業碩士班林育存、楊宗明及陳柏翔以 Intel Galileo 架構所開發的汽車智慧防盜系統，透過手機 APP 等軟體作為控制面，再利用 RFID、車門遙控開關為基礎架構，設計出便利的防盜系統，除了擁有最先進的定位功能外，還能夠在汽車被竊之後，切斷供油、截斷起動電路設計，讓竊賊無法開動汽車，也無法偵測拷貝。這套智慧防盜在 2014 英特爾全國大專院校智慧系統設計學生競賽中，以創新的設計及實用性，拿下季軍。

獲得亞軍的「環繞音效電子聽診器」專題是由一群還在南臺科技大學電機工程系就讀的郭家銓、黃聖婷、林芠以開發完成。透過指導教授魏兆煌的全力輔導，這件可將單聲道的心音信號經由構向濾波器分割輸出，對雙耳產生一個模擬立體音效，使得聽診者能更容易區分不同的心音，同時將原始心音及分離後的左右心音以波形顯示，得到評審的青睞與肯定。尤其學生團隊能夠運用高階 FPGA 板卡，設計出能區分小於 40mS 間隔之心跳聲，並將心跳聲以波形顯示，以目視輔助聽診和使聽診者更容易診斷心血管相關病情外，也因能記錄與重播心跳聲及其波形，便於共同分析診斷或教學。

受邀在 Intel 亞洲區創新高峰會一起與其他來自英特爾實驗室共同展示多項技術創新的冠軍作品，是由國立交通大學范倫達教授所指導的團隊資訊工程學系學生楊耘安、謝永耀和李嘉棋開發的 "智能升降機系統"，這項以 Intel Galileo 為平台的作品，針對傳統電梯運行系統的幾項缺陷做了改良，透過聰明的運算和設計，能讓電梯外的乘客能夠了解電梯的即時使用情況，使電梯內的乘客不用面臨明明滿載卻還在非目的地的樓層停留，並且讓各樓層的使用者能夠得到合理的資源分配，可以直達電梯目的地，節省成本。這項將 "梯次" 的概念加入智能升降機運行系統和將載重狀況顯示給等待乘客知道，相信這套系統能在未來對於大量使用的電梯作更有效的利用和節省可觀的電力資源。

VIP Research Lab (2014)



VIP Research Lab (2009)

VIP Research Lab (2007)