VLSI FOR NEURAL NETWORKS AND ARTIFICIAL INTELLIGENCE

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PREFACE

Neural network and artificial intelligence algorithms and computing have increased not only in complexity but also in the number of applications. This in turn has posed a tremendous need for a larger computational power that conventional scalar processors may not be able to deliver efficiently. These processors are oriented towards numeric and data manipulations. Due to the neurocomputing requirements (such as non-programming and learning) and the artificial intelligence requirements (such as symbolic manipulation and knowledge representation) a different set of constraints and demands are imposed on the computer architectures/organizations for these applications.

Research and development of new computer architectures and VLSI circuits for neural networks and artificial intelligence have been increased in order to meet the new performance requirements. This book presents novel approaches and trends on VLSI implementations of machines for these applications. Papers have been drawn from a number of research communities; the subjects span analog and digital VLSI design, computer design, computer architectures, neurocomputing and artificial intelligence techniques.

This book has been organized into four subject areas that cover the two major categories of this book; the areas are: analog circuits for neural networks, digital implementations of neural networks, neural networks on multiprocessor systems and applications, and VLSI machines for artificial intelligence. The topics that are covered in each area are briefly introduced below.

Analog Circuits for Neural Networks

Using analog circuits as a mean to compute neural networks offers a number of advantages such as smaller circuit size, higher computing speed, and lower power dissipation. Neural network learning algorithms may need be implemented directly in analog hardware in order to reduce their computing time. *Card* presents a number of analog circuits for on-chip supervised and unsupervised learning. *Landolt* has developed and implemented in analog CMOS a full Kohonen network with learning capability. *Valle et al* report an implementation of a backpropagation learning algorithm along with some simulation results. *Lafargue et al* address the problem of designing a mixed analog-digital circuit for the Boltzmann machine learning rules. *Brause* introduces the building blocks of a linear neuron that uses anti-Hebb rule and restricted weights. *Raffo et al* present a set of functional primitives that perform synaptic and neural functions which are implemented on an analog circuit.

Digital Implementations of Neural Networks

Digital implementations of neural networks provide some advantages, such as: noise free, programmability, higher precision, reliable storage devices. *Delgado-Frias et al* present a pipelined bit-serial digital organization that is able to implement a backpropagation learning algorithm. *Fornaciari and Salice* propose a tree-structure architecture based on a pseudo-neuron approach. *Viredaz et al* introduce a multi-model neural network computer based on the systolic computing paradigm. *Asonovic et al* present a fully programmable single chip microprocessor that is intended to be used within a Sun Sparcstation. *Ae et al* extend the self-organizing system (or Kohonen network) for semantic applications. *Hui et al* present a probabilistic RAM-based model that incorporates a reward-penalty learning algorithm. *Hurdle et al* propose an asynchronous design approach for neuro-computing; the CMAC neural model is used to demonstrate the approach capabilities.

Neural Networks on Multiprocessor Systems and Applications

König and Glesner present an architecture and implementation of a scalable associative memory system. *Ryan et al* describe how neural network can be mapped onto dataflow computing approach. A custom associative chip that has 64 fully interconnected binary

neurons with on-chip learning is presented by *Gascuel et al* The use of RISC processors as implementation of neural network simulation is a study by *Rückert et al;* they report results from eight different processors. *Kolcz and Allinson* have studied the implementation of CMAC, a perceptron-like computational structure, using conventional RAMs. *Wang and Tang* have developed GENET which is a competitive neural network model for AI's constraint satisfaction problems. *Luk et al* introduce a declarative language, called Ruby, that could be used in developing of neural network hardware. *Palm et al* present a study of the integration of connectionist models and symbolic knowledge processing. *Styblinski and Minick* present two Tank/Hopfield-like neural network methods for solving linear equations.

VLSI Machines for Artificial Intelligence

Eight papers address a number of current concerns in the hardware support of artificial intelligence processing. *Lavington et al* present a SIMD approach for pattern matching that is often used in production systems. *Howe and Asonovic* introduce a system that incorporates 148X36-bit content addressable parallel processors. *Cannataro et al* explain a message-passing parallel logic machine that can exploit AND/OR parallelism for logic programs. *Rodohan and Glover* outline an alternative search mechanism that can be implemented on the Associative String Processor. *De Gloria et al* present two performance analysis of a VLIW architecture where global compaction techniques are used. *Civera et al* discuss the application of a VLSI prolog system to real time navigation system; requirements, such as processes, memory bandwidth, and inferences per second, are presented. *Demarchi et al* present the design and a performance evaluation of a parallel architecture for OR-parallel logic programs. *Yokota and Seo* present a RISC Prolog processor which include compound instructions and dynamic switch mechanisms.

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This book is an edited selection of the papers presented at the *International Workshop on VLSI for Neural Networks and Artificial Intelligence* which was held at the University of Oxford in September 1992. Our thanks go to all the contributors and especially to the programme committee for all their hard work. Thanks are also due to the ACM-SIGARCH, the IEEE Computer Society, and the IEE for publicizing the event and to the University of Oxford and SUNY-Binghamton for their active support. We are particularly grateful to Laura Duffy, Maureen Doherty and Anna Morris for coping with the administrative problems.

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