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Research Article

VLSI Implementation of Green Computing Control Unit on Zynq FPGA for Green Communication

Anurag Shrivastava[1], **Ali Rizwan**[2], **Neelam Sanjeev Kumar**[3], **R. Saravanakumar**[4], **Inderjit Singh Dhanoa**[5], **Pankaj Bhambri**[6] and **Bhupesh Kumar Singh**[7]

[1]*ECE, Lakshmi Narain College of Technology and Science Indore, India*
[2]*Department of Industrial Engineering, Faculty of Engineering, King Abdulaziz University, Jeddah 21589, Saudi Arabia*
[3]*Department of BME, Saveetha School of Engineering, Saveetha Institute of Medical and Technical Sciences, Thandalam, Chennai, India*
[4]*Department of Wireless Communication Institute of ECE, Saveetha School of Engineering, Saveetha Institute of Medical and Technical Sciences, Chennai, India*
[5]*Department of Computer Science and Engineering, Guru Nanak Dev Engineering College, Ludhiana, Punjab, India*
[6]*Department of Information Technology, Guru Nanak Dev Engineering College, Ludhiana, Punjab, India*
[7]*Arba Minch Institute of Technology, Arba Minch University, Ethiopia*

Correspondence should be addressed to Bhupesh Kumar Singh; dr.bhupeshkumarsingh@amu.edu.et

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The issue of the energy shortage is affecting the entire planet. This is occurring because of massive population and industry growth around the world. As a result, the entire world is attempting to implement green networking systems and manufacture the power/energy efficient products. This research work discusses the green networking system technologies. This work introduces a power-efficient control unit (CU) design and implemented on the Zynq SoC (System on Chip) ultrascale field programmable gate array (FPGA). The VIVADO HLx Design Suite is used to simulate and analyze the CU model which is considered as one of the key components of central processing unit (CPU), used for data communication purposes. The CU is made suitable for the green communication by making it power-efficient. Therefore, the power consumption of the CU is analyzed for the various set frequency value ranging between 100 MHz and 5 GHz, and it is discovered that as the clock frequency rises up, the total power consumption also tends to get increased. The total power of the proposed model is reduced by 77.42%, 21.29%, and 17.93% from three models, respectively, being compared in the present paper. Final results shows that the CU is better suited to run at low frequencies to optimize power consumption.

1. Introduction

There have been many issues with the scarcity of natural resources in the Earth because of the rapid population expansion and industrialization in the world [1]. Thus, people are worried about the future generation saving of those resources. This can be done using green technology of connectivity and energy-efficient machines [2]. The work represents a step in the direction of promoting green networking technology and energy-efficient devices. A control unit (CU), to minimize the power consumption, is installed on field programmable gate array (FPGA) in this work. A control unit is a part of a circuitry that regulates activity in the computer [3]. It gives instructions on how to react to instructions that the program sends to these devices in the logic unit, memory, input, and output devices [4]. Figure 1 shows the block scheme for the control unit. It selects and retrieves instructions from the main memory in the proper sequence and interprets them to allow other functional elements to perform the respective operations at the

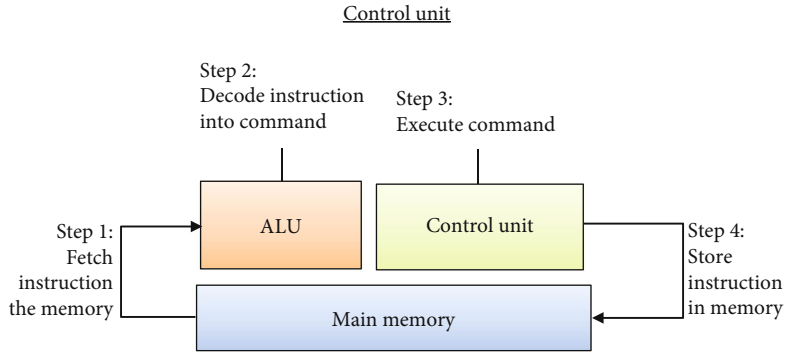

Figure 1: The block scheme for the CU.

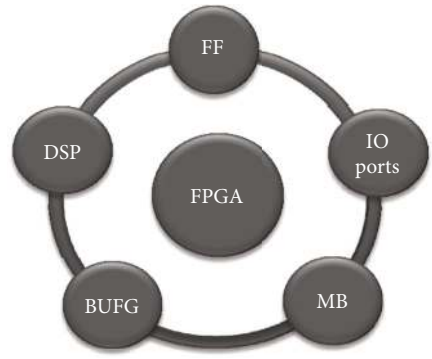

Figure 2: Building components of the FPGA device.

appropriate time [5–7]. Each input data is passed via the main memory to a processing device, comprising the four basic arithmetic functions (i.e., adding, subtracting, multiplying, and dividing) as well as certain logical operations such as data comparison and the selection of the required problem-solving method or a suitable alternative, on the basis of default decision criteria [8, 9].

Of all these features and vast application in the field of computing, CU is regarded as one of the suitable components which can be used for green computing as well as green communication; also, these green computing and green communication makes the environment sustainable. By reducing its power consumption, the CU can be made suitable for green applications. Therefore, the power-efficient CU will be the great choice for communication technologies [10, 11]. The power consumption of CU is optimized by its realization on FPGA devices. FPGAs are those devices which are made-up with semiconductor materials. It is called field programmable because it can be reconfigured/reprogrammed after its manufacturing [12–14]. FPGA devices are made-up with many components, and theses components are regarded as building components such as clock buffers (BUFGs), flip-flops (FF), input/output (IO) ports, memory blocks (MB), and digital signal processors (DSPs) [15, 16]. The building components of the FPGA device are represented in Figure 2.

1.1. Green Computing Communication. Green computing (GC) is a future generation environmentally friendly way of utilizing the computers, mobile device, and their resources. GC is also regarded as green information technology (green IT). In a broad way, GC term can also be coined as the method of designing, manufacturing, implementing, using, and disposing the mobile and computing peripherals and devices with least damage on environment resources. A brief idea of green computing is described in Figures 3 and 4.

Figure 3 shows the things which are associated with green computing. These are such power management of devices, designing of energy-efficient devices, processors, and other computer devices, cloud, and virtualization. In cloud and virtualization, we try to communicate the data with cloud server and access the data from cloud.

Figure 4 represents the utilities of GC. Generally, there 4 major points concerned with GC.

(i) Green use—it implies minimising power consumption of computer and mobile devices

(ii) Green disposal—it implies reusing and recycling of unwanted electronic devices

(iii) Green design—it covers the implementation and designing power and energy efficient devices

(iv) Green manufacturing—green manufacturing discusses about manufacturing computer and mobile devices with minimized waste

The communication of green devices with cloud and virtualization are known to be as green computing communication (GCC). The overview of GCC is shown in Figure 5.

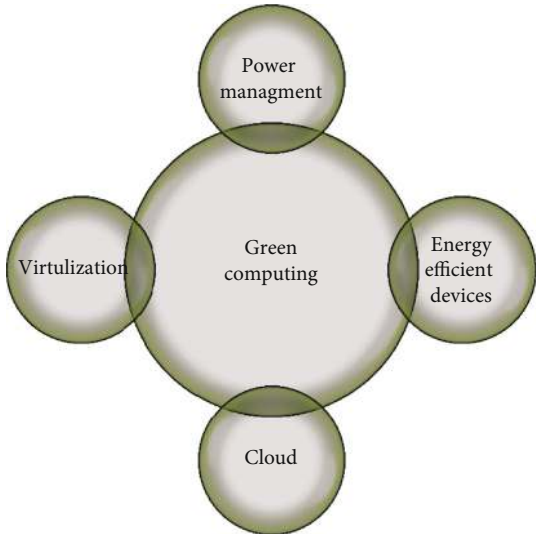

Figure 3: Idea of green computing.

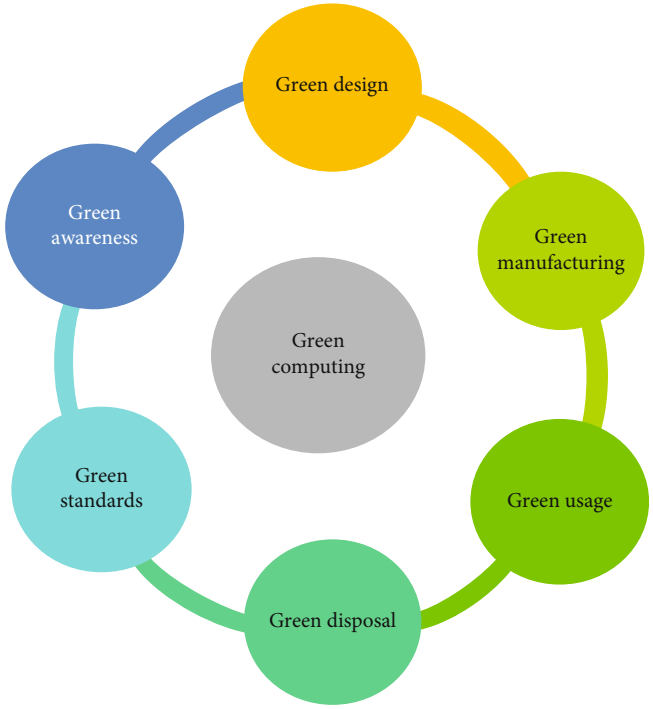

Figure 4: Utilities of green computing.

2. Related Work

With the help of IO standard, researchers have developed a power-efficient CU on Artix-7 FPGA with the support of various Low Voltage CMOS (LVCMOS) technologies. Input and output impedance are used to minimize the electricity consumption. Authors on Artix-7 FPGA design a power-efficient CU by modifying its frequency values. The shift in frequency values would change the CU's power consumption by FPGA [17]. Researchers are using I/O standards of Stub Series Terminated Logic (SSTL) to increase CU power consumption on 40 nm of Virtex-6 FPGA. The standards of the SSTL I/O correspond to the input load impedance w.r.t with the output load to minimize power consumption [18]. An electronic CU has been developed for the control of the vehicle system by FPGA authors. The RISC processor (ARM) is used in combination with FPGA to perform parallel computing tasks [19]. A power-efficient CU on Virtex and the Spartan family FPGA was introduced to support the concepts of Green Communication researchers [20]. Authors have designed the integration of green communication on Virtex 4, Virtex 5, and Virtex 6 FPGA [21] in an energy-efficient instruction register. In [22], FPGA was used by the authors to produce a true random number by

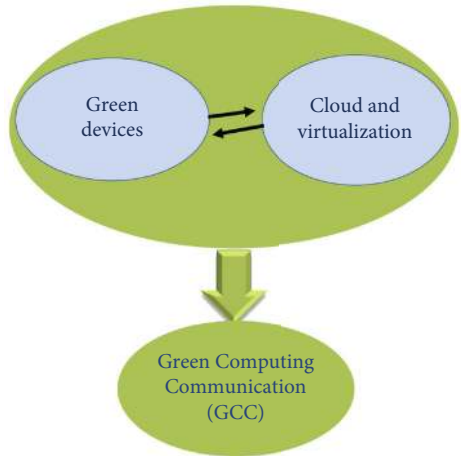

Figure 5: Green communications.

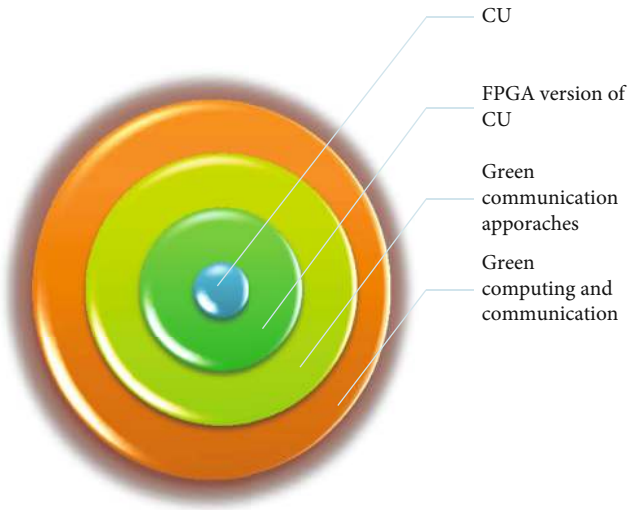

Figure 6: Green computing model of CU.

inducing metastability. In [23], photovoltaic simulation modules with FPGA were built in real time. In [24], researchers carried out a frequency change design of the arithmetic logic unit (ALU) for FPGA. Virtex-6 FPGA was used in [25] researchers to design a four-bit unregistered counter, allowing for clock and cutting. Random access memory (ROM) architecture for Virtex-6 FPGA was interfaced in [26]. In [27], researchers have used FPGA device to design a low power model for wireless data communication. In [28], researchers used energy-efficient techniques such as scaling the capacitance value of the capacitor of output load to design a green communication model of FIR Filter. With the help of Spartan-6 FPGA, authors have designed a green communication model of FIR Filter [29]. In [30], different families of FPGA devices have been used by the authors to develop a green UART for communication purpose. In [31], various FPGAs of the Spartan Group have been used for the implementation of energy-efficient transceiver model. In [32], researchers have developed a green CU with FPGA. For designing such model, authors have used HSTL and HSULIO standards. By using Pseudo Open Drain (POD) IO standards, an efficient FPGA model of ALU has been designed by the researchers [33]. To endorse green communication, researchers have designed an energy-efficient model of instruction register on FPGA [21]. In [34], different FPGAs and SOC has been utilized to enhance the performance of FIR filter for data communication and communication channel. In [35], LVCMOS IO standards are considered to execute a power-efficient UART for green computing and green communication. In order to endorse the green wireless communication, authors have projected the idea of Vedic multiplier design on FPGA devices by

Table 1: Resource utilization of CU on Zynq Soc.

Resource	Used	Available	Utilization %
LUT	14	230400	0.01
FF	4	460800	0.01
IO	23	360	6.39
BUFGs	1	544	0.18

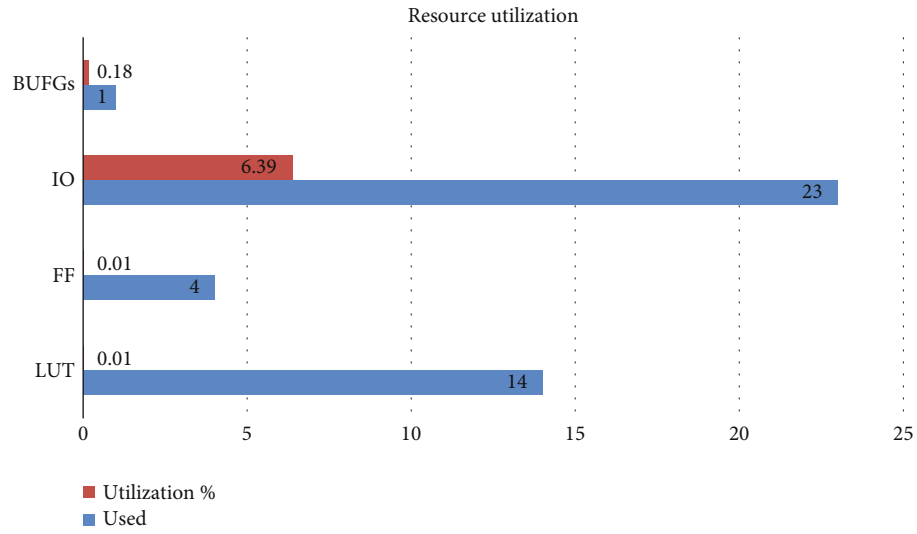

Figure 7: Resource utilization of CU on Zynq Soc.

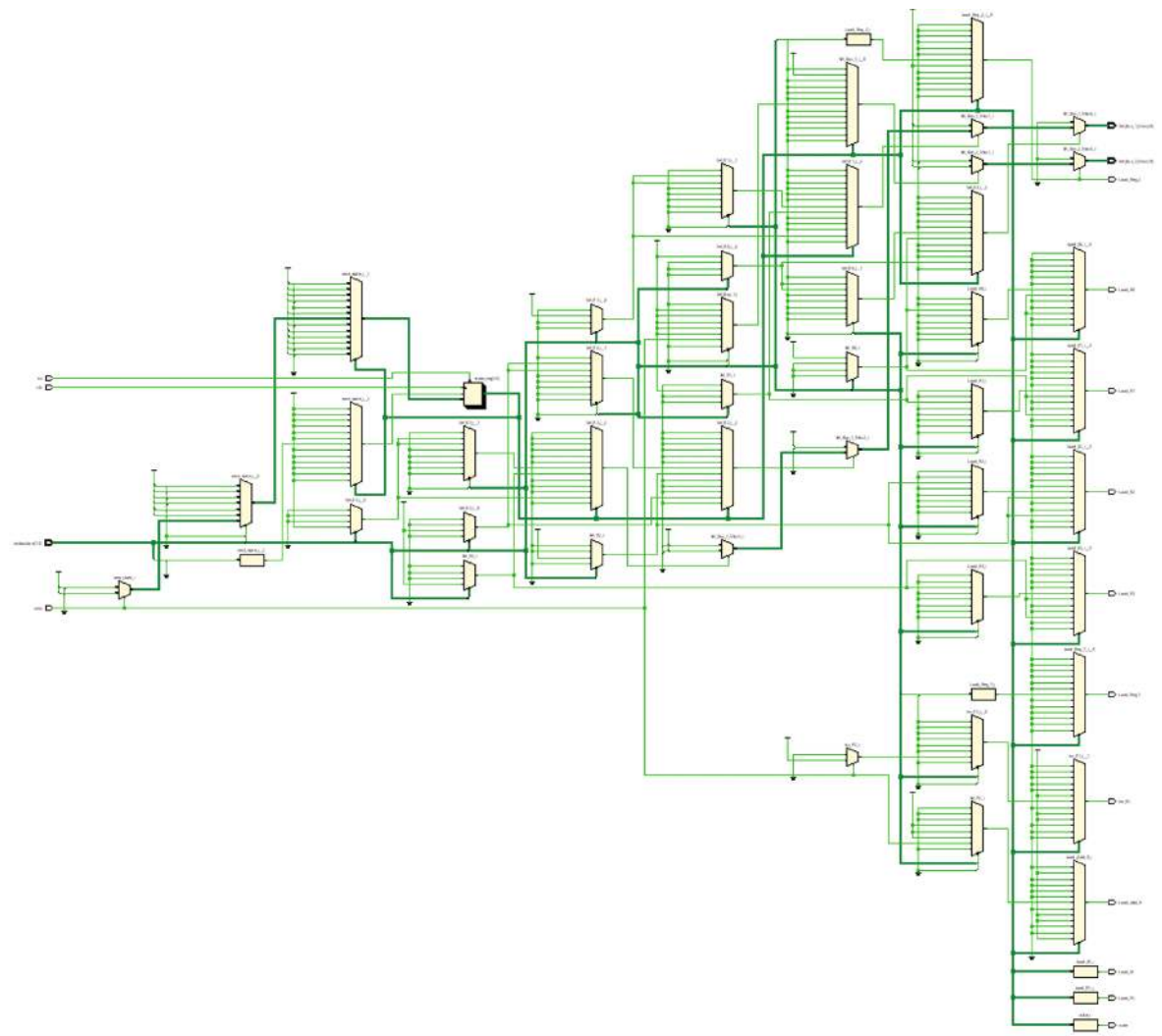

Figure 8: RTL of CU on Zynq SoC.

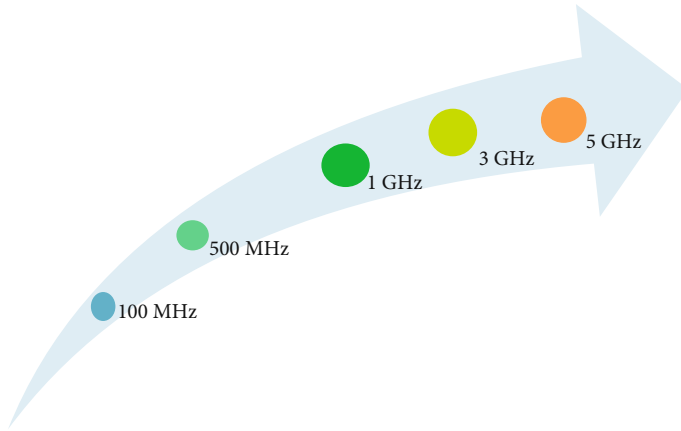

Figure 9: Frequency values for power calculation.

Table 2: Power calculation at 100 MHz.

On chips power	Power (W)
DP	0.006
SP	0.589
TP	0.595

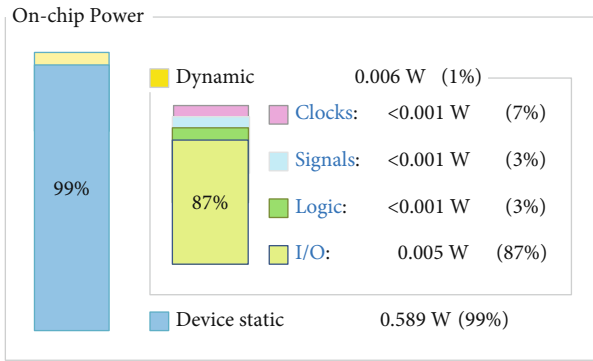

Figure 10: Power calculation at 100 MHz.

Table 3: Power calculation at 500 MHz.

On chips power	Power (W)
DP	0.030
SP	0.589
TP	0.619

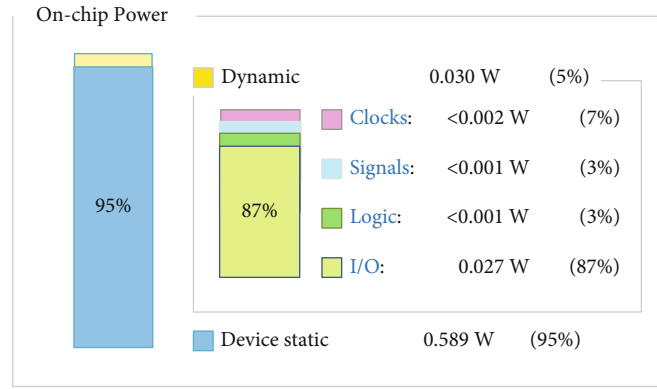

Figure 11: Power calculation at 500 MHz.

Table 4: Power calculation at 1 GHz.

On chips power	Power (W)
DP	0.214
SP	0.590
TP	0.804

reducing its power consumption with the help of several IO standards techniques [36]. In [37], researchers built a power-efficient green communications paradigm employing the data outage and BUFG MB DSP state information (CSI) channel FPGA FF IO ports. In [38], authors have developed a green FF design for green wireless communication using FPGA architectures. In [39], researchers have used 28 nm FPGA device to design a thermal efficient as well as power-efficient CU to incorporate with green communication. Kintex Ultra-scale FPGA has been taken for modeling an energy-efficient CU for promoting the green communication [40, 41]. Therefore, it has been observed that in the recent times, a lot of work has been done for incorporating the concepts of green communication and the energy/power efficient devices for future generations with the help of FPGAs, but a very few works have been done with respect to the implementation of the CU for green communication. Therefore, this work is all about the realization of CU on Zynq Ultra-Scale FPGA for promoting the values and ethics of green computing and green communication. The FPGA version of green computing model of CU is represented in Figure 6.

3. Experimental Setup

The ultrascale Zynq Soc FPGA board is used to set up the CU implementation. The VIVADO HLx architecture suite

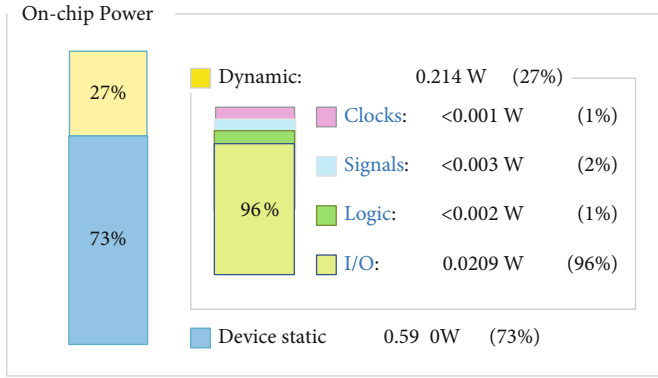

Figure 12: Power calculation at 1 GHz.

is the tool used to simulate CU on the FPGA board. Lookup tables (LUTs), flip-flops (FF), input-output (IO), and global buffers (BUFGs) are among the FPGA tools used to implement CU on the ultrascale Zynq Soc FPGA board, as shown in Table 1 and Figure 7 [42, 43].

The utilization of LUTs is 14, whereas 23-400 LUTs are available on FPGA boards for designing CU. Similarly, the utilization FF, IO, and BUFG are 4, 23, and 1, respectively, for designing CU on the ultrascale Zynq SoC FPGA. The Register Transfer Logic (RTL) of CU on Zynq SoC is shown in Figure 8.

4. Results and Discussion

In addition, FPGA system dynamic power (DP) and static power (SP) are correlated with the power measurement of CUs using the Zynq FPGA [44]. The summation of both DP and SP is the overall total power (TP) consumption. The dynamic power is the device's leakage power release.

The SP is the summation of I/O, logic (L/G), clock (CK), and signal (S/G). The power analysis of CU is done for five set of frequency value such as 100 MHz, 500 MHz, 1 GHz, 3 GHz, and 5 GHz, as shown in Figure 9.

4.1. Power Calculation for 100 MHz. For the frequency of 100 MHz, the SP of the device is 0.589 W, which is 99% of the TP consumption. The SP is the summation of I/O, L/G, CK, and S/G. Here, I/O power is 0.005 W, and the CK, L/G, and S/G power are less than 0.001 W. The DP, also called as leakage power, is 0.006 W, which is only 1% of the TP consumption. The TP for 100 MHz frequency is 0.595 W, as shown in Table 2 and Figure 10.

4.2. Power Calculation for 500 MHz. For the frequency of 500 MHz, the TP consumption is 0.619 W, which is the summation of SP and DP which are 0.589 W and 0.030 W, respectively. The SP consumes 95% of the TP while DP consumes 5% of TP, as shown in Table 3 and Figure 11.

4.3. Power Calculation at 1 GHz. For the frequency of 1 GHz, the SP of the device is 0.590 W, which is 73% of the TP consumption. The SP is the summation of I/O, L/G, CK, and S/G. Here, I/O power is 0.209 W, and the CK power is less than 0.001 W, while L/G and S/G power are 0.002 W and 0.003 W, respectively. The DP, also called as leakage power, is 0.214 W, which is 27% of the TP consumption. The TP for 1 GHz frequency is 0.804 W, as shown in Table 4 and Figure 12.

Table 5: Power calculation at 3 GHz.

On chips power	Power (W)
DP	0.184
SP	0.590
TP	0.773

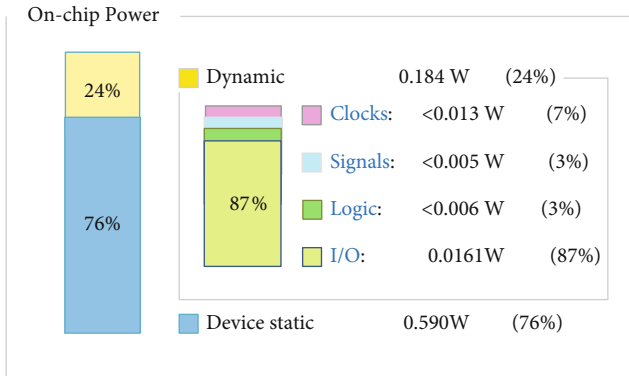

Figure 13: Power calculation at 3 GHz.

Table 6: Power calculation at 5 GHz.

On chips power	Power (W)
DP	0.303
SP	0.590
TP	0.893

4.4. Power Calculation at 3 GHz. For the frequency of 3 GHz, the TP consumption is 0.773 W, which is the summation of SP and DP which are 0.590 W and 0.184 W, respectively.

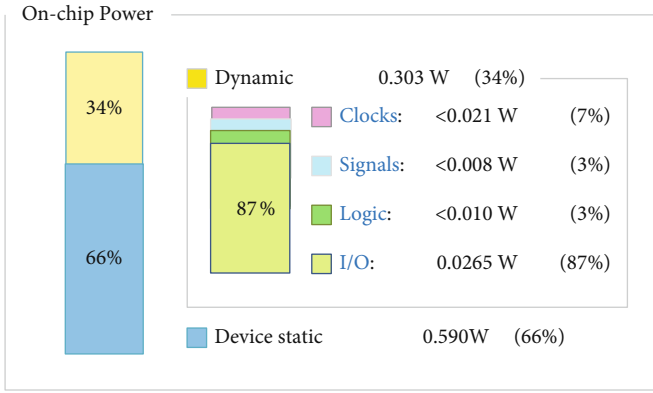

Figure 14: Power calculation at 5 GHz.

Table 7: TP consumption for different frequency.

Frequency	TP (W)
100 MHz	0.595
500 MHz	0.619
1 GHz	0.804
3 GHz	0.773
5 GHz	0.893

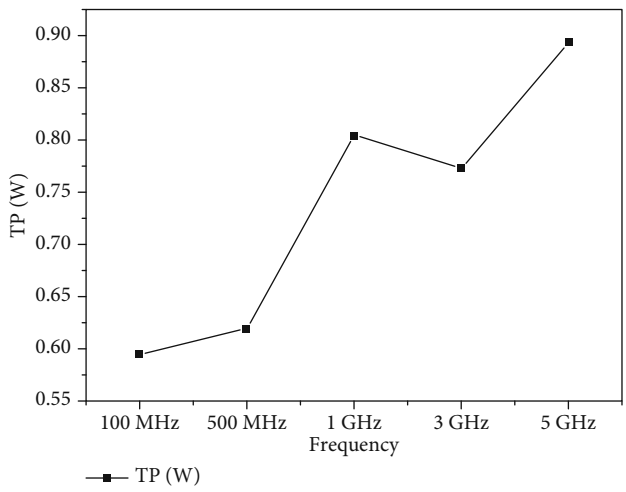

Figure 15: TP consumption for different frequency.

The SP consumes 76% of the TP while DP consumes 24% of TP, as shown in Table 5 and Figure 13.

4.5. Power Calculation at 5 GHz. For the frequency of 5 GHz, the TP consumption is 0.893 W, which is the summation of SP and DP which are 0.590 W and 0.303 W, respectively. The SP consumes 66% of the TP while DP consumes 44% of TP, as shown in Table 6 and Figure 14.

Form the power calculation for different values of frequency, it is found to be that the power consumption is maximum for higher values of frequency, i.e., 5 GHz and minimum for 100 MHz. The TP consumed for all frequency values is depicted in Table 7 and Figure 15. It is also observed that there is an increase of 4.03% in TP as the frequency is raised to 500 MHz from 100 MHz. Also, the increment observed for 1 GHz, 3 GHz, and 5 GHz, which are 35.12%, 29.91%, and 50.08%, respectively.

Table 8: Comparison of TP consumption.

References	TP (W)
[18]	2.636
[20]	0.756
[40]	0.725
Proposed work	0.595

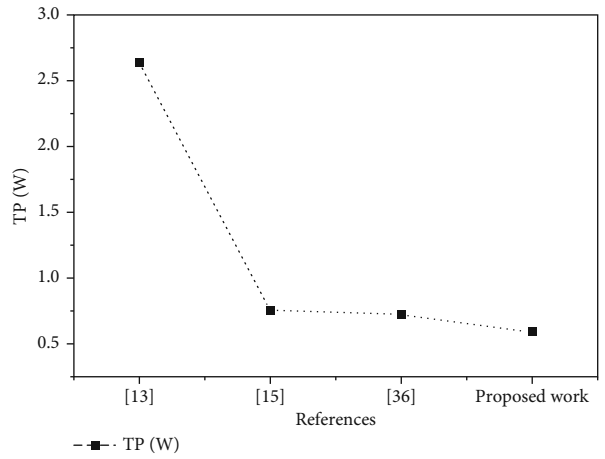

Figure 16: Comparison of TP consumption.

5. Comparative Analysis

In this section, a comparison of TP consumption has been made with the existing works of CU on FPGA and with this work. In [18], with Spartan 6 FPPGA, the TP for CU is found to be 2.636 W, while in [20, 40], the TP consumption for CU was 0.756 W and 0.725 W, respectively. In this work, CU is designed with Zynq SoC FPGA for incorporating with

green communication. The TP consumption with Zynq SoC is found to be optimized for 100 MHz frequency, i.e., 0.595 W. Therefore, it is observed that the TP consumption of CU is optimized in this proposed model. The TP of the proposed model is reduced by 77.42% from [18]. Similarly, the TP of this proposed model is reduced by 21.29% and 17.93% from [20, 40], respectively. The TP consumption of CU with existing models and the proposed model is shown in Table 8 and Figure 16, respectively.

6. Conclusion and Future Scope

The transition to green communication is critical in this period, as energy crises can be seen all over the world. As a result of this study, several steps have been taken to promote the concepts of green communication and power-efficient devices. The implementation of CU is carried out on the Zynq SoC ultrascale FPGA, and the simulation of the CU circuit, resource usage, and power analysis is carried out on the VIVADO Hlx Design Suite. It has been found that as the clock frequency of the circuit is increased, the power consumption decreases. As a result, it can be inferred that the overall power consumption is reduced when the clock frequency is low. Therefore, it is observed that there is an increase of 4.03% in TP as the frequency is raised to 500 MHz from 100 MHz. Also, the increment observed for 1 GHz, 3 GHz, and 5 GHz, which are 35.12%, 29.91%, and 50.08%, respectively. Also, the TP of the proposed model is reduced by 77.42% from [18]. Similarly, the TP of this proposed model is reduced by 21.29% and 17.93% from [20, 40], respectively, as shown in Figure 16. This CU circuit can be studied for other ultrascale and ultrascale plus FPGA devices in the future. Other power-saving methods, such as voltage, current, and capacitance scaling, can be used on the CU circuit as well. Impedance matching methods can also be used to make circuits more energy efficient with the aid of I/O specifications. For better performance, this FPGA design can later be converted to ASIC designs.

Data Availability

Data is available upon request.

Conflicts of Interest

The authors declare no conflicts of interest.

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