VLSI Implementations of Threshold Logic—A Comprehensive Survey

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***Abstract*—This paper is an in-depth review on silicon implementations of threshold logic gates that covers several decades. In this paper, we will mention early MOS threshold logic solutions and detail numerous very-large-scale integration (VLSI) implementations including capacitive (switched capacitor and floating gate with their variations), conductance/current (pseudo-nMOS and output-wired-inverters, including a plethora of solutions evolved from them), as well as many differential solutions. At the end, we will briefly mention other implementations, e.g., based on negative resistance devices and on single electron technologies.**

***Index Terms*—Integrated circuits, neural-network (NN) hardware, threshold logic, very-large-scale integration (VLSI).**

I. Introduction

RESEARCH on neural networks (NNs) goes back 60 years. The seminal year for the development of the "science of mind" was 1943, when the article *A Logical Calculus of the Ideas Immanent in Nervous Activity* by McCulloch and Pitts was published [31]. They introduced the first, very simplified, mathematical model of a neuron operating in an all-or-none fashion: the threshold logic gate (TLG). It computes the sign of the weighted sum of its inputs

$$f(x_1,\ldots,x_n) = \operatorname{sgn}(w_1x_1+\cdots+w_nx_n-\theta) = \operatorname{sgn}\left(\sum_{i=1}^{n} w_ix_i-\theta\right) \quad (1)$$

with w_i being the synaptic weight associated to x_i, θ the threshold and n the fan-in of the TLG.

It did not take very long for a hardware implementation to be developed. In fact, the *summing amplifier* from [42] precedes even [31] by submission date: May 1, 1941. It can be considered the first hardware implementation of a TLG. The patent details: "an electrical calculating device [...] for obtaining the sum of a plurality of electrical voltages" using "an electrical amplifier having a feedback. [...] by adjustment of the impedances connected in series with the various sources of voltage, any one or more of the sources may be, in effect, multiplied by any desired factor [...]" (see Fig. 1). In 1951, Minsky teamed with Edmonds and designed the first 40-neuron "neurocomputer," *Snark* [32]. Although it was an electromechanical implementation built of tubes, motors, and clutches, it successfully modeled the behavior of a rat searching for food in a maze. In 1957, Rosenblatt generalized the McCulloch–Pitts neuron inventing the perceptron [40]. During 1957 and 1958, Rosenblatt, together with Wightman *et al.*, constructed and successfully demonstrated the *Mark I Perceptron*. The Mark I Perceptron had 512 adjustable weights implemented as an $8\times8\times8$ array of potentiometers. Due to the successful presentation of the Mark I Perceptron, the neurocomputing field became a subject of intensive research. Shortly afterward, Bernard Widrow, together with his students, developed another type of neural computational element: the adaptive linear element (ADALINE) [46]. They used an electrically adjustable resistor called a *memistor*. Widrow also founded the first neurocomputer hardware company, Memistor Corporation, which produced neurocomputers during the early to mid 1960s. More details can be found in Nilsson's book *Learning Machines* [37]. The neurocomputer industry was born.

The general belief that a neuron is a TLG that fires when some variable reaches a threshold can be questionable as to whether such a drastic simplification can be justified. For answering that, the precise four-dimensional neuron model of Hodgkin and Huxley has been used; the threshold model has been tested on a spike train generated by the Hodgkin–Huxley model with a stochastic input current. The result was that the threshold model correctly predicts nearly 90% of the spikes, which justifies the description of a neuron as a TLG [23].

In the last decade, the tremendous impetus of very-large-scale integration (VLSI) technology has made neurocomputer design a very lively research topic. Research on hardware implementations of NNs in general, and TL in particular, has recently been very active. While there is a large body of literature on hardware implementations of NNs (see, for example, [11, Part E] and the many references therein), to the knowledge of the authors there are no up-to-date review papers on hardware implementations of TL since [15], [18], [47], and [48]. Books on TL have been written some time ago [17], [28], [34], with only

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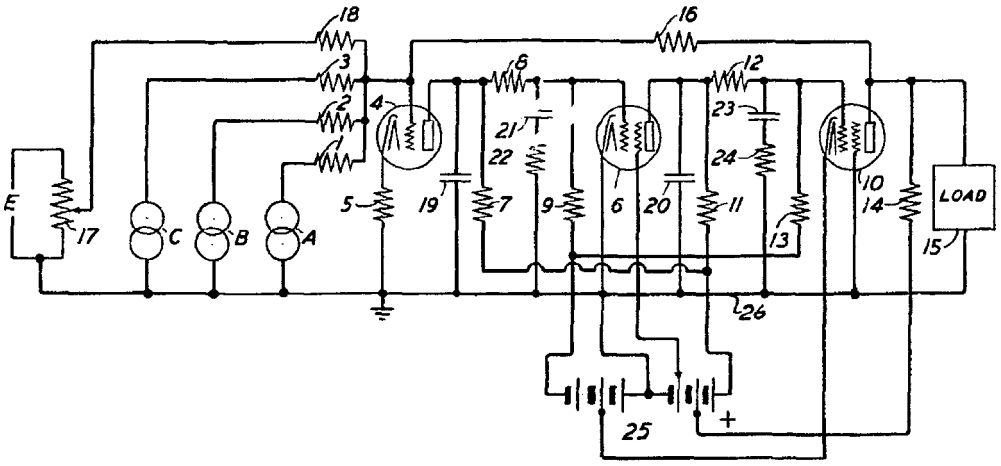

Fig. 1. Summing amplifier from [42].

one recent chapter [1] and a forthcoming book [4], as exceptions. Particular TL implementations using either currents [8] or a few capacitive solutions [7], [38] are the exception rather then the rule. Also, they have covered only particular subclasses of solutions. Even more, nanoelectronics devices such as those based on single electron technology (SET) or on negative resistance devices (NRDs) have not been included [12], [33], [39]. Besides, there are many theoretical results showing that TL circuits (TLCs) are more powerful/efficient than classical Boolean circuits (BCs; see [5] and [3]). These have been another motivation to investigate various VLSI implementations.

One important aspect for NNs is their adaptive behavior, but in this in-depth review paper we will focus only on the many different approaches that have been tried for implementing TL in silicon. Effectiveness of TL as an alternative to modern VLSI design is determined by the availability, cost, and capabilities of the basic building blocks. In this sense, many interesting circuit concepts for developing standard CMOS-compatible TLGs have been explored.

As the number of different proposed solutions and fabricated chips reported in the literature is on the order of hundreds, we cannot mention each here. Instead, we will try to cover important types of architectures and present representative examples—although some readers may at times disagree with our choice. The paper is structured in four main sections, Sections II–V. Each is dedicated to a different design approach (such as in [24]). Section II covers a few CMOS solutions. Section III is dedicated to capacitive implementations, dealing both with floating gate approaches and with switched capacitor solutions. Section IV details many conductance/current implementations starting from pseudo-nMOS and the output-wired inverters. It presents many solutions that have evolved from them, as well as a large variety of differential solutions. Finally, Section V is dedicated to several other implementations, including SET and resonant tunneling device (RTD). In most cases, the various solutions discussed are sorted chronologically by order of their publication date; however, in some cases, the order would somehow be different by submission date.

To keep the paper's length reasonable, the early days of TL implementations (i.e., when the technologies were TTL, ECL, I^2L, and nMOS), although quite instructive, will not be covered here (the interested reader should consult [2]). However, it is worth mentioning here that many technologies have been proposed and investigated. The very early implementations were

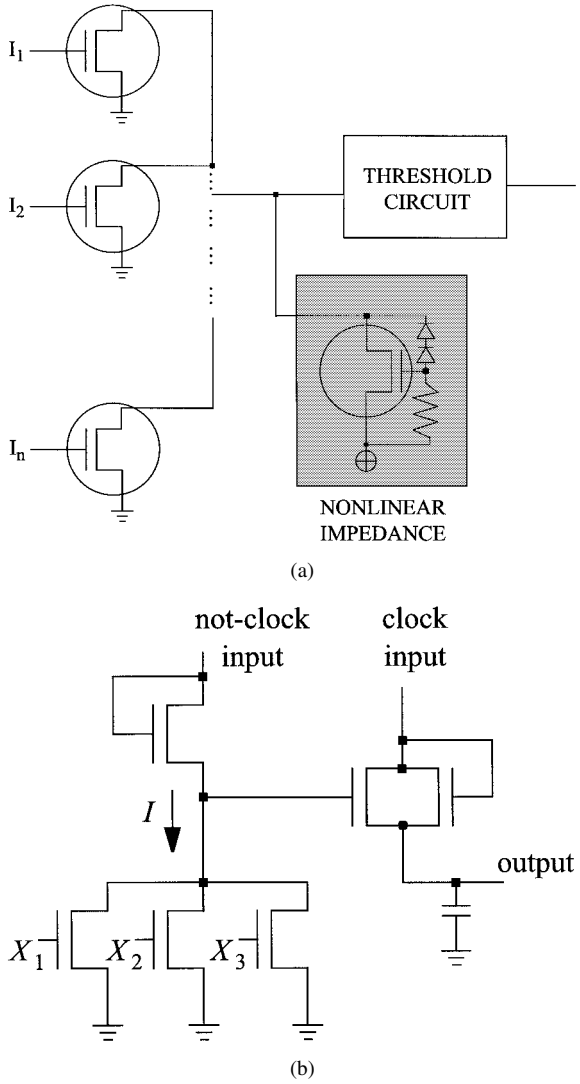

Fig. 2. MOS implementation from (a) [16] and (b) [29].

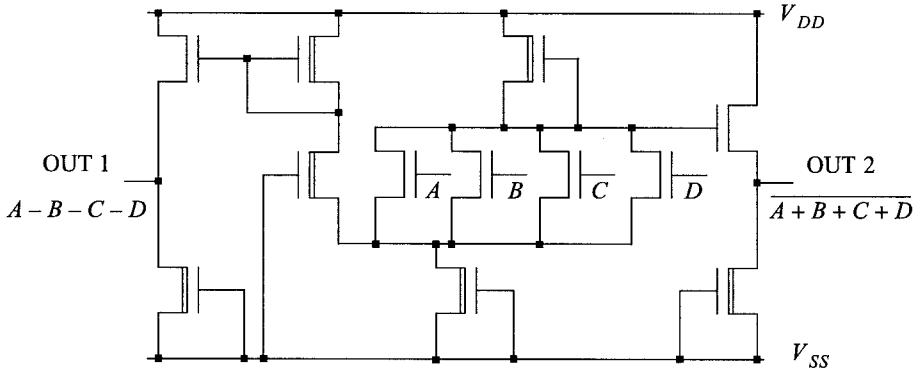

Fig. 3. nMOS solution from [10].

based on magnetic cores [22], [41] or on multiple coil relay circuits [43]. Parametron circuits [13] were followed by neuristor circuits [30]. Other technologies considered have been those based on Josephson junction [20], fluidic [9], or (for very low power) charge-coupled devices [45]. The use of tunnel diodes [27] and NRDs [44] was advocated as early as 1959 [26], [14]. A few representative MOS implementations are [6] (to be detailed in Section III.B), [16] [Fig. 2(a)], [29] [Fig. 2(b)], and [10] (Fig. 3). Obviously, the evolution of integrated circuits has made it so that the enduring implementations have been those based on resistor–transistor and capacitors–transistor circuits (or their variations). In spite of all these efforts, only a very small number of TLG implementations (or their variations) have been used commercially: MIPS R2010 [19], SUN Sparc V9 [25], a CMOS fingerprint sensor array [21], and recently the Itanium 2 microprocessor [35], [36].

In the conclusion section, we will discuss and compare the different implementations and will comment on the future directions of research.

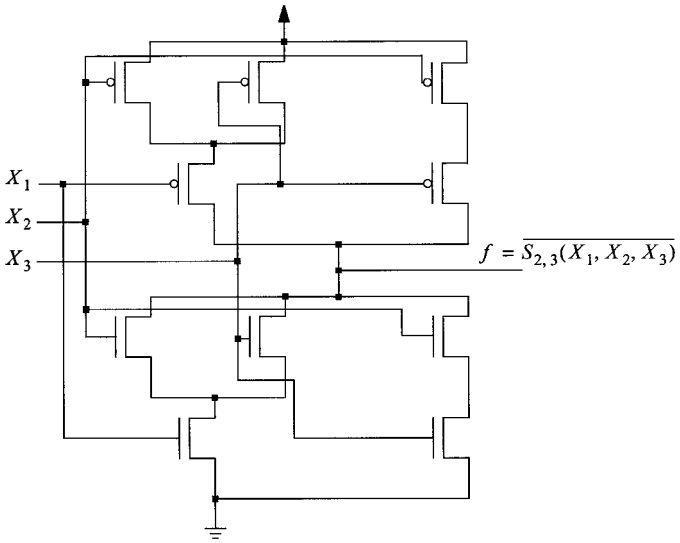

Fig. 4. CMOS solution for MAJORITY functions from [49].

II. CMOS Solutions

The solutions presented in this section are totally different from the other solutions, which each have represented a distinct weighted sum (of inputs) by an analogue value (voltage, charge, or current). In principle, this implies static power dissipation, which is hardly acceptable. Currently, low-power solutions are at a premium and three different low-power CMOS solutions will be detailed further.

The first pure CMOS solution is probably due to Hampel [49] (Fig. 4). The CMOS devices form a plurality of TLG configurations having MAJORITY logic functions with near-symmetrical switching delay times. MAJORITY functions are threshold logic functions (TLFs) that have identical (unit) weights. Any TLF can be represented as a MAJORITY function by repeating/complementing its inputs. Hence, the gate can implement arbitrary TLFs by tying together several inputs. Corresponding gate terminals of individual MOS devices within the identical nMOS and pMOS complementary stacks are commonly connected to the input signals. The fact that the nMOS and pMOS stacks are alike leads to symmetrical switching delay times. The gate has low power consumption and large noise margins. A variation of this type of gate can be found in almost any textbook on VLSI as part of the "mirror adder." The only disadvantage is that larger fan-in gates are slow due to the large number of series transistors and the larger capacitance. Even more, when implementing arbitrary TLF, the fan-in is reduced because several inputs have to be tied together for implementing weights differently from the unit weight.

A NULL convention logic (NCL) gate [51]–[53] receives a plurality of inputs, each having an asserted state and a NULL state. The TLG switches its output to an asserted state when the number of asserted inputs exceeds a threshold number. The TLG switches its output to the NULL state only after all inputs have returned to NULL. Signal states may be implemented as distinct voltage or current levels. This approach implements m-of-n TLGs with hysteresis. This gate is a generalization of both a Muller C-element (n-of-n) and a Boolean OR (1-of-n) gate. NCL is an asynchronous delay-insensitive logic-design methodology. Several implementations are possible: static (Fig. 5 shows an n-of-n gate), semistatic, and dynamic. The gate has low power and large noise margins, being reasonably fast for small fan-ins (the large number of transistors in a series slows it down for larger fan-ins).

Finally, another low-power solution based on a pass-transistor logic style has been presented in [50]. It offers an attractive alternative to pure CMOS solutions. In particular, complementary

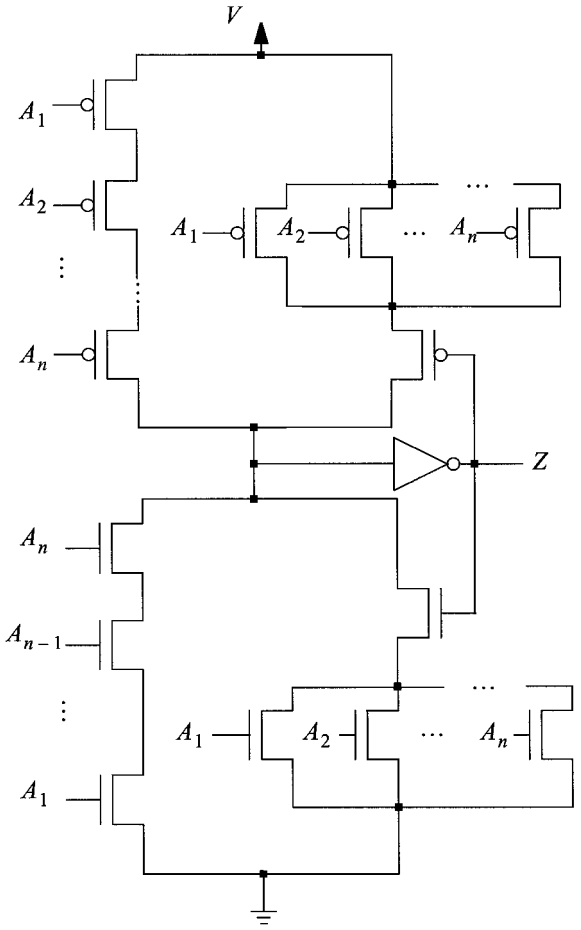

Fig. 5. Static "NULL convention threshold logic" of an n-of-n gate [51].

pass-transistor logic (CPL) is a well-known low-power logic design style. A steering circuit, which produces all TLFs for an n-input logic function, was detailed in [50]. Weights different from 1 are implemented by modifying the diagonal connection pattern in the steering circuit (instead of tying together as many inputs as given by w_i). Fig. 6 shows the steering logic circuit realizing all the six possible TL functions that can be obtained with the set of weights $[1, 1, 2, 2]$. A distinguishing characteristic differentiating this approach from others TLG realizations is that pass-transistor-based ones depend only on the number of variables, not on their associated weights. However, as the CPL-based design is a class of static pass-transistor logic, it inherits problems that are specific to this class of circuits.

III. Capacitive Implementations

The concept underlying capacitive TLGs is the use of an array of capacitors to implement the weighted sum of the inputs. Distinct circuits structures have been proposed, which differ in the way the value of the threshold is set and in the circuit techniques used to carry out the comparison involved in determining the output value. Capacitive TLGs can be classified into two major groups: Neuron MOS (νMOS), also known as multi-input floating-gate transistor (MIFG or MFMOS) and CTL. Although closely related, these two original approaches were different at the beginning: static versus clocked and different mechanisms for setting the threshold value, while their current developments have become increasingly similar. Several comparisons, such as [7] and [38] (see also [60]), draw the following conclusions:

- The operation of the νMOS is simpler than CTL.
- The maximum fan-in attainable by νMOS is an order of less magnitude than that of the CTL gate, which is less limited by process variations.
- Both solutions exhibit large power consumptions, as the floating gate voltage of the primary inverter in the comparator chain causes direct current (dc), an exception being the Floating-Gate UV-programmable MOS (FGUVMOS) circuit [66].
- The delay has a logarithmic dependence with respect to large fan-ins (fan-in ≤ 255 in [60], fan-in ≤ 64 in [38]), while for small fan-ins (fan-in ≤ 20 in [7]) the behavior of the normalized delay looks linear: $1 + 0.35n$ (n being the fan-in).

A. Switched Capacitor

Originally introduced in 1987, the main idea was to use switched capacitors, switches, and inverters and to take advantage of the inherent saturation of the inverters to implement the neuron nonlinearity without additional elements [63], [64]. This first approach required a somewhat complex three-phase clock, as shown in Fig. 7.

The principle of capacitive synapse was also presented in [54] and [55], with the same three-phase clock. It has quickly evolved into a simpler two-phase clock solution [60], known as the CTL gate. Its conceptual circuit schematic is shown in Fig. 8 for an n-input gate. It consists of a row of capacitors $C_i, i = 1, 2, \ldots n$, with capacitances proportional to the corresponding input weight $C_i = w_i \times C_u$ and a chain of inverters that functions as a comparator to generate the output. This TLG operates with two nonoverlapping clock phases: Φ_{R} and Φ_{E}. During the reset phase, Φ_{R} is high and the row voltage V_R is reset to the first inverter threshold voltage, while the bottom plates of the capacitors are precharged to a reference voltage V_{ref}. Evaluation begins when Φ_{E} is at a logic 1, connecting the gate inputs to the bottom plates of the capacitor. As a result, the change of voltage in the capacitor top plates is given by $\Delta V_R = [\sum_{i=1}^{n} C_i(V_i - V_{\mathrm{ref}})]/C_{\mathrm{tot}}$ where C_{tot} is the total row capacitance including parasitics. Choosing adequate definitions for V_{ref} and C_i as functions of the input weight and threshold values, the above relationship can be expressed as $\Delta V_R = [\sum_{i=1}^{n}(w_i x_i - \theta)C_u V_{\mathrm{DD}}]/C_{\mathrm{tot}}$. In combination with the comparison function of the chain of inverters, this gives the TL operation $V_O = V_{\mathrm{DD}}$ if $\sum_{i=1}^{n} w_i x_i \geq \theta$ and $V_O = \mathrm{GND}$ if $\sum_{i=1}^{n} w_i x_i < \theta$. Between two consecutive reset phases, a large number of input vectors can be processed.

Experimental results from different CTL gates fabricated in standard CMOS technology [56]–[58], [60] have shown the proper functionality of this type of TLG and its large fan-in capability (gates with fan-in $= 255$ have been simulated). This later feature is due to the auto-offset cancellation technique widely used in chopper-type CMOS comparators. Originally, CTL gates required a double-poly process, but some developments (such as dynamic and differential CTL [56]) use the MOS cap with a small penalty on the fan-in (fan-in ≤ 64).

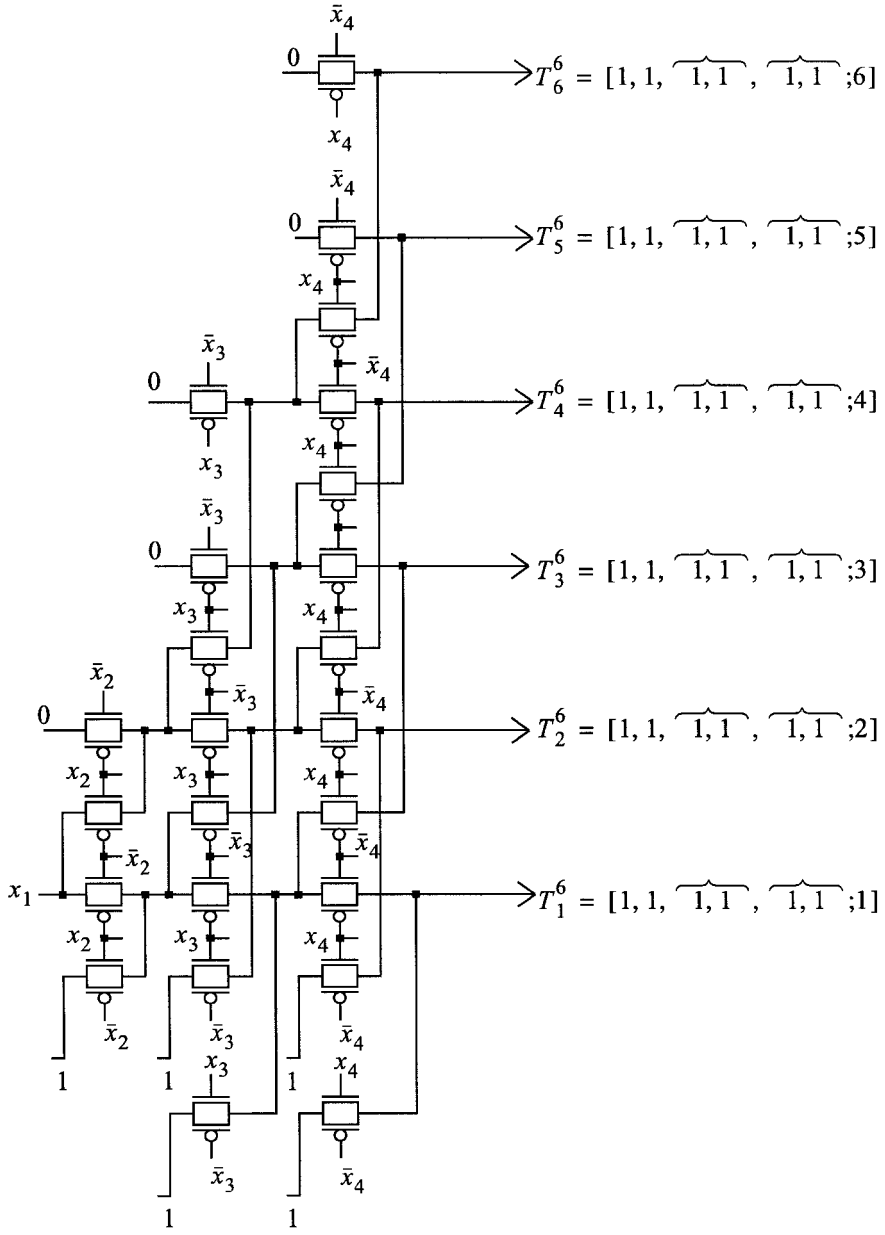

Fig. 6. Steering logic network implementing $[1, 1, 2, 2; k]$ for $k = 1, \ldots, 6$, from [50].

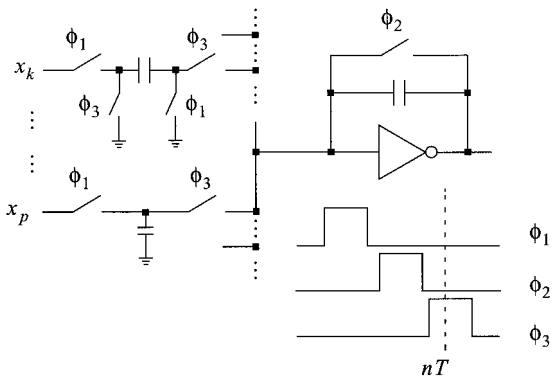

Fig. 7. Switched capacitor from [63] and [64].

CTL gates have a simple regular structure and are able to implement large fan-ins, while their main drawbacks are large delays, large area, dc power consumption, and the threshold value programming mechanism. The reset time grows with the fan-in of the gate, due to the large capacitance, and can become quite large (thousands of evaluation phases) [38]. Propagation delay is logarithmic in the number of inputs and has a strong dependence on the unit capacitor [60]. The estimated area of the unit capacitor is equivalent to several minimum sized inverters; hence, the capacitor array occupies a large area. Due to the linear operation of the sense amplifier, the power consumption is high. Several developments proposed for overcoming CTLs limitations are summarized below. The fact that the threshold value is set by an analog reference voltage complicates its integration. In addition, each CTL gate may require a different reference voltage; thus, it is very difficult if not impossible to build circuits with a large number of CTL gates. This problem is solved by the improved CTL gate [56], which operates exclusively with binary input logic levels. Another solution to

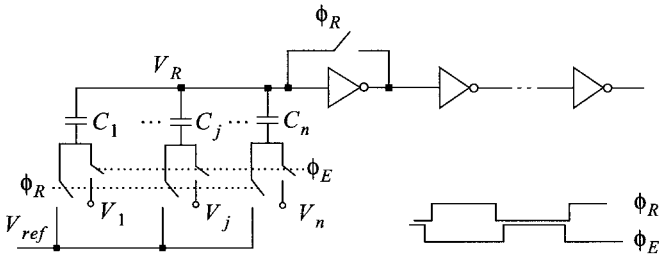

Fig. 8. CTL from [60].

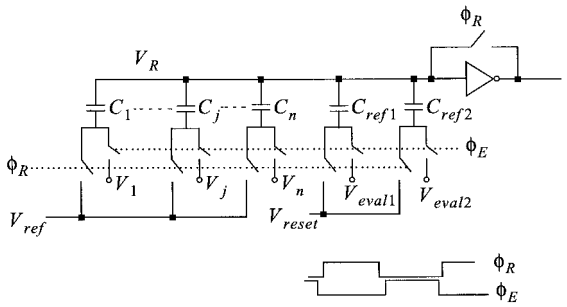

Fig. 9. Capacitor-programmable capacitive threshold logic (CP-CTL) from [61] and [62].

this problem is the CP–CTL [61], [62], which does not rely on the presence of additional external voltages. Fig. 9 depicts its schematic. The original CTL gate is augmented with a number of capacitors. The programming of the gate is now achieved by setting $V_{\rm ref}, V_{\rm eval1}, V_{\rm eval2}$, and $V_{\rm reset}$ to readily available voltage levels. Different combinations of ground (GND), $V_{\rm DD}$, and $V_{\rm DD}/2$ (programming methods) can be used.

Finally, another variation called balanced-CTL (B-CTL) [59] is shown in Fig. 10. The requirement for a very precise reference voltage is eliminated by implementing functions with thresholds equal to 0. This is not a restriction on the class of TLFs that can be implemented, since it is well known that any TLF can be converted into an equivalent TLF with threshold equal to zero by inverting certain inputs and changing the sign of their associated weights [34]. The basic structure is formed by two banks of capacitors (Bank A and Bank B in Fig. 9). Both banks are connected to a differential amplifier that determines which bank has a larger number of inputs at logic one. That bank has a higher voltage level on its common line. This gate implements TLFs, with thresholds equal to zero, if the inputs having positive weights are connected to one bank and the inputs having negative weights are connected to the other bank. One additional half capacitor $(\mathrm{CA}_0, \mathrm{CB}_0)$ unbalances the voltage levels at the amplifier inputs in the case that both banks have an identical number of high-level inputs. B-CTL gates operate from one clock that switches the gate between two states: reset and evaluation. B-CTL gates are reported to be faster than CIAL gates [157] (to be described in Section IV-D). Their main characteristics are high fan-in and low power consumption.

B. Neuron-MOS Transistor

The first CMOS capacitive solution was presented in 1966 [6] and can be seen in Fig. 11(a). It was rediscovered 25 years later [82], when its integration led to the well-known

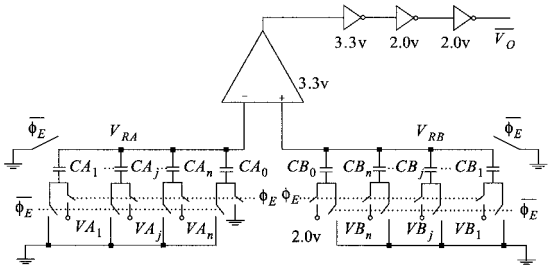

Fig. 10. B-CTL from [59].

Neuron-MOS (νMOS) transistor. This transistor has a buried floating polysilicon gate and a number of input polysilicon gates capacitively coupled to the floating gate. The voltage on the floating gate becomes a weighted sum of the voltages on the input gates and controls the current in the transistor channel. The most simple νMOS-based TLG is the complementary inverter using both pMOS and nMOS νMOS devices [81], [83]–[86]. A schematic of this TLG is shown in Fig. 11(b). The floating gate is common to both the pMOS and nMOS transistors and the input gates correspond to the TLG inputs $x_1, x_2, \ldots, x_n$. The weights are proportional to the ratio between the corresponding input capacitance C_i (between the floating gate and each of the input gates) and the total capacitance (including the transistor channel capacitance) between the floating gate and the substrate $C_{\rm chan}$. The voltage on the floating gate is given by $V_F = (\sum_{i=1}^{n} C_i \cdot V_{x_i})/C_{\rm tot}$, where $C_{\rm tot} = C_{\rm chan} + \sum_{i=1}^{n} C_i$. When V_F becomes higher than the inverter threshold voltage, the output switches to logic 0.

In the case of the simple static $\boldsymbol{\nu}$MOS, the gate's threshold is adjusted via additional threshold-setting capacitors. It is obvious that νMOS TLG is very simple and very compact. However, there are a number of problems. Degradation in the long-term stability is anticipated due to the use of a floating gate. Sensitivity to parasitic charges in the floating gate and to process variations could limit its effective fan-in, unless adequate control is provided. In particular, ultraviolet light erasure is required for initialization/reprogramming. Static νMOS gates have dc power consumption; different schemes have been proposed to alleviate at least some of these problems.

A solution for diminishing the power dissipated by a simple (conventional) static νMOS TLGs is represented by the deep-threshold $\boldsymbol{\nu}$MOS TLG [77]. This gate is composed of a deep-threshold $\boldsymbol{\nu}$MOS inverter and a two-staged CMOS buffer. The deep-threshold inverter is built of nMOS and pMOS transistors that have threshold voltages large enough such as both transistors are off for any of the multiple voltage levels on the common floating gate. Consequently, there is no dc current, paving the way for impressive power reductions. A power reduction down to 3.33% (when compared to conventional static $\boldsymbol{\nu}$MOS TGL) has been reported in [77]. Unfortunately, the penalty that has to be paid is an almost threefold increase of the delay. This can be somewhat compensated by buffering the output signal with a combination of a small-sized low-capacitance inverter followed by a conventional inverter (output buffer). Overall, the power-delay product for the deep-threshold $\boldsymbol{\nu}$MOS TLG is six times better than conventional static $\boldsymbol{\nu}$MOS TLG and 3.5 times better than standard CMOS technology.

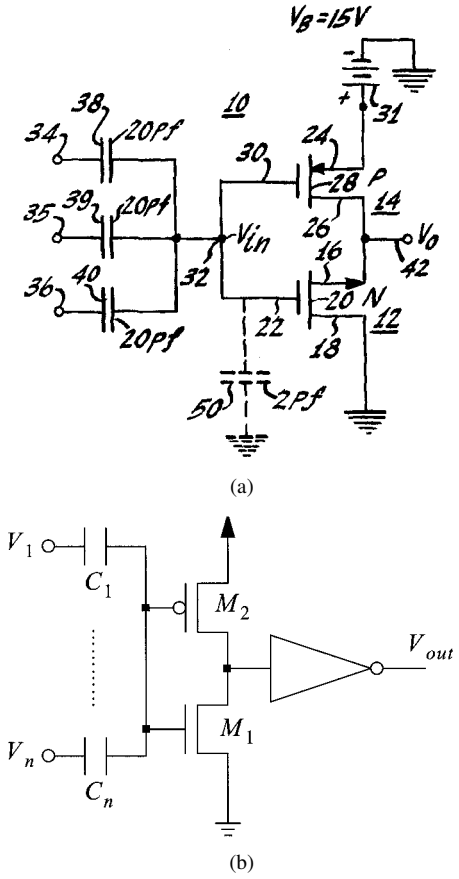

Fig. 11. (a) First CMOS capacitive solution from 1966 [6] and (b) the neuron MOSFET (neuMOS or νMOS) complementary νMOS inverter (static gate) [82]–[86].

In the clock-controlled νMOS TLG [75], [76], a clock-driven switch is attached to the floating gate to initialize the floating-gate charge (reset phase). This switch short circuits the floating gate and the inverter output, thus biasing the inverter at the most sensitive point of the inverting characteristics (see Fig. 12). This is the same auto-offset cancellation technique used for CTL gates (and in chopper-type CMOS comparators). At the same time, each input capacitors is set to an analog voltage V_{ref} [Fig. 12(a)] or to either GND or V_{DD} [Fig. 12(b)] such that the logical threshold of the gate is correlated with the physical threshold of the inverter. This means that, in each reset phase, the floating-gate charge is refreshed, avoiding the problems due to parasitic charges and long-term stability. The inverter threshold is also automatically readjusted, reducing sensitivity to process and ambient parameters variations, and allowing for larger fan-in gates. As an example, static νMOS TLGs for MAJORITY with up to nine inputs are possible (typically the fan-in of a static νMOS is limited by 12), while clocked νMOS can reach up to 30 inputs. The gate is not very fast: a neuron with 32 synapses of 5-b accuracy in 0.8 μm CMOS exhibit delays in the 3–17-ns range [78]. A similar concept is used by the controlled floating-gate devices (CFGDs) [65]. These dynamic versions have relatively high static power and might require multiple phase clocks.

The static power consumption of the basic νMOS TLG can be eliminated and its speed increased by a current comparison between a νMOS transistor and a reference device using a positive feedback circuit. Many different configurations that take advantage of this concept have been reported [75]. One example is the configuration called sense-amplifier νMOS TL [76] [Fig. 13(a)]. It applies a current-controlled latch-sense amplifier circuit to the basic νMOS TLG. Variations can be found in [88] and [89], followed by [79], [80], [87], and [90], [Fig. 13(b)]. They use a solution similar to the digital comparator based on the clock-coupled inverters introduced in [161]. (This is a differential conductance solution to be described in Section IV-D.) However, the authors mention that this solution is valid only when it is applied to gates having very large fan-ins (125–256). In [89], significant speed improvements (100 to 500 MHz) and power savings for the νMOS gate detailed in Fig. 13(b), over static νMOS gates, are reported. In [80], a very thorough analysis with respect to parameter variations, namely coupling capacitances of the floating gate and the sensing amplifiers of νMOS TLGs using a dynamic comparator latch for sensing, is carried out. The dominant mismatch originates from the input–offset voltage variations of the sensing circuits. Measured results show that the most critical components are the comparators circuits. Improved noise margins can be traded off for increased layout areas and increased power consumption (due to increased capacitances). The conclusion is that this is a problem that will be exacerbated by future CMOS technologies, since lower supply voltages and increased device mismatch will have a diminishing effect on the threshold window, sensing margins, signal-to-noise ratio (SNR), and reliability. In addition, it is claimed that a careful comparison with the area and power consumption of a standard CMOS logic circuit is absolutely necessary and that the use of νMOS gates is not always advisable. However, they explicitly mention that there are applications in which floating gate MOS devices can be employed advantageously, such as TLCs with low logic depth implemented in fault-tolerant architectures requiring high functional densities (e.g., data-processing architectures in image sensors).

A variation, called CMOS capacitor coupling logic ($\mathbf{C^3L}$), uses the capacitor coupling technique and a current sense amplifier [72] (Fig. 14). These circuits do not have an offset cancellation mechanism, but fluctuation in device parameters can be compensated by the differential configuration.

Fig. 15(a) shows the structure of yet another TLG, based on a charge-recycling differential sense amplifier. It is called charge-recycling threshold logic (CRTL) gate [69], [68]. The inputs are capacitively coupled onto the floating gate of transistor M_5 and the gate voltage of transistor M_6 sets the threshold. A CRTL gate has two operation phases controlled by a single-phase clock. When $\bar{E}$ is high, the output voltages are equalized. When E is high, the outputs are disconnected and the differential circuit (transistors M_5, M_6, and M_7) draws different currents from the OUT and $\overline{\text{OUT}}$. The sense amplifier is activated and amplifies the difference of potential between OUT and $\overline{\text{OUT}}$, accelerating the transition. Thus, it evaluates whether the weighted sum of the inputs is greater or less than the threshold. It is based on a charge-recycling asynchronous sense-differential amplifier (ASDL) [73], [74]. The symmetry of the layout is important. CRTL gates exhibit high speeds and are suitable for high fan-ins, while also having low power consumption. In fact, CRTL gates achieve the highest speed and 15–20% lower

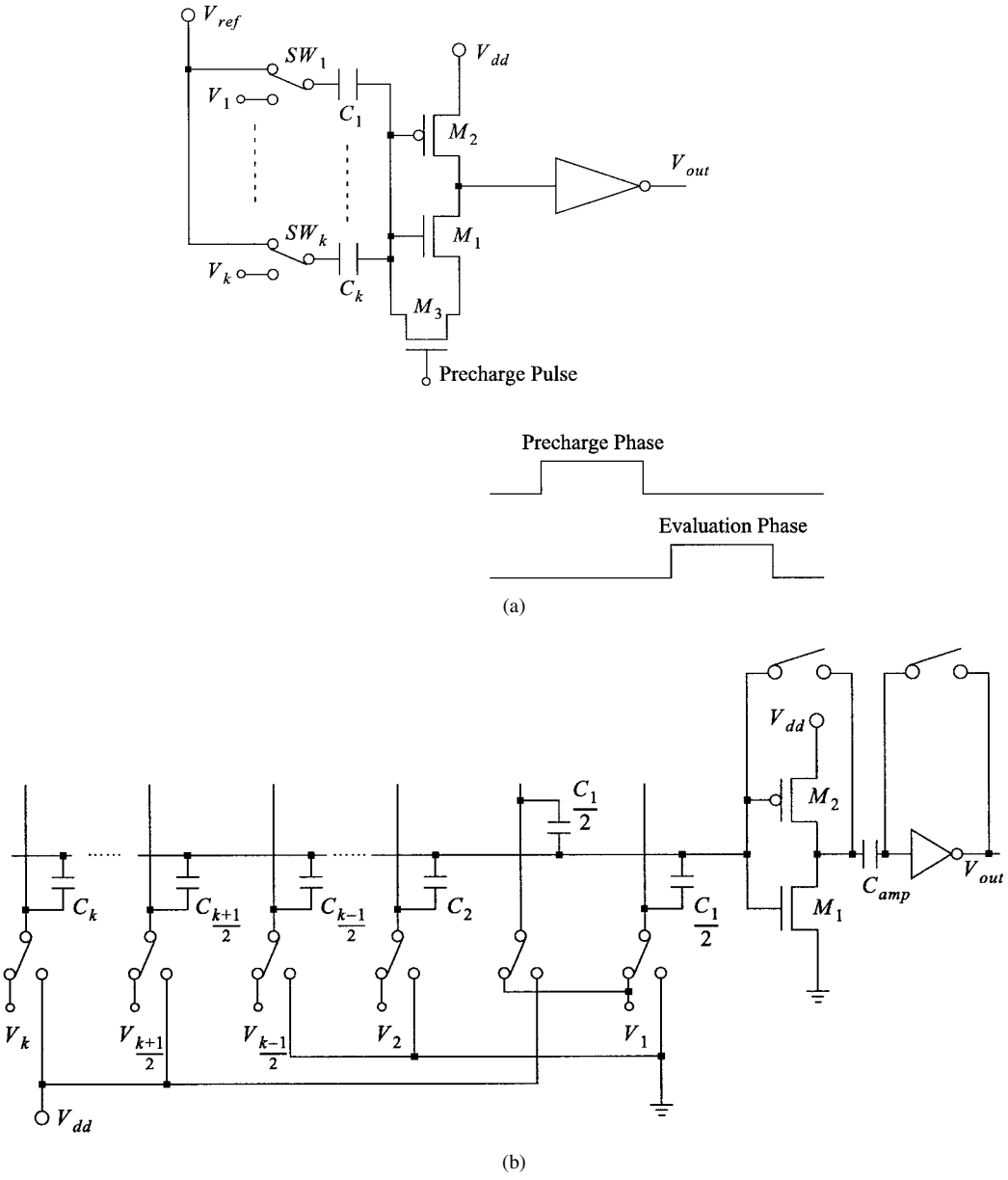

Fig. 12. (a) Clock-controlled neuron-MOS (with reference voltage) from [75]. (b) Clock-controlled neuron-MOS without reference voltage from [78].

power consumption when compared with clocked νMOS [76], C^3L [72], and LCTL [152] (to be described in Section IV-D). CRTL gates have been tested for process variations at 45 corners and seem to be robust. A 4-b carry look-ahead adder using CRTL gates was implemented in a 0.25 μm double poly CMOS process [68]. It can be operated at frequencies in excess of 400 MHz. At 100 MHz and $V_{\rm DD} = 2$ V, it dissipates 0.5 mW, i.e., 15–20% lower power dissipation than other capacitive TLGs.

Very recently, a novel self-timed threshold logic (STTL) has been proposed [70], [71]. It describes a "capacitor-sharing" technique for significantly reducing the occupied area, which can be easily applied to other νMOS implementations. The fact that STTL (and CRTL) can include negative weights without requiring inverted inputs also has clear area benefits. The self-timing idea comes from asynchronous circuits, the goal being to eliminate the clock and, thus, to reduce power consumption (a self-timed power-down mechanism applied to conductance TLGs [124]–[126], [128] will be detailed in Section IV-C). The gate is based on the cross-coupled nMOS transistor pair, M_3 and M_4 [Fig. 15(b)]. Precharge and evaluate are specified by an enable signal: E and $\bar{\rm E}$. Two current mirrors, M_8-M_1 and M_9-M_2 are used. Because the capacitances of node A and B have to be matched, the two buffering inverters have to be identically sized. The enable signals E and $\bar{\rm E}$ are generated from the outputs and passed to the next stage, being propagate in a self-timed fashion. The solution is low power (as being differential) and eliminates the clock at the expense of a double-rail signaling and the additional "enable generate" block. It is too early to say if the power reduction due to the elimination of the clock and its distribution is off balanced by the "enable generate" block required by each gate. Obviously,

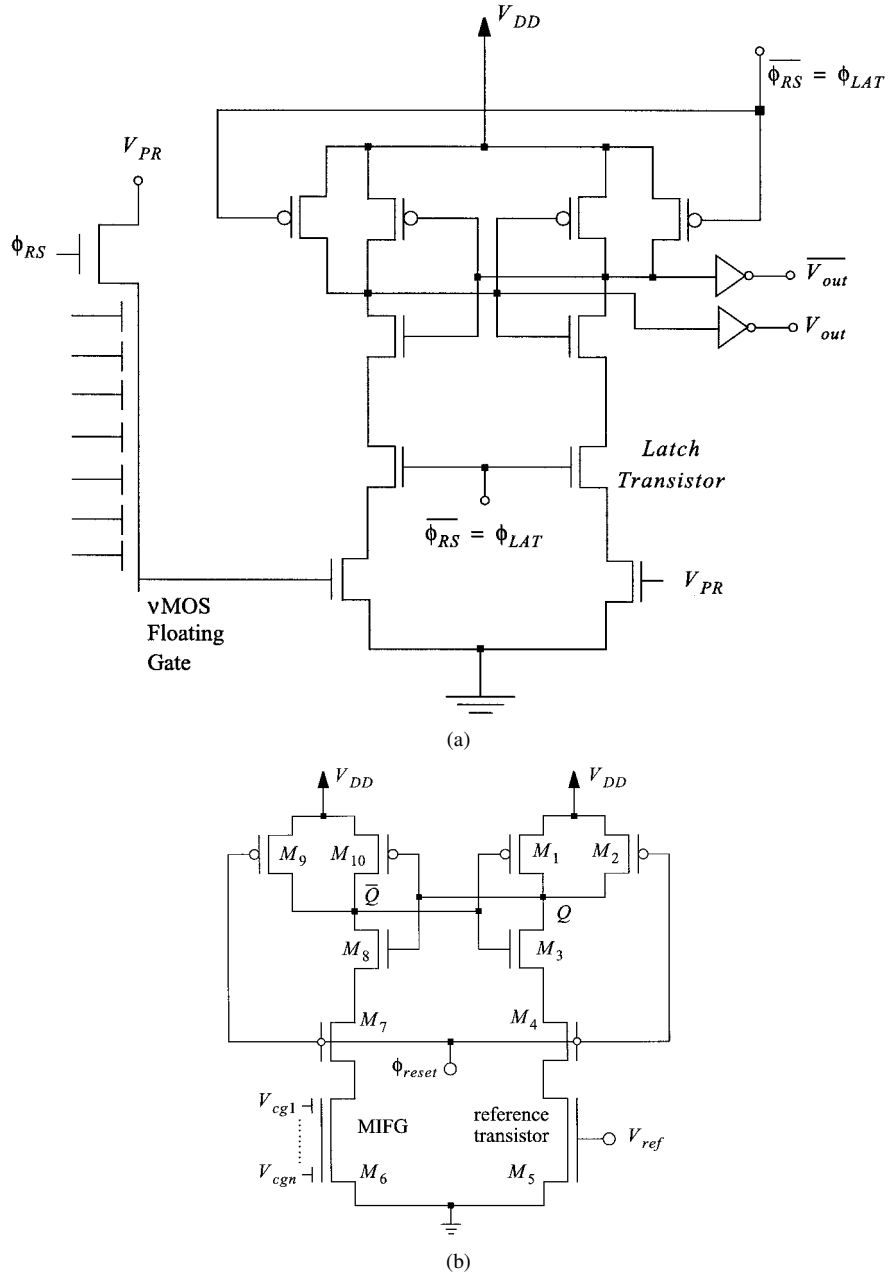

Fig. 13. (a) Dynamic latched-sense-amplifier (comparator) neuron MOS from [76] and (b) the solution from [79], [80], [87], and [90].

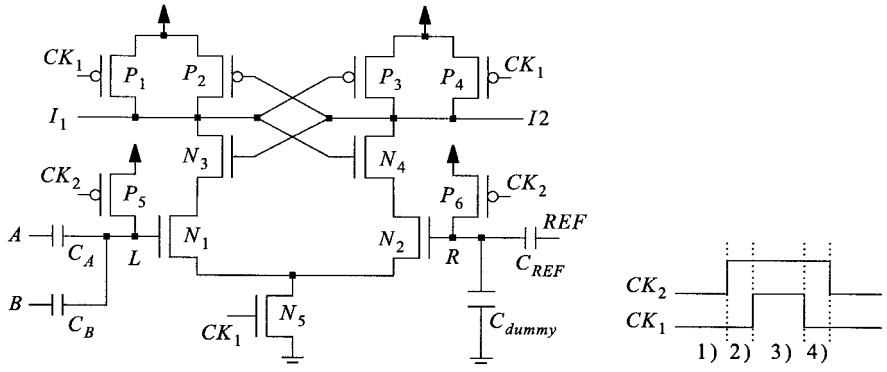

Fig. 14. CMOS capacitor coupling logic ($\mathbf{C^3L}$) from [72].

low-power solutions have to be used in designing this block. The only results reported so far are for a (7, 3) counter, a fundamental building block for binary multipliers (used for reducing the partial products). In a 0.25 μm double poly

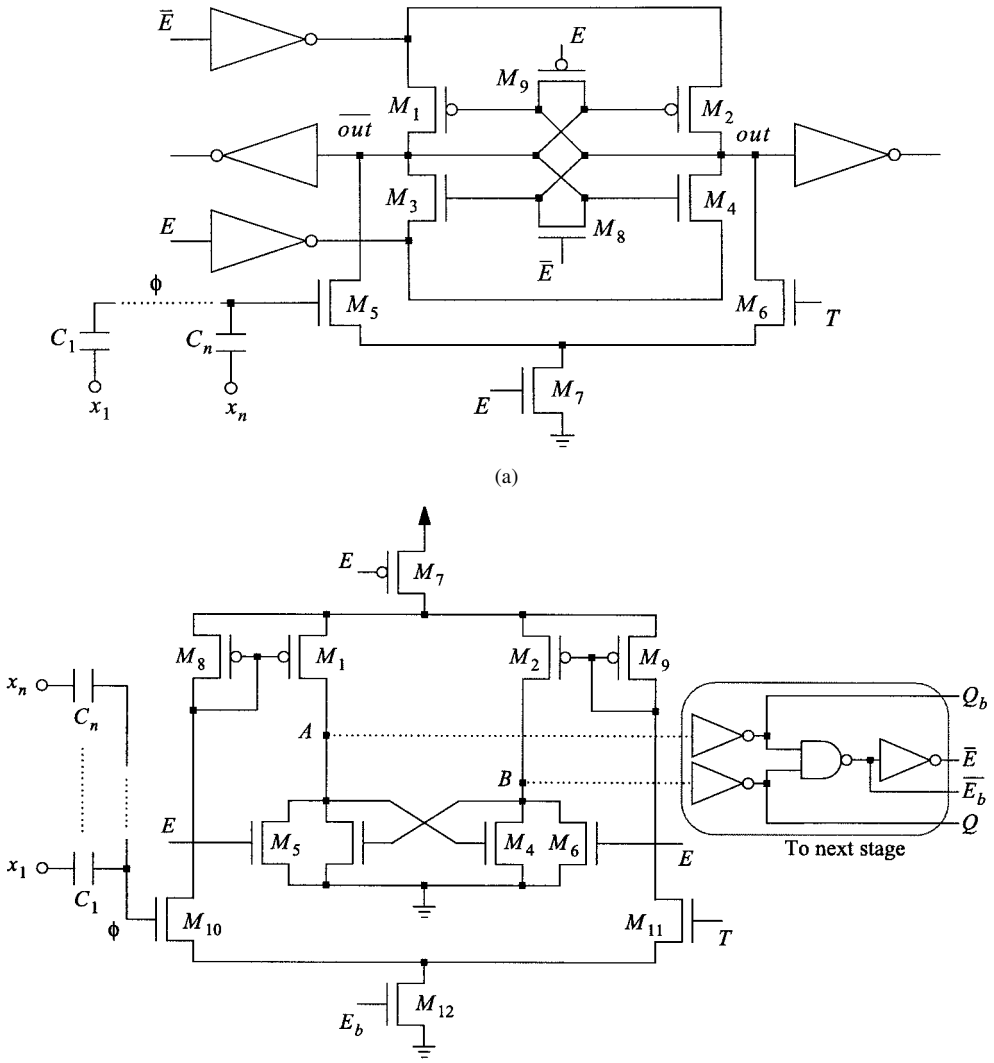

Fig. 15. (a) CRTL from [69]. (b) STTL, another asynchronous sense amplifier differential logic with self-timed enable signaling, from [70].

CMOS, the (7, 3) counter has a delay of 1.4 ns and dissipates 870 μW @ 2 V when driven by a 300-MHz enable signal.

IV. Conductance/Current Implementations

A. Early Conductance/Current Solutions

The first conductance/current-based implementation of TLGs was made in the mid-1940s using resistive circuits [42]. Later, bipolar realizations [16], [29], [94] were proposed and MOS solutions followed [10], [16], [29] (see Fig. 3). A conductance solution (MOSFET synapse followed by an amplifier-comparator) having the weights stored on capacitors was introduced in [104] and a differential version was described in [101].

In this section, we will start with two early TL solutions in CMOS,[1] which time has proven to be enduring: the pseudo-nMOS (also know as grounded-pMOS) and the output-wired inverters (also known as ganged CMOS). Although apparently quite similar, the standard pseudo-nMOS solution uses only one pMOS transistor as a constant load, while the output-wired inverters use several pMOS transistors that form a dynamic load. This leads to two major differences.

- The load is data controlled in the case of the output-wired inverters.
- Having several (identical) pMOS transistors, instead of only one large pMOS transistor, allows for better matching (with a carefully done layout).

The nMOS technology was suitable for high fan-in gates. A depletion nMOS transistor was used as a load (pull-up), making NOR gates very fast (the pull-down network has only parallel transistors). In CMOS, the solution was to use a pMOS with its gate grounded. This is the pseudo-nMOS (also known as grounded pMOS) solution: fast, having dc power, and using ratio rules. The reduced output voltage swing and gain makes the gate more susceptible to noise. That is why, instead of just grounding the pMOS load, its current should track the nMOS device (making the gate less sensitive to process variations), e.g., by using a current mirror. This also accelerates the rise time. In time-critical signal paths, pseudo-nMOS logic can lead to substantial speed improvements if wisely combined with static CMOS (at the cost of only slightly increasing the power

[1]These are not pure CMOS solutions like those detailed in Section II.

consumption). Furthermore, because the gate of the pull-up pMOS transistor can be turned off, pseudo-nMOS supports a power-down mechanism at no extra cost. Large fan-in gates with very fast switching times and reduced static power can be built. One last advantage of such gates is their low transistor count. The ratio rules make it possible to implement TLFs. In the particular case of pseudo-nMOS TLG, the noise margins are reduced as the common output node has meaningful analog voltages. That is why these gates are limited to small fan-in values and an inverter is used both for buffering and for recovering the voltage.

The second solution is based on a plurality of inverters with their outputs hard wired together. The first TLG implementation, based on output-wired inverters followed by a recovering buffer inverter [see Fig. 16(a)], was detailed in 1973 by Lerch: "A threshold gate comprising a plurality of complementary-symmetry, field-effect transistor inverters, each inverter receiving at its common gate connection a different input signal and each connected at its output terminal to a common circuit output terminal [i.e., another inverter]. The gate may have inputs all of the same weight or, with appropriately chosen values of transistor conduction channel impedance or parallel connected inverters, may have inputs of different weight"[98]. It produces a nonlinear voltage divider that drives a restoring inverter (or a chain of inverters) whose purpose is to quantize the nonbinary (analog) signal at the common node v_g. Fig. 16(b) shows the circuit structure for these output-wired-inverters TLGs. Each input x_i drives a ratioed CMOS inverter with only one transistor conducting at a time (because the input is either logic "1" or "0"). Both the pMOS and the nMOS transistors are operated as resistors (conductance). That is why the voltage on v_g depends on how many pMOS and nMOS transistors are conducting, being proportional to $\sum_{i=1}^{n} w_i x_i$. The output inverter is designed to switch when this sum is greater than θ and as an output buffer for recovering the signal. It also provides additional driving capability. The design process for these threshold gates involves sizing only two different inverters [97]. Assuming the same length for all the transistors, the widths $[W_p, W_n]_{i,b}$ for each inverter are chosen taking into account the permissible sums of the weights $\sum_{i=1}^{n} w_i$ and the θ to be implemented. Only positive and integer weight and threshold values are allowed when using this technique. Still, this is not a limiting factor because any TLG can be implemented using only positive integer weight and threshold values [34]. Moreover, nonunit weight values $w_i = k > 1$ can be realized by simply connecting in parallel k basic inverters (one inverter corresponding to $w_i = 1$). The threshold value θ is determined by the output inverter's threshold voltage $V_{\rm th}$. The v_g node is effectively isolated from external circuitry, thereby tolerating some (local) noise. Unfortunately, due to the sensitivity of the voltage on v_g, and of the $V_{\rm th}$ of the output inverter to process variations, the output-wired-inverter TLGs are fan-in limited. A good study of this limitation can be found in [91], while upper and lower bounds on the channel width ratio were obtained analytically in [96]. All of these prove that process variations and operating conditions are limiting the fan-in. A different approach for the determination of the W/L ratios of the transistors uses an evolutionary algorithm

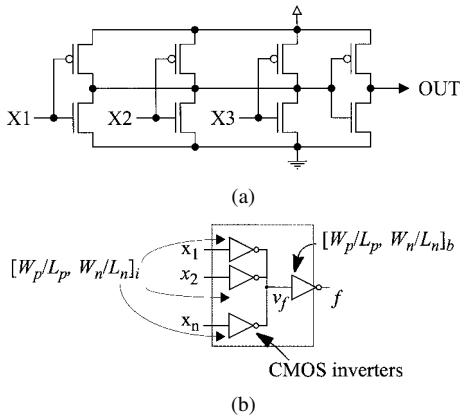

Fig. 16. Output wired inverters discovered by Lerch [98].

[93]. Still, these TLGs are extremely fast, while exhibiting high power consumption (assumable when traded-off for speed), as well as narrow noise margins. After their discovery in 1973 [98], two very similar solutions were shortly proposed [92], [105]. Afterward, output-wired-inverters TLGs have been rediscovered several times. In [19], a very fast CMOS NOR gate is presented, which is Lerch's construction [98] without the final restoring inverter. This was used in the MIPS R2010 coprocessor. Later, Schultz *et al.* [103] rediscovered Lerch's original construction [98] and called it "Ganged-CMOS logic" (GCMOS), the name under which it became well known. The design was extended to multiple-valued logic [102]. The output-wire-inverters technique has been employed to build TLCs for nonlinear filtering [95]–[97], Muller C-elements [100], Losqs voters with multithreshold TLGs [100], or TLCs for D flip-flops [99].

Both pseudo-nMOS and output-wired-inverters solutions are very fast. By the time they were introduced, the dc power consumption was not such a stringent concern/limitation as it is today. Even more, the higher supply voltage made their reduced noise margins acceptable for small fan-ins. As an example of that era, output-wired inverters implementing NOR functions with two and three inputs have been used in the MIPS R2010, the FPU of MIPS R2000 [19].

These two solutions have represented the starting points of two long series of variations/modifications, which made incremental enhancements on their two major drawbacks: the dc power consumption and their reduced noise margins. An almost exhaustive enumeration follows in the next two sections.

B. Beyond Pseudo-nMOS

The dc power consumption was the major drawback of pseudo-nMOS gates when implementing BCs, while noise margins were a concern only when such gates were used to implement TL. As many applications have focused on very fast Boolean gates, pseudo-nMOS was an attractive alternative; especially for a large fan-in, they are much faster than equivalent CMOS gates, which are slowed down by long series of transistors. That is why a good seal of effort has been devoted to reducing the power consumption of large fan-in (wide) pseudo-nMOS gates (e.g., implementing NOR functions). Although TLGs are not always mentioned explicitly, the

results reported are immediately applicable to TLGs. The other drawback, the reduced noise margins, was left as an unsolved open question for TL research.

The main idea for reducing the dc power was to replace the pMOS load transistor (which is always "on") with a more or less complex load circuit. Such solutions rely on using asynchronous feedback and/or feedforward, reducing the voltage swings (unfortunately, this reduces the noise margins even more), using a clock signal (dynamic solutions), or using controlled current mirrors or even data-dependent solutions. As we will see, combinations of several such techniques have also been proposed.

The original pseudo-nMOS has dc current in $2^n - 1$ of the 2^n possible states (where n is the fan-in of the gate), being a data-dependent dc power consumption. For uniformly distributed random inputs, an approximation is given by the ratio $(2^n - 1)/2^n$. Even for relatively small fan-in values, this ratio is close to 1 and will be considered as "100% dc power." The data-dependent dc power consumption of the different solutions will be estimated as a percent of this "100% dc power" or the exact percent will be given when known.

One of the first solutions for reducing the dc power is due to Takemoto [118] [see Fig. 17(a)]. It is a pseudo-nMOS design with feedback: an inverter receives the output of the gate and drives part of the pMOS load. On average, the power is reduced to 50% (supposing that the output is also a uniformly distributed random variable). This solution is now considered as granted and included in many textbooks. A similar solution was presented later by Raza and Nazarian [113], the main differences being that the feedback loop has two inverters (instead of one) and that an additional reference voltage was used to control a second parallel load transistor. A solution for a MAJORITY gate using a current load was presented in [115]. A nonthreshold logic (NTL) was derived from its bipolar counterpart [122], and by that time its speed was comparable to I^2L and ECL. The power-delay product was nearly the same as that of conventional CMOS operated at high frequencies. Reduced voltage swings decrease the power consumption, but also degrade the noise margins.

An enhancement over [118] is detailed in [121] [Fig. 17(b)]. It is "a high-speed low power dissipation, all parallel FET logic circuit." The basic improvement is that the inverter is used both for controlling the active pull-up (load) transistor, as well as recovering the voltage and buffering the output. The output is recovered by an inverter and latched through the pMOS load. The voltage transfer function of the inverter is deliberately skewed for improving the speed. On average, the power is reduced to 50% (similar to the previous solutions). A multigate serial load transistor may further reduce power consumption, unfortunately also slowing down the gate.

A precharged dynamic (clocked) load design, with both feedback and feedforward for increased speed, was presented in [108] (Fig. 18). It has a screening transistor (M_{20}) and clocking circuitry (M_{17}, M_{18}, M_{19}). The clocking circuitry alternately precharges nodes 30 and 34 to V_{DD} and evaluates the voltage on them to output a logic level. Two latching transistors, $(M_{21}$and$M_{22})$, improve the behavior with respect to process variations and circuit instabilities. Inverters, isolating node 30, buffer the outputs. On average, the power is reduced to about 25%.

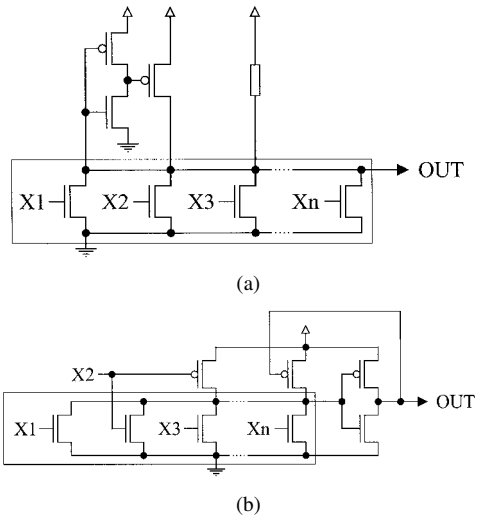

Fig. 17. (a) Dynamic load for lowering the power from [118]. (b) Variation from [121].

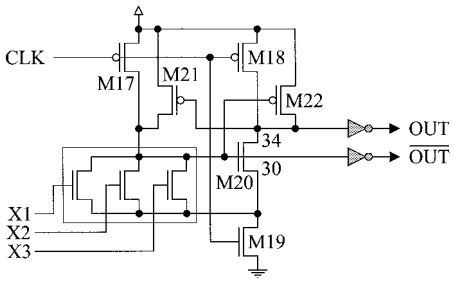

Fig. 18. Clocked (dynamic) solution from [108].

Another method for reducing the dc current uses both feedback and feedforward [112] [Fig. 19(a)]. This design is self-timed (asynchronous), i.e., it does not use a clock. This circuit has both a strong (310) and a weak (309) pull-up pMOS. The weak pull-up device (309) is always "on" and holds the node high if the pull-down device is in an "off" state. However, if the pull-down device is in an "on" state, the strong pull-up device (310) is also turned "on," thereby providing a stable intermediate voltage on the node. A feedback path from the output (317, 316, 314, and 315) controls the state of the strong pull-up device (310). The feedback path can be made sensitive to both the temperature of the circuit and the supply voltage through a control input CTRL (320). The power reduction is difficult to estimate as depending on the sizing of the transistors, but should be better than 50% (probably as low as 25% with a carefully designed layout).

A similar solution, using both a weak and a strong pull-up, is the asynchronous high-speed large fan-in NOR gate, inspired by pseudo-NMOS and dynamic designs, and introduced in [123] [Fig. 19(b)]. The basic idea is to use feedback from the output to control the load and to cut the dc current (Q9B). A regulator (V_{ref}) is coupled to the strong pull-up transistor (Q7B) for regulating the drive current in response to temperature and power supply voltage variations (for maintaining the speed). Four different versions allow for: 1) high speed; 2) reduced voltage swings on the inputs; 3) temperature and voltage compensation;

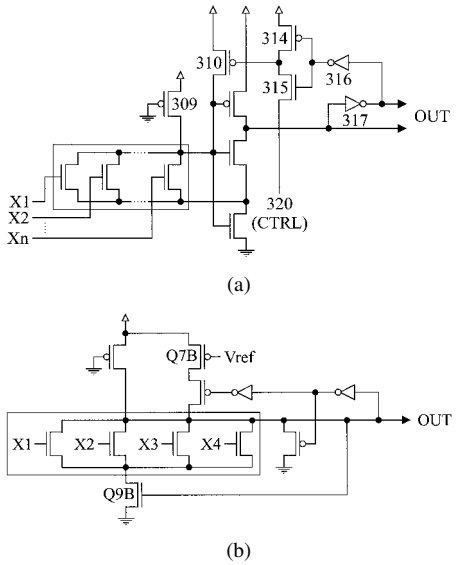

Fig. 19. Self-timed feedback solutions: (a) for low power consumption from [112] and (b) limiting the voltage from [123].

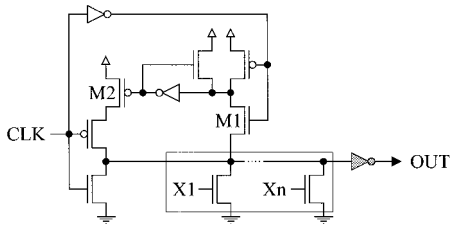

Fig. 20. Predischarged ratio logic from [110] and [111].

and 4) limited low voltage on the output (using a feedback technique). Power reduction is difficult to estimate, but should be better than 50%. The regulator providing the reference voltage $V_{\rm ref}$ complicates the design.

A method for significantly reducing the dc power consumption of clocked pseudo-nMOS (ratioed) gates is presented in [110], [111] (Fig. 20). A sensing circuit (M_1) analyzes the voltage transitions of the ratioed node and controls the dc current flow (M_2) through the entire circuit. Simulations have shown that dc power is reduced to 14%, making it one of the best solutions with respect to dc power reduction (for pseudo-nMOS/ratioed circuits).

A simple improved pseudo-nMOS design for minimizing power is described in [109] [see Fig. 21(a)]. The solution uses a clock to control a current mirror. Voltage floating of the output is also eliminated and, on average, power is reduced to 50%. Another more complex version of the gate [Fig. 21(b)] uses both a clock signal (CLK) and a power-up signal (POWER UP). The power-up signal is a delayed version of the clock signal and, together with the feedback from the output, further diminishes the power consumption. This second solution is complex and requires a demanding timing scheme, but could be rewarded by a dc power reduction even lower than 14% (obtained in [110] and [111]).

By far ,the simplest solution for reducing the power consumption to 50% (on average) is presented in [119] and [120] [see Fig. 22(a)]. This is a data-dependent pseudo-nMOS gate, where the pull-up transistor is controlled by one of the input variables. The idea has been also used in [117] [see Fig. 22(b)] for an m-of-n TLG [116].

A hybrid solution was presented in [106] and [107] (see Fig. 23). It corresponds to the category of conductance with one pMOS transistor driven by a reference voltage $(V_{\rm ref})$ and all the nMOS transistors driven by the inputs through floating gates (i.e., instead of setting the weights by the width to length ratio of the transistors, the weights are encoded as charges on the floating gates). These charges modify the transistor threshold voltage and, therefore, its current. Hence, weights are programmable and can be quadratic or exponential in the voltage stored on the floating gate, resulting in a large dynamic range. A 16-input programmable gate is reported. Programming is achieved through tunneling and injection of hot electrons. The solution is sensitive to noise, relatively slow, and has data-dependent static power dissipation, but allows for large fan-ins.

Very recently, two other variations of the pseudo-nMOS style of design have been presented. One is called pseudodynamic and "was highly leveraged across the Itanium 2 processor" [35], [36]. It is mentioned that such gates "garner most of the benefit of dynamic logic while maintaining the ease of use [...] associated with static gates; [...] these gates are higher power than traditional static design; [...] the low input capacitance, small area required by the NFET-only evaluate structure and high fan-in that these device achieve more than makes up for their cost; [...] this design yields a 15%–20% delay improvement over traditional pseudo-nMOS; [...] these [...] circuits, essential to the Itanium 2 processor's success, have been shown to be robust through post-silicon analysis" [36]. The schematic of a pseudodynamic gate can be seen in Fig. 24. Finally, the idea of using ratioed static gates (i.e., pseudo-nMOS inspired) for achieving very high speeds even with high fan-in has also been advocated by Schuster and Cook [114]. The circuit implemented is an advanced Muller C-element, with roughly 3 ps of delay for each additional input (when implemented in 0.18 μm bulk CMOS). Concerning reliability, the authors state that "The circuit has been designed for worst case device variations in the strength of the n-channel clamp and the p-channel pullup so that switching will not occur until all the inputs have gone low. [...] it takes roughly three times the maximum parameter variation of 20% for failure to occur" [114].

C. Beyond Output-Wired Inverters

Output-wired inverters suffer from the same disadvantages as pseudo-nMOS solutions: dc power consumption and reduced noise margins. That is why solutions for trying to overcome either one or the other of these disadvantages have been on the research agenda for quite some time.

A first enhancement can be seen in Fig. 25. It showed how to connect the inputs only to the nMOS transistors [135]. This makes the solution look similar to a pseudo-nMOS one, but the matching is still better. The solution reduces input capacitance by having the input signals connected only to the nMOS stack. The threshold of the function to be implemented is set by prewiring all the pMOS transistors to either $V_{\rm DD}$ or GND. The

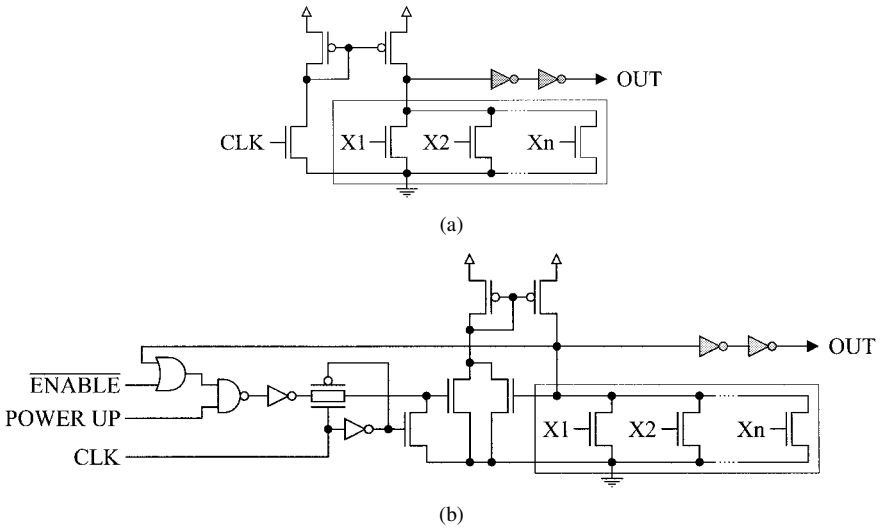

Fig. 21. Two clocked (dynamic) solutions from [109].

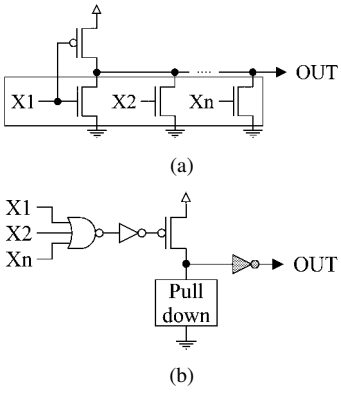

Fig. 22. (a) Modified data dependent pseudo-NMOS gates from [119] and [120] and (b) data dependent m-of-n threshold gate from [117].

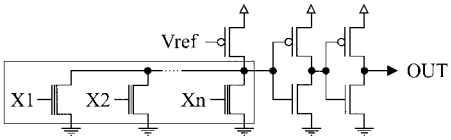

Fig. 23. Solution using floating gates for the inputs from [106] and [107].

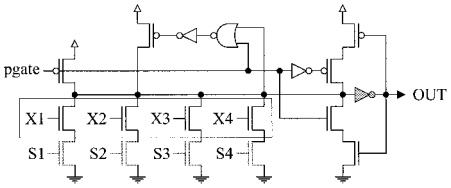

Fig. 24. Solution used in the Itanium 2 [35], [36].

solution slightly increases the speed (due to the reduced capacitance), but does not improve the power consumption or noise margins.

A modification to the basic idea was introduced in [142] and [143], where a new class of logic gates called source follower pull-up logic (SFPL) is described. The pull-up and pull-down structures are separated and connected through an inverter. A high fan-in gate implemented following this technique is shown in Fig. 26(a). The power dissipation is still large. It is mentioned

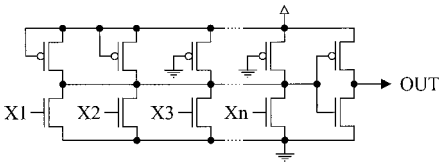

Fig. 25. CMOS solution from [135].

that SFPL has acceptable noise margins. An enhancement over SFPL is detailed in [140] [see Fig. 26(b)] and is used in custom comparators to speed up critical stages in a superscalar processor: SUN Sparc V9 [25]. Other comparators specifically designed for low power are described in [139] and are compared against SFPL.

The original output-wire inverters have two transistors per input. Using only one transistor per input was shown for particular BFs in [133]–[134] and [136]–[138]. The formal proof and a systematic method on how to design TLGs having one transistor per input (either nMOS or pMOS), led to the β-driven threshold element ($\boldsymbol{\beta}$-DTE) [144], [150], [151]. The computing block is a classical voltage divider formed by pMOS and nMOS transistors (called the β-comparator) and can be seen in Fig. 27(a). The feasibility of such an implementation follows from the fact that any TLF can be represented in a ratio form

$$y = \operatorname{sgn}\left(\sum_{i=1}^{n} w_i x_i - \theta\right) = \operatorname{sgn}\left(\sum_{j\notin S} w_j x_j - \sum_{j\in S} w_j \overline{x_j}\right)$$
$$= \operatorname{sgn}\left(\frac{\sum_{j\notin S} w_j x_j}{\sum_{j\in S} w_j \overline{x_j}} - 1\right) \quad (2)$$

where S is a certain subset of indexes such that $\sum_{j\in S} w_j = \theta$.

The voltage on node v_β is determined by the ratio of sums of βs of pMOS and nMOS transistors. Its implementability depends only on the threshold value θ and not on the number of inputs and their weights. The βDTE solution reduces the input capacitance and the internal node capacitance, making the gate very fast, but does not tackle any of the two main disadvantages: the high power consumption and the narrow

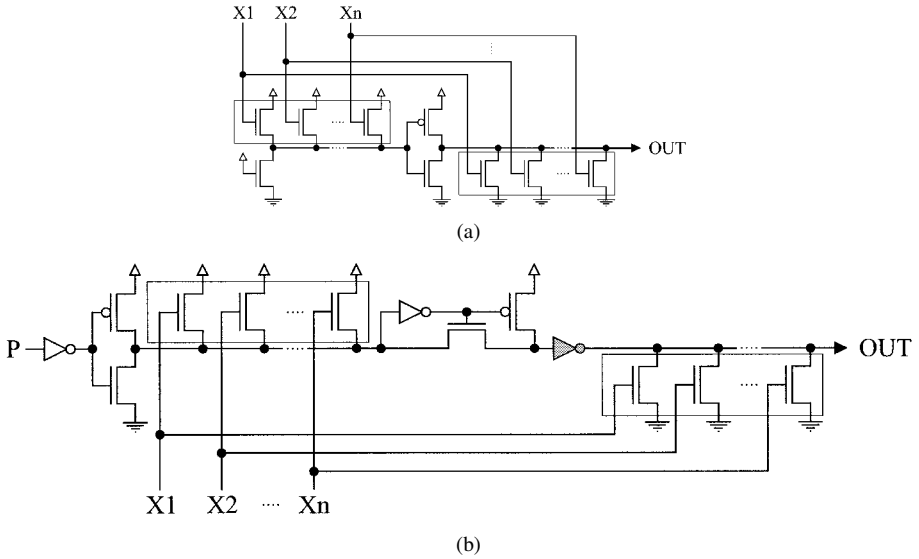

Fig. 26. (a) SFPL from [142] and [143]. (b) Enhanced version from [140] and [25].

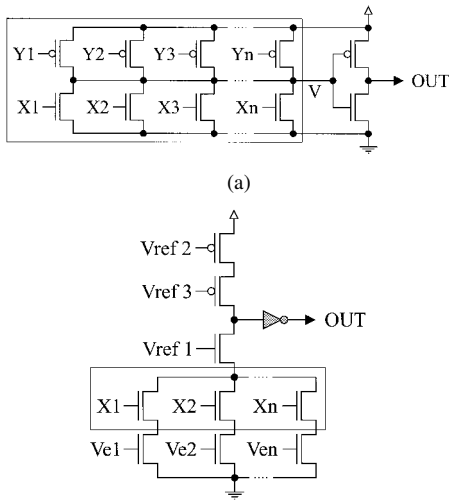

Fig. 27. (a) Beta-driven threshold element (βDTE) from [144], [150], and [151]. (b) Modified beta-driven threshold element (βDTE) from [147] and [148].

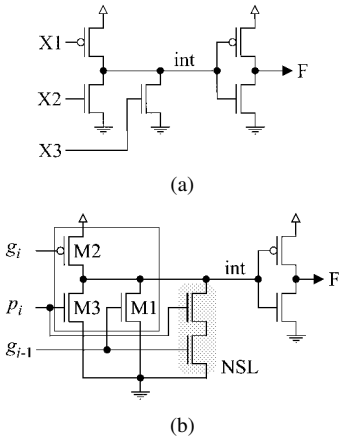

Fig. 28. Implementation (a) without the data dependent noise suppression logic (NSL) and (b) with NSL [124]–[126], [129].

noise margins. An improved β comparator having higher nonlinearity in the threshold zone (hence, improving on the noise margin) is presented in [147], [148] [Fig. 27(b)]. This is achieved using three additional highly stable reference voltages: $\mathrm{V_{ref1}}, \mathrm{V_{ref2}}, \mathrm{V_{ref3}}$ (a quite demanding condition). SPICE simulations for 0.8 μm CMOS have proven that the fan-in is limited to about 10. Artificial learnable neurons based on βDTEs have been reported in [145], [146], [148], and [149].

Another method for enhancing the noise margins of TLGs is presented in [124], [125], and [129]. The method is data dependent, which is simpler than the ones detailed in [147] and [148]. It adds data-dependent nonlinear terms to the βDTEs, practically converting the TLG into a "high-order perceptron" [126]. The nonlinear terms form a noise-suppression logic (NSL), which can always be determined from the Boolean form of the TLF by subtracting the minterms implemented by the pMOS stack: $f_{\mathrm{NSL}} = f \setminus (\prod_{j \in S} x_j)$. Fig. 28(a) shows the implementation of $F = x_1 \vee (x_2 \wedge x_3)$, which can be expressed as $F = \mathrm{sgn}(2x_1 + x_2 + x_3 - 1.5)$. Fig. 28(b) shows the implementation of the same function with the additional NSL. By properly sizing the transistors. the noise immunity can be improved (i.e., better noise margins are traded off for larger area) and the speed can be increased (at the expense of higher dc power consumption). NSL has been tested for gates with fan$-in \leq 7$. The TLG implementing F with NSL in 0.5 μm CMOS has a delay of less than 80 ps at $V_{\mathrm{DD}} = 3.3$ V (when driving four identical gates). A five-layer 32-bit adder using F and three other BFs —$f_6 = g_i \vee (p_i \wedge g_{i-1}) \vee (p_i \wedge p_{i-1} \wedge g_{i-2}), h_4 = (a_i \wedge b_i) \vee [(a_i \vee b_i) \wedge (a_{i-1} \wedge b_{i-1})]$, and $g_{i:i+3} = g_{i+2:i+3} \vee (p_{i+3} \wedge p_{i+2} \wedge g_{i:i+1})$ (see [127] and [129]–[132]) —has been implemented using TLGs with NSL in 0.18 μm CMOS. It achieves a delay of less than 300 ps dissipating 142 mW @ 2.5 GHz (running continuously).

For reducing the dc power, a data-dependent self-timed power-down (STPD) mechanism has been recently developed [124], [126]–[128]. It uses either one or two additional transistors isolating the gate from V_{DD} and/or GND [Fig. 29(a)]. Each of these transistors is driven by a control logic having as inputs

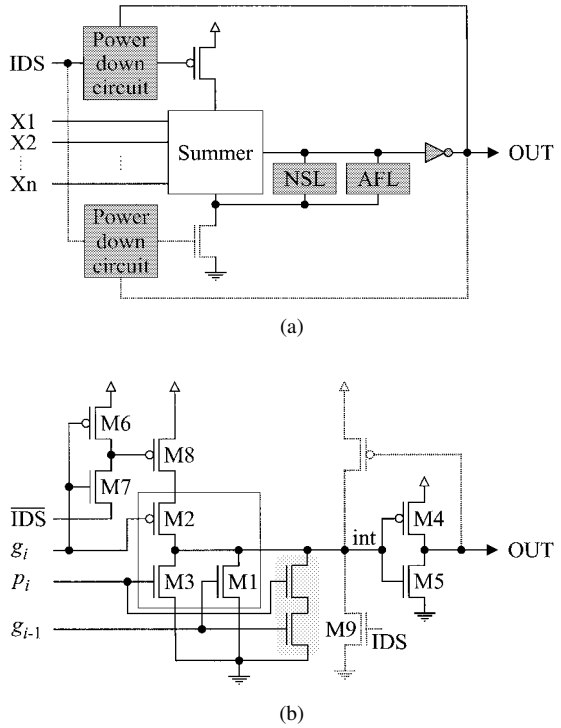

Fig. 29. Data-dependent STPD mechanism from [124], [126], and [128]. (a) Block diagram and (b) particular solution.

the incoming data, the output of the gate, and an asynchronous external signal IDS. One of the solutions reduces the dc power to about 50% [Fig. 29(b)], while another solution reduces the dc power to about 25% (see [127] and [128]). For the 32-bit adder mentioned above, the power can be reduced from 142 to 46 mW @ 2.5 GHz.

Finally, a method to significantly increasing the fan-in of a MAJORITY gate has been recently proposed [141]. With a safety margin of 3% $V_{\rm DD}$, the patent claims that gates with up to 1000 inputs can be realized ($V_{\rm DD} = 5$ V). The solution combines CMOS inverters with analog circuitry that automatically adjusts to the variances of the MOS characteristics. A bias circuit generates a voltage similar to the threshold voltage of the inverter, cancelling the offset of the potential on the internal (analog) node that arises due to the disagreement of the conductance of the nMOS and pMOS transistors. Such a MAJORITY gate is significantly less sensitive to process variations, but still leaves open the power-dissipation problem.

D. Differential Solutions

Many of the differential TLG implementations in the current/conductance category have in common two parallel connected sets of nMOS transistors implementing the weighting operation, as well as a CMOS comparator for the threshold operation. The main advantage over the solutions presented previously (Sections IV-B and C) is their low power consumption (as having only dynamic power).

The first differential solution based on resistor-diode structures and bipolar transistors and comparing $\Sigma w_i x_i$ with θ was introduced in 1964 [162]. A very interesting differential solution was presented in 1967 [158]. The solution can be used for comparing either $\Sigma w_i x_i$ with θ or with direct and inverted inputs (i.e., having f and $\bar{f}$ as the differential inputs). An input signal and its complement are inserted in a direct-coupled transistor flip-flop pair through a differential transistor amplifier. This solution does not require closely matched components and is substantially insensitive to noise. Two other novelties brought in were the fact that the inputs are isolated from outputs (reducing input–output capacitance) and that a clock source replaces the standard GND (reducing the dissipated power), making this the first adiabatic TLG solution.

The operation of cross-coupled inverters with asymmetrical loads (CIAL) was exploited to implement digital (bus) comparators [161], a particular example of a TLG (see Fig. 30). At the same time, a generic latch-type TL (LCTL) gate was proposed in [152] (Fig. 31), which consists of a CMOS current-controlled latch (transistors $\rm M_2/M_5$ and $\rm M_7/M_{10}$), which provides both the output and its complement, as well as two input arrays $(M_{4_1} - M_{4_n})$ and $(M_{9_1} - M_{9_n})$, which have an equal number of parallel transistors whose gates are the inputs of the TLG. Transistor pairs $\rm M_1/M_3$ and $\rm M_6/M_8$ specify the precharge or evaluate phase and two extra transistors $M_{4_{n+1}}/M_{9_{n+1}}$ ensure correct operation for the case when the weighted sum of inputs is equal to the threshold value. Precharging occurs when the reset signal $\Phi_{\rm R}$ is at logic 0. $\rm M_1$ and $\rm M_6$ are "on," while $\rm M_3$ and $\rm M_8$ are "off," and both OUT and $\overline{\rm OUT}$ are at logic 1. Evaluation begins when $\Phi_{\rm R}$ is at logic 1. $\rm M_1$ and $\rm M_6$ are turned "off," while $\rm M_3$ and $\rm M_8$ are turned "on," and nodes OUT and $\overline{\rm OUT}$ begin to be discharged. In this situation, depending on the logic values on the inputs of the two transistor arrays, one of the paths will sink more current than the other. This accelerates the falling of its corresponding output voltage (either OUT or $\overline{\rm OUT}$). When the output node of the path with the highest current value falls below the threshold voltage of either $\rm M_5$ or $\rm M_{10}$, it turns it off, fixing the latch situation completely. Supply current only flows during transitions and, consequently, this TLG does not consume static power. Input terminal connections and input transistor sizes in this TLG implementation must be established according to the threshold value θ to be implemented. When all transistors M_{4_i} and M_{9_i} $(i = 1, 2, \ldots, n)$ have the same dimensions and the same voltage is applied to their gates, $I_{\rm in} > I_{\rm ref}$ due to $M_{4_{n+1}}$.

The speed performance of LCTL gates has been improved by the solution proposed in [157]. Here, the nMOS banks are external to the latch (see Fig. 32), avoiding the large long feedback chain of LCTL. It is called cross-couple inverters with asymmetrical loads threshold logic (CIALTL). Note that, in spite of using the same name, the circuit topologies in [157] and [161] are different. In this gate, the input transistor arrays $(M_{x_i} - M_{y_i}, i = 1, 2, \ldots, n)$ are connected directly to the latch's output nodes and precharging occurs when Φ_1 and Φ_2 are at logic 0, putting nodes D, OUT, and $\overline{\rm OUT}$ at logic 1. For the evaluation phase, both Φ_1 and Φ_2 are at logic 1, but Φ_2 must return to a low level before Φ_1 in order to allow the latch to switch. CIALTL needs two control signals, which have to be obtained from a general clock. Therefore, a great deal of power is dissipated in the

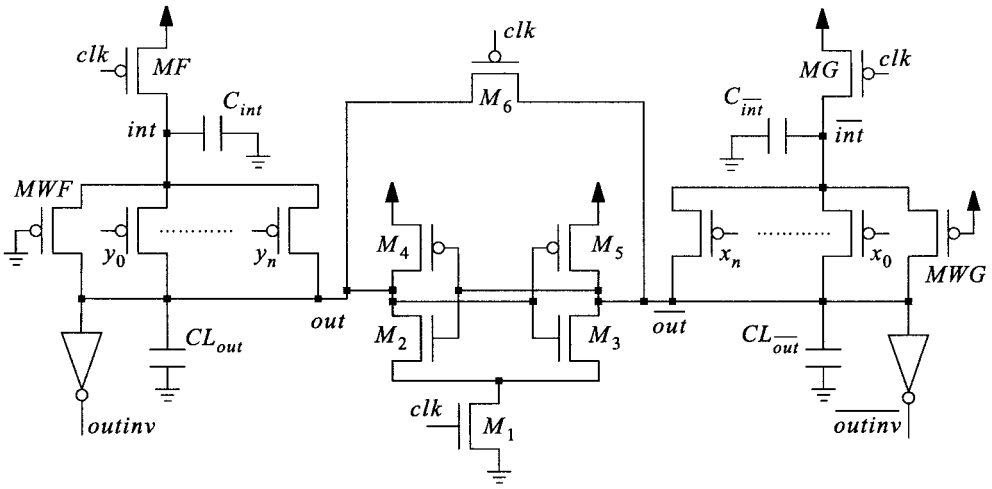

Fig. 30. Digital comparators based on CIAL from [161].

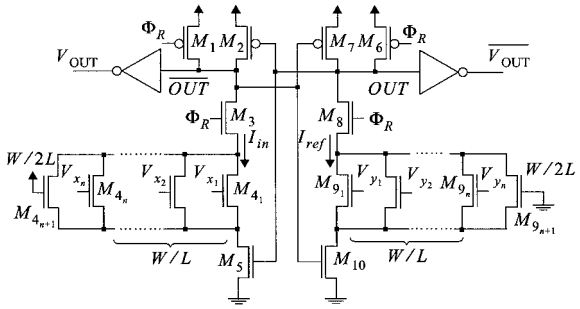

Fig. 31. Latch type LCTL from [152].

internal clock front end. The circuit arrangement for realizing logic elements that can be represented by threshold value equations patented by Prange *et al.* [167] is a simplified version of CIAL (see Fig. 33).

Recently, a number of TLGs have been proposed based on advanced clocked CMOS differential logic structures by implementing the pull-down networks with two banks of parallel nMOS transistors, instead of using nMOS complementary logic trees. Examples are as follows.

- Single-input current-sensing differential logic (SCSDL) [170], [171] after the CSDL [163]. Fig. 34 shows its schematic for a generic pull-down tree and the circuit structure for an n-input MAJORITY gate.
- Differential current-switch threshold logic (DCSTL) [164]–[166] (Fig. 35) after the DCSL [168], [169]. This is a differential cascove voltage swing (DCVS) [159] approach that restricts the voltage swing of the internal nodes for lowering the power consumption. DCSTL requires a single clock. Reported experiments from a 31-input AND show that DCSTL exhibits better power-delay product than the other two latch-based TLG implementations described above: LCTL [152] and CIALTL [157].
- Current-mode threshold logic (CMTL) [154] also uses two banks of parallel transistor for inputs and threshold followed by sensing. Low power is achieve by limiting the voltage swing on interconnects and the internal nodes of the CMTL gates. Various clocked cross-coupled loads have led to discharged CMTL (DCMTL) and equalized CMTL (ECMTL).

These TLGs, based on current comparisons, are still sensitive to noise and mismatch of process parameters, which limit their maximum fan-in. For example, yield analysis for SCSDL implemented in 0.35 μm CMOS have shown that fan-in ≤ 14 [170], [171]. Reliability can be improved by well-known analog layout and circuits techniques, where the devices behavior is matched (substrate voltage control, shield and isolations, layout of transistors with the same orientation, and use the same size for transistors, i.e., use multiple smaller transistors connected together to realize a larger device with reduced statistical parameter variations).

All the solutions detailed above (with the exception of [158]), fall under one of the following two cases: either compare the sum of weights with a threshold [154], [167], [171] (also [69], [70], [72], and [76]), or compare two weighted sums [152], [157], [161] (also [59]). An original solution improving over all of these (even over the solution presented in [158]) is to implement function f with one bank and $\bar{f}$ with the other, while adding an NSL scheme both for f and $\bar{f}$ [153]. It is well known (e.g., see [34]) that inverting a TL function requires only to invert the inputs (and change the threshold). The fact that f and $\bar{f}$ always have transitions in opposite directions leads to increased speed and better noise margins. This method can be used with any of the differential techniques. As an example, this technique has been demonstrated in conjunction with the split-level precharge differential (SLPD) logic [160]. This is the split-precharge differential noise-immune threshold logic (SPD-NTL) gate [172] (Fig. 36). The power consumption is reduced to less than 10%. The gate is currently being test and will be used in the design of a four-layer 32-bit adder, a five-layer 64-bit adder [130], [131], and a 32-bit multiplier [132]. We estimate that the 32-bit adder will have an overall delay of less than 200 ps while dissipating less than 10 mW @ 5 GHz (i.e., when

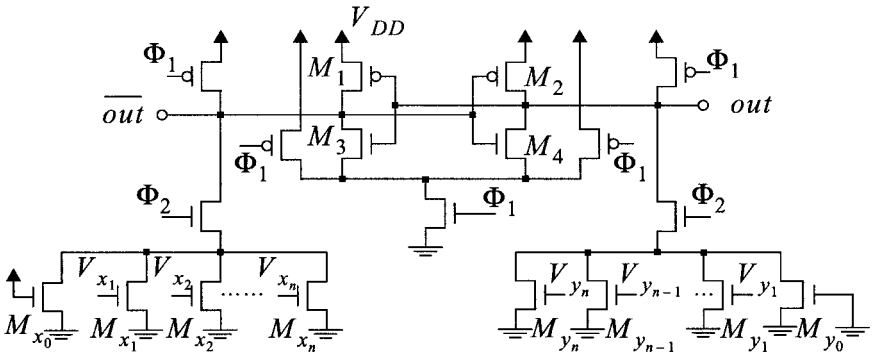

Fig. 32. CIAL-TL from [157].

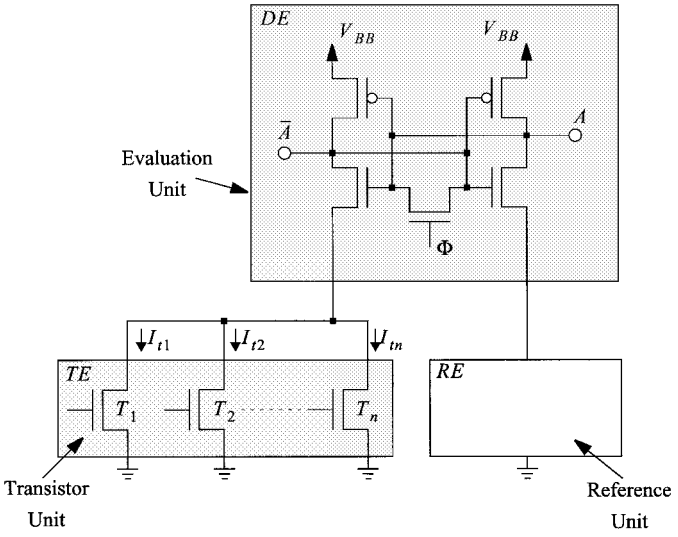

Fig. 33. Differential implementation from [167].

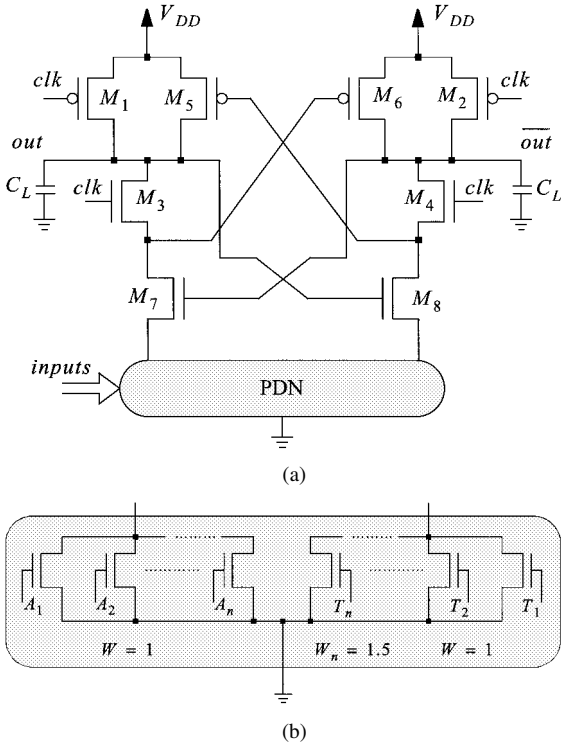

Fig. 34. SCSDL from [170] and [171].

running continuously) in 0.13 μm CMOS. The power reduction comes both from having fewer TLGs and from using the new SPD-NTL gates.[2]

Finally, a conceptually different implementation was proposed in [155] and [156]. The key computational concept is to use a floating-gate device as a programmable-switched conductance (as in [106] and [107]). By storing an analog value as the threshold of a floating gate device and applying a second digital value to the gate of the device, the conductance can be either zero or a preprogrammed analog value. These conductances store the weights associated to each input. Fig. 37 depicts the circuit schematic. Two parallel Flash-EEPROM banks implement the weighted sum of inputs with positive weights and the weighted sum of inputs with negative weights. The rest of the circuit, called the conductance comparator, provides for measuring conductance based on the current through the "memory" cells. The precision to which the threshold of a floating gate can be programmed determines the bit equivalent precision of the weights.

V. Other Implementations

Many other approaches have been used for implementing TLG. As early as 1966, Jones has looked into superconducting implementations [20]. In particular, research on Josephson TLs has been well published [175], [176], [178], [179]. Other researchers have experimented with charge-coupled devices [173]. These can reach very low power, but are very low speed also. A survey can be found in [174]. Even optical [177], [181] and biological [180] TLGs have been investigated.

Currently, the emerging devices are single electron devices, RTDs, double layer tunneling transistors, and Schottky barrier MOSFET.

A. Single Electron Tunneling (SET) Solutions

SET has been receiving increased attention because it combines large integration and ultra-low power dissipation. Operation of a SET device is based on the quantum-mechanical tunneling phenomena. This allows control of the current flowing through SET devices per individual electron, if desired. The fundamental physical principle of SET devices is the Coulomb Blockade [194], which results from the quantization of the elementary charge in an isolated node of a double junction

[2]All the SPD-NTL gates include NSL (i.e., noise suppression logic).

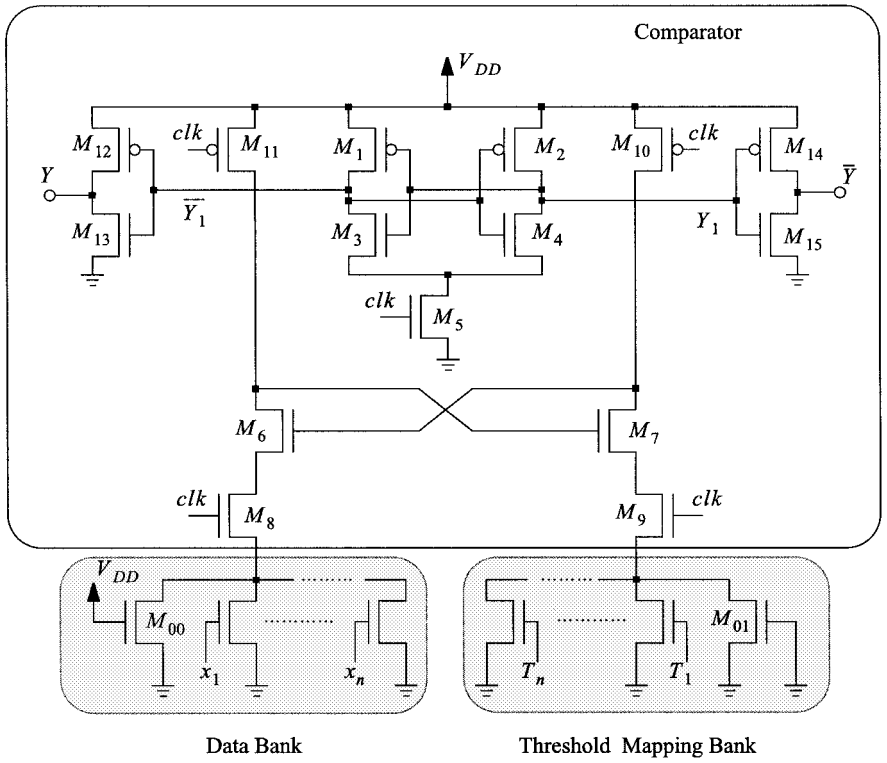

Fig. 35. DCSTL from [164] and [165].

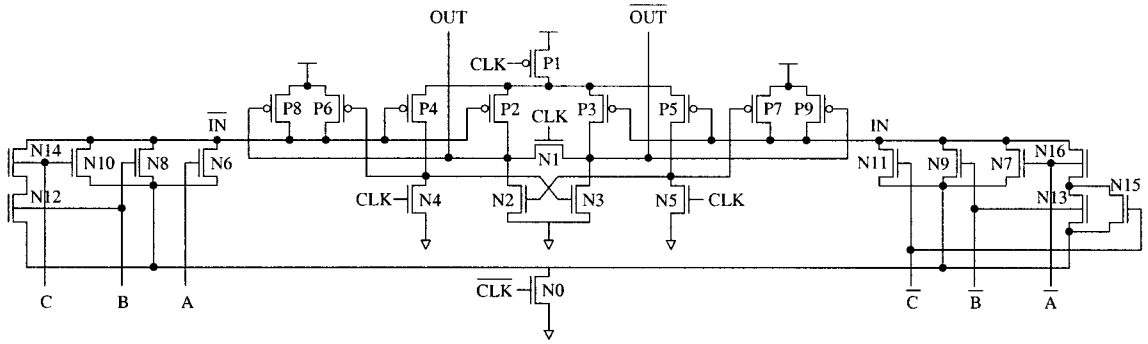

Fig. 36. Split-precharge differential noise-immune threshold logic (SPD-NTL) from [153] and [172].

structure. To observe the blocking of the electron tunneling through the island, the charging energy of the island has to exceed the thermal energy, which at room temperature requires ultra-fine structures. Recently, the use of SET technology to TLCs have been proposed [182], [184]–[186], [192], [193], [196] and several implementations of TLGs have been presented. Many use a capacitor array for input summation, which are similar to the solutions reported in Section III, but differ in the way the thresholding operation is carried out [183].

A SET implementation of MAJORITY gates, similar to the static νMOS TLGs, is presented in [187]. The circuit consists of a capacitor array for input summation and a SET inverter for threshold operation. Fig. 38(a) shows a three-input MAJORITY gate. It consists of an input capacitor array (six capacitors C) for input summation and a Tucker-type [194] inverter (tunnel junctions $C_{j1}, \ldots, C_{j4}$ and capacitors C_1, C_2, and C_3) for threshold operation. The input nodes P and Q of the inverter are coupled to V_1, V_2, and V_3 through the input capacitances (C), such that the potential of each input node is changed proportionally to the mean value of the inputs.

Klunder and Hoekstra [188] have proposed the use of the electron box as a programmable logic circuit (NAND and NOR functions) and, although not explicitly mentioned, arbitrary TLGs. It consists of an electron box [see Fig. 38(b)] in which the nontunneling capacitor has been divided into $n + 1$ capacitors. For this type of circuit, $V_{\rm out} = (V_c C_c + \sum_{k=1}^{n} V_{{\rm in},k} C_{{\rm in},k} + q_i)/C_{\rm tot}$ with $C_{\rm tot} = C_c + C_j + \sum_{k=1}^{n} C_{{\rm in},k}$ and q_i the total charge of the island (equal to ne, with n the number of electrons that have left the island), assuming that the background charge and the initial charge are both zero. The circuit naturally compares $V_{\rm out}$ to $e/(2C_{\rm tot})$, as an electron can tunnel through the junction if $-e/(2C_{\rm tot}) \geq V_{\rm out} \geq e/(2C_{\rm tot})$. The values for V_c and for the capacitors can be selected to implement a given TL

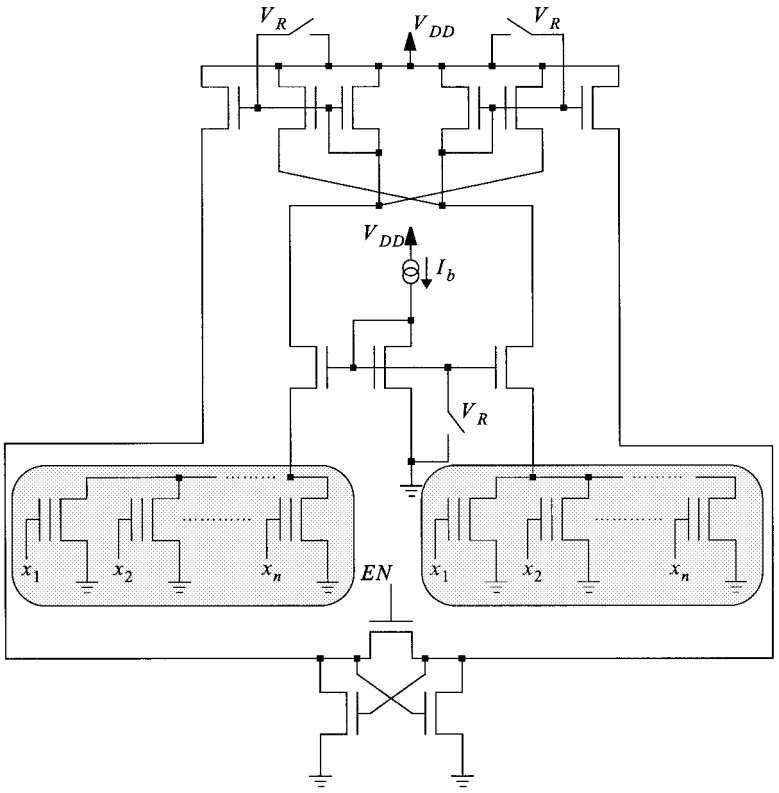

Fig. 37. Conductance sensing using floating gates for the inputs from [155] and [156].

function. Correct operation at $T = 0°$K, logic input swing of 0.2 mV, and logic output swing of 1 mV was validated through simulation with SIMON [195].

Another n-input TLG was proposed in [189]. It requires one tunnel junction and $n+2$ true capacitors [Fig. 38(c)]. The TL function performed by this circuit is the comparison of the voltages V_j across the tunnel junction and the critical voltage needed to enable tunneling. Both positive and negative weights can be implemented with this structure. Correct operation was also validated using SIMON [195], assuming $T = 0°$K and no background charge effects. It exhibits voltage levels of 0 V and 16 mV for the 0- and 1-logics, respectively. A full adder was reported as having a delay of 2 ns. When such TLGs are placed in a network structure, strong feedback effects occur, which could result in erroneous behavior. For solving this problem, an active buffer is used after the TLG [190]. Recently, a MAJORITY gate using a balanced pair of single electron boxes has also been proposed [191].

B. Resonant Tunneling Devices (RTDs)

NRDs have been proposed for implementing TLGs as early as 1961 [44], followed by [198], [206], and [210] and more recently by [208] and [209]. The transistors currently in use are in fact potential barriers. If the width of such a "potential barrier" at the base becomes smaller than the wavelength of the electron (about 10 nm), the electrons will tunnel through (the tunnel effect discovered by Esaki [202], [203]). Such a small transistor will leak and it will not be possible to use it as a switch. Nanoelectronic devices in general, and RTD in particular, are designed to take advantage of exactly this effect. The simplest such device is the resonant tunneling diode, which consists of an emitter and collector region and a double tunnel barrier structure. This contains a narrow quantum well (about 5 nm), which allows electrons to travel through only at the resonant energy level. The characteristic of this device is similar to the Esaki tunnel diode, exhibiting a region of negative resistance, with a peak B and a valley C [Fig. 39(a)].

While RTD is the basic two-terminal negative differential resistance (NDR) device, it is also possible to introduce tunneling (at the base-emitter junction) within

- conventional bipolar devices, such as heterojunction bipolar transistors (HBTs);
- high-performance bipolar GaAs devices, such as hot-electron transistors (HETs);

and (at the gate-source junction)

- field-effect devices, such as modulation-doped field-effect transistors (MODFETs).

In this way, three-terminal NDR devices such as resonant tunneling bipolar transistors (RTBTs) or resonant HETs (RHETs) are obtained. Another approach commonly used is that RTD-based logic gate configurations are implemented by using cointegrated, but separate, RTD and HBT/MODFET devices.

Circuit applications of RTDs are mainly based on the monostable-bistable logic element (MOBILE) [197], [201]. The MOBILE is a rising-edge-triggered current-controlled gate, which consists of two RTDs connected in series and is driven by a switching bias voltage $V_{\rm bias}$, as shown in Fig. 39(b). The RTD is a two-terminal device without input–output capabilities. A specific logic functionality of a MOBILE is determined by

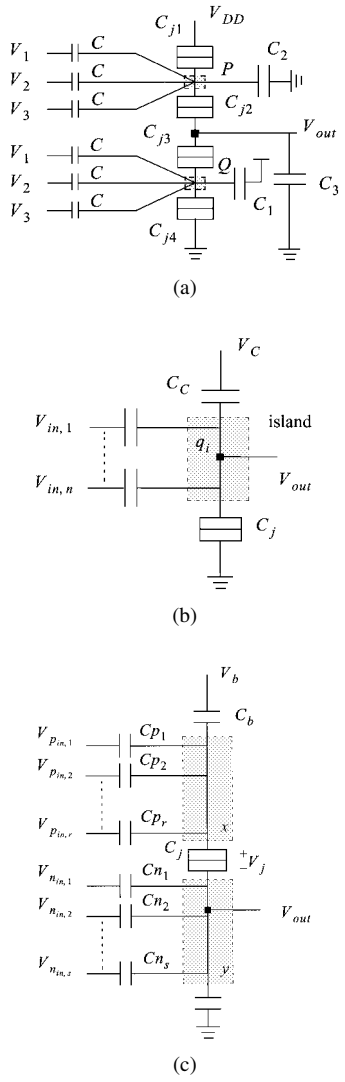

Fig. 38. (a) SET: three-input MAJORITY gate from [187] and (b) programmable gate from [188], and (c) n-input TLG from [189].

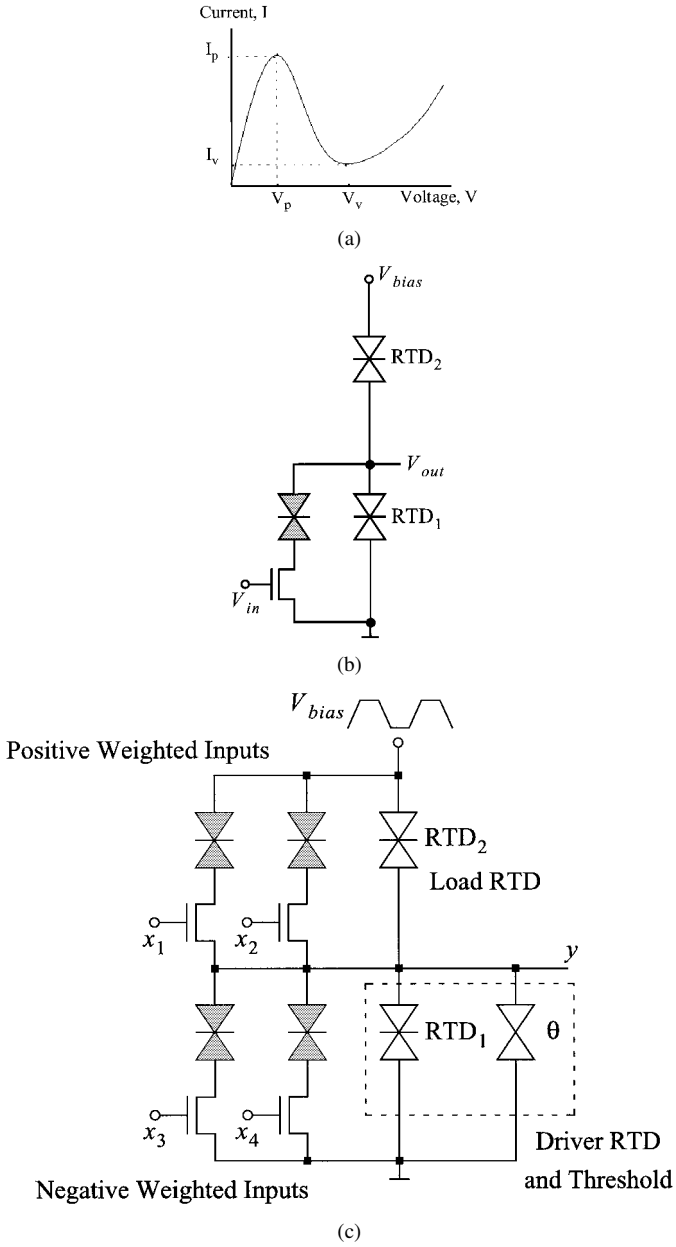

Fig. 39. (a) Current-voltage characteristic of an RTD, (b) an RTD-HFET, and (c) a threshold gate circuit from [207].

embedding an input stage, which modifies the peak current of one of the RTDs.

There are different options for implementing the MOBILE input stage, examples being:

- the series connection of an RTD with a heterojunction field-effect transistor (HFET);
- in parallel to the driver (or load); or
- the one selected to increase the fan-in [207].

When V_{bias} exceeds twice the peak voltage of the RTD, the monostable to bistable transition occurs and results in two self-stabilizing digital output states (on and off states). During a critical period when V_{bias} rises, the voltage at the output node V_{bias} goes to one of the two stable states (low and high corresponding to "0" and "1" in binary logic), depending on which NRD has a smaller peak current. As the peak of RTD_1 can be controlled by an external input signal V_{in}, an inverter function can be obtained.

TLGs implemented with RTDs have been widely studied, as well as their noise margins [199]. Fig. 39(c) shows the RTD implementation of the threshold gate defined as $y = \text{sgn}(x_1 + x_2 - x_3 - x_4 - \theta)$. It is based on the same current controlled switching principle of the MOBILE and, for the sake of robustness mentioned above, is using an RTD-HFET input stage (instead of the original version from [200]). Input stages controlled by external inputs are placed in parallel to RTD_1 and RTD_2 (depending on whether the weight is positive or negative), allowing for the modification of the peak currents of both RTDs. As can be easily seen, there is a striking similarity with the β-comparator [Fig. 27(a)]. Other configurations are possible, but the major advantage comes from the fact that the NRD characteristic directly supports multiple valued logic style [211], making TL an ideal candidate.

RTDs are the most mature type of quantum-effect devices. They exhibit NDR at room temperature and have already been implemented [205]. A prototyping technique based on four MOS-NDR transistors has also been reported [204].

TABLE I
CIRCUITS FABRICATED USING THRESHOLD LOGIC GATES

FUNCTION	CATEGORY	COMMENTS	REF.
Full adder	Static vMOS	double-poly process	[85]
Multiplier cell (plus FA)	Static vMOS	30% area of conventional worse power and speed	[89]
8-input C-Muller	Static vMOS	single nine input gate with feedback area, speed and power advantages over conventional CMOS 0.8 µm process	[81]
3-input EXOR	Clocked-vMOS	3 µm process two stages of floating gate inverters	[76]
Multiplier cell (plus FA)	Clocked-vMOS	50% are of conventional better power over 50 MHz. Better speed	[80]
Sensor array	vMOS	0.65 µm CMOS triple-metal double-poly process	[218]
3 input programable gate (NOR3, NAND3 and CARRY)	2-FGUVMOS	for low voltage applications transistor in subthreshold (its effective threshold is change by UV)	[66]
16 input programable neuron	Conductance	weighths codified as charge in a floating gate 2 µm process only qualitative characterization 1 MHz	[106]
8-input Muller C-element	Conductance	multi-output TLG 1.6 µm process	[100]
Analog rank order filter	CTL	1.2 µm process compares favourably with other reported designs	[215]
MAJORITY	CTL	ORBIT 1.2 µm double-metal double-poly process	[60]
(31,5) parallel counter	CTL	1.2 µm double-poly AMS process Input rate: 16Mvectors/s Area: 0.08mm^2	[57]
(3x3) image filter	CTL	1.2µm double-metal double-poly process	[58]

VI. CONCLUSION

The present state of the art of TL shows a large diversity of solutions for coping with the two major drawbacks of TLGs: power dissipation and reduced noise margins. Several implementation results (representing only a small fraction) are reported in Table I. Some of the solutions presented in this survey are highly advanced: differential and even asynchronous (data-dependent and self-timed; see also [217]). TLG have clearly benefited from developments in the more general field of differential logic structures and will certainly continue to do so. Practically, the power dissipation should not be a major problem anymore. Solutions for enhancing the noise margins have also been proposed and could be used together with differential designs, but TLGs are more sensitive to noise than standard CMOS. Still, for a fair comparison, TLGs should be evaluated against advanced Boolean gates (BGs) such as, e.g., domino logic, and not against standard CMOS.

It is quite amazing how much effort, ingenuity, and tenacity has been spent/invested over several decades to make TL a success, let alone the remarkable diversity of technologies that have been tried and the numerous solutions designed. These efforts have tried to improve the power dissipation, the reduced noise margins, and the sensitivity to process variations. Clearly, fast and low-power TLGs are implementable. The major differences between one particular solution and another are the power-delay tradeoffs, conductance implementations being in general faster than the others (see [24]). Slow and very-low-power solutions (capacitive, differential, data-driven, and asynchronous) are also possible. Lastly, the other design parameter to consider is the fan-in. Only a few solutions allow for really large fan-ins, while most are somehow limited with respect to fan-in. Still, the claim that TLG should have a large fan-in comes from their original goal of mimicking the brain. Theoretical results [212] have shown that small fan-ins (fan-in $= 6 \ldots 9$) can lead to VLSI-optimal solutions. If this were the case, almost all the solutions presented in this survey would qualify.

In addition to hardware neurons, potential applications for TLCs start from general microprocessors, DSPs, and cores where addition, multiplication, and multiply-accumulate are at a premium. Others are floating point units for gaming workstations and graphics accelerators, which could clearly benefit from a boost in speed and/or reduced power. Among the dedicated applications, those that are computationally intensive immediately come to mind: encryption/decryption (RSA, ECC—elliptic curves cryptosystems, AES—Rijndael, etc.), convolution/deconvolution (FFT, DFT, DCT, etc.), compression/decompression (MPEG, etc.), and nonlinear filtering. For example, weighted order statistic filters that can be efficiently implemented with flip-flops and TLGs are widely used in image processing [215]. The first capacitive solution, invented in 1966 [6] and reinvented in 1991 [82], was used after improvements in a CMOS fingerprint sensor array [21]. The output-wired- inverters, discovered in 1973 [98] and rediscovered in 1988 [19], were used in MIPS R2010. Differential solutions were introduced in 1964 [162] and 1967 [158]. Of the many variations that followed, only the CMOS fingerprint sensor array has taken advantage of a differential approach [21]. The earliest pseudo-nMOS power reduction mechanism was introduced in 1975 [118] and has been improved too many times over the years, with a variation being recently used in the Itanium 2 microprocessor [36].

Still, this scarcity of commercial applications is not because TLGs have poor performances. As the results presented in this survey have shown, advanced TLGs can easily compete with BGs. So why are they not used? The answer to this question has its roots in the TL design approach, namely the fact that TLGs need full custom design and that there is a lack of high-level synthesis tools. The usefulness of TL as a design alternative, in general, will be determined not only by the availability, the cost, and the high capabilities of the basic building blocks (the TLGs), but significantly more by the existence of automatic synthesis tools that could take advantage of them. Many logic synthesis algorithms exist targeting conventional BGs, but few (if any) have

been developed for TLGs. The problem was addressed as early as the beginning of the 1970s [34] and several Ph.D. theses have investigated the topic , [213], [214], [216], [218], [219], [221], [222]. Unfortunately, it seems that almost nothing has been done since the 1970s. The two-level (depth-2) LSAT algorithm [220], inspired from techniques used in classical two-level minimization of Boolean circuits, is one remarkable exception. As long as the effort will be put only into improving the gates, there will be few chances for TLCs, except in some dedicated applications and maybe inside a few cores.

Lastly, because nano (and reconfigurable) computing will probably get center-stage positions in the (near) future, TL will surely benefit from that. As RTDs are already operating at room temperature (as opposed to SET), they appear to hold the most promise as a short-to-medium-term solution. The fact that TL is a perfect fit for RTDs will certainly help. This trend is proven by many projects funded by the NSF.

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