VOLTAGE AND CURRENT PROGRAMMED MODES IN CONTROL OF THE Z-SOURCE CONVERTER

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VOLTAGE AND CURRENT PROGRAMMED MODES IN CONTROL OF THE

Z-SOURCE CONVERTER

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Thesis

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ABSTRACT

The Z-source converter (ZSC) is an alternative power conversion topology that can both buck and boost the input voltage using passive components. It uses a unique LC impedance network for coupling the converter main circuit to the power source, which provides a way of boosting the input voltage, a condition that cannot be obtained in the traditional inverters. It also allows the use of the shoot-through switching state, which eliminates the need for dead-times that are used in the traditional inverters to avoid the risk of damaging the inverter circuit.

Dynamic modeling of the ZSC from different perspectives has been studied in the literature. So far, based on these models, the peak dc-link voltage has been controlled using direct measurement, or through indirect control using measurement of the capacitor voltage. Direct measurement control requires a peak detection circuit due to the pulsating nature of the dc-link voltage. Indirect control using the capacitor voltage makes the peak dc-link voltage sensitive to line disturbances.

In this research, the peak dc-link voltage is reconstructed using the measurements of the capacitor and input voltages. The ZSC is then controlled using two methods; namely the Voltage Mode (VM) and Current Programmed Mode (CPM). The two control laws for the ZSC with inductive loading are derived based on a small signal model of the converter. In CPM, since the order of the system is reduced by one, it is possible

to achieve a dynamic performance similar to VM control with a simpler compensator. Performances of both VM and CPM controlled ZSC are verified by the simulation and experimental results for line and load disturbances. The simulation and experimental results for both steady state operation and disturbance rejection cases observed to be comparable. Line disturbance rejection of CPM controlled ZSC is found to be better than the VM control case. Both control methods showed satisfactory dynamics in case of the load disturbance rejection.

ACKNOWLEDGEMENTS

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CHAPTER I

INTRODUCTION

1.1 Research Motivation

In power electronics literature, the level and characteristics of the source voltage have been changed using different converter topologies. Each converter topology has its own limitations regarding different aspects like number of components used, stress on semiconductor switches and converter efficiency. Some of these converters have found places in industry for a variety of applications. Today, efficient power conversion is more important than before because of the alternative energy sources like fuel cells, solar energy, wind energy and ocean wave energy that require proper power conditioning to adapt to different loads. Also hybrid vehicles are very promising new applications of power converters. Moreover, the area of electrical drives is still demanding for new topologies in order to find more efficient and cheaper ways of converting the form of energy from electrical to mechanical or vice versa. Since clean, reliable and high quality energy is one of the main concerns in today's world, power electronics will definitely play an important role in filling this gap.

Because of its interdisciplinary nature, power electronics combines semiconductor devices, digital systems, control theory and power systems. This fact implies that any

innovation in one of these fields affects power electronics and opens for new research opportunities. Among these fields, control theory is in a very close relationship with power electronics. This is because power converters are "variable structure periodic systems" whose state is determined by control signals. In most applications, converter voltages and currents are to be limited by maximum values specified by component vendors and to be strictly controlled around a steady state value defined by the design specifications. This can be achieved by designing controllers based on true mathematical models. As discussed in the literature many times, power converters can be modeled based on averaging state variables over a switching cycle; hence they are suitably conformed for the application of existing control theories.

The Z-source converter (ZSC) is a newly proposed power conversion concept that is very promising in the above mentioned areas of power conditioning especially in alternative energy sources and distributed generation. Z-source inverter (ZSI), which is based on Z-source network, can buck and boost the output AC voltage, which is not possible using traditional voltage source or current source inverters. Also, the ZSI has the unique ability to allow the dc-link of the inverter to be shorted, which is not possible in the traditional voltage source inverters. This improves the reliability of the circuit. Actually concept of boosting the input voltage is based on the ratio of "shoot-through" time to the whole switching period. This thesis presents a continuation of the research that has been recently developed in the area of modeling and control of the ZSC. An acceptable dynamic performance is achieved in [12-14]. However, regarding to the effective control methods like Current Programmed Mode (CPM) control [7], the dynamic performance of the ZSC could be improved further.

1.2 Brief Literature Review

This section gives a review of the research that has been done so far in the literature about controlling the ZSI. Modeling of the ZSC from different perspectives including different loading and filtering conditions are given in [8], [9], [10] and [11]. In [8], modeling of Z-source network with inductive loading is given. In [9] and [10], modeling with an assumption of a constant load current including Z-source network parasitic resistances is given. In [11], modeling and design of a multi-loop controller for distributed generation including a second order filter at the output is given.

An indirect controller for the dc-link voltage on the DC side of the ZSI and a modified space vector PWM for the AC side of the ZSI is given in [12]. Another indirect dc-link voltage controller with a modified modulation method is given in [13]. A PID controller design by direct measurement of the peak dc-link voltage is given in [14]. Finally, controllers designed for specific applications, namely fuel cell and voltage sag compensation are given in [15] and [16].

1.3 Problem Definition

There are two parameters to be changed in order get the desired output AC voltage in a ZSI. The first one is the modulation index, which also exists in traditional voltage source inverters. The second one is the boosting factor, which depends on the shoot-through time. Theoretically, the modulation index can take values from zero to one, while the boosting factor can take values from one to infinity. So their multiplication gives all levels of desired voltages at the output. However, there are some practical

limitations for both parameters. Decreasing the modulation index increases the voltage stress on the switches, whereas controlling the voltage level when shoot-through duty cycle is near 0.5 (or boosting factor is near infinity) becomes hard because of the sharp increase of the voltage gain. Moreover, small signal model of the ZSI shows that there is a non-minimum phase behavior (RHP zero) in the control-to-capacitor voltage transfer function, which limits the control range of the system.

The results given in [12-14] show good transient response in terms of reference tracking and disturbance rejection. However, there are limitations some of which were also mentioned in [14]. These limitations can be summarized as follows:

- The control method mentioned in [12-13] is based on indirect control of the peak dc-link voltage of the ZSC by controlling the capacitor voltage in Z-source network. Figure 1.1 shows the indirect control of the ZSI where the Z-source network is cascaded with a 3-phase bridge. Here the average capacitor voltage is kept constant using a compensated voltage loop. But as will be shown later, it is not possible to keep the peak dc-link voltage constant by only controlling the capacitor voltage. For example, in the case of a step change in the input voltage, the capacitor voltage will be kept constant but the peak dc-link voltage will change. This is not desired because a change in the peak dc-link voltage will affect the output AC voltage, which may force one to change the modulation index. This may result in a higher switch stress and a distorted output voltage waveform.

- In order to keep the peak dc-link voltage constant another control method is discussed in [14] using direct measurement of the peak dc-link voltage. Figure 1.2 shows a block diagram of the direct measurement control. Because of the pulsating nature of the dc-link voltage, direct measurement will require a peak detection process with an additional circuitry which makes the control more complex. A detailed discussion on this additional circuitry is given in [14].

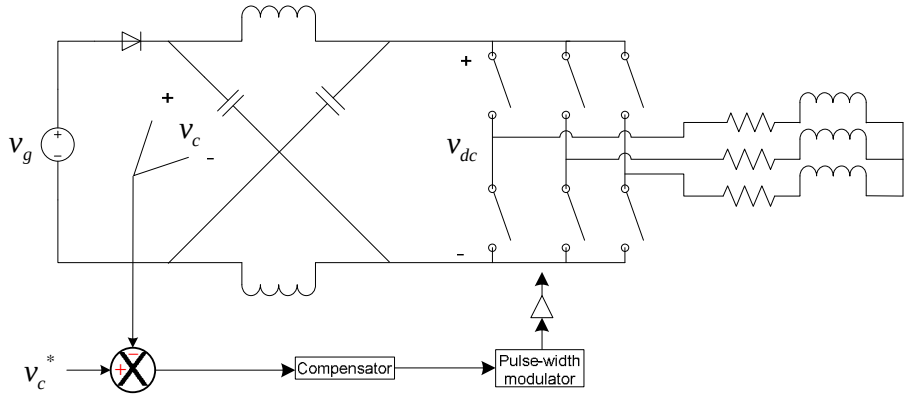


Figure 1.1 Indirect control of the dc-link voltage by controlling the capacitor voltage

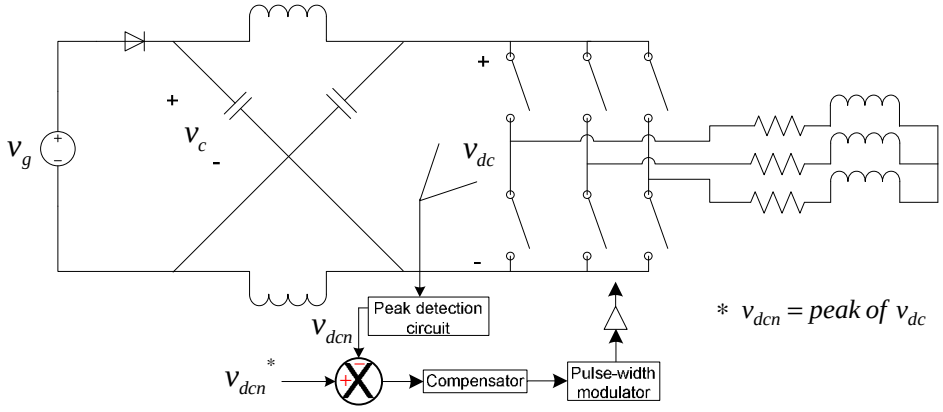


Figure 1.2 Control of the dc-link voltage by direct measurement

A method is needed for controlling the dc-link voltage boost without measuring the pulsating dc-link voltage itself and avoiding the above mentioned effects of indirect dc-link voltage control. Also a proper compensator is to be designed based on the transfer functions of the system so that the non-minimum phase behavior is minimized and a good transient performance is guaranteed.

1.4 Thesis Contribution

The method proposed in this research aimed to overcome the two limitations mentioned in the previous section. Figure 1.3 shows a basic block diagram of the proposed method and Figure 1.4 shows the simplified ZSC circuit used to verify the validity of the proposed method. This method controls the dc-link voltage by avoiding direct measurement. Therefore, it eliminates the peak detection circuitry given in [14]. Also, since this method controls dc-link voltage itself rather than controlling only the capacitor voltage, it avoids the problems faced in [12-13].

The proposed control method is based on measuring the input voltage and the capacitor voltage and estimating the peak dc-link voltage based on these voltages. The disadvantage is that two measurements are required instead of one. The proposed method is applicable to both Voltage Mode (VM) and Current Programmed Mode (CPM). In VM control, the estimated value of the peak dc-link voltage is compared to the desired value and the error is compensated through a PID compensator. This compensator is designed based on the model given in [8]. In CPM, the outer loop produces a current command from the difference between the estimated and the desired values of the peak dc-link voltage. This current command is used in the inner loop to control the inductor current.

The small signal model of the Z-source network is verified by comparing the results obtained from the derived averaged small signal model and the actual switching circuit waveforms. Compensators are designed for both cases based on the transfer functions driven from the models. The compensated converters are simulated and the theoretical results are verified by simulation and experimental results.

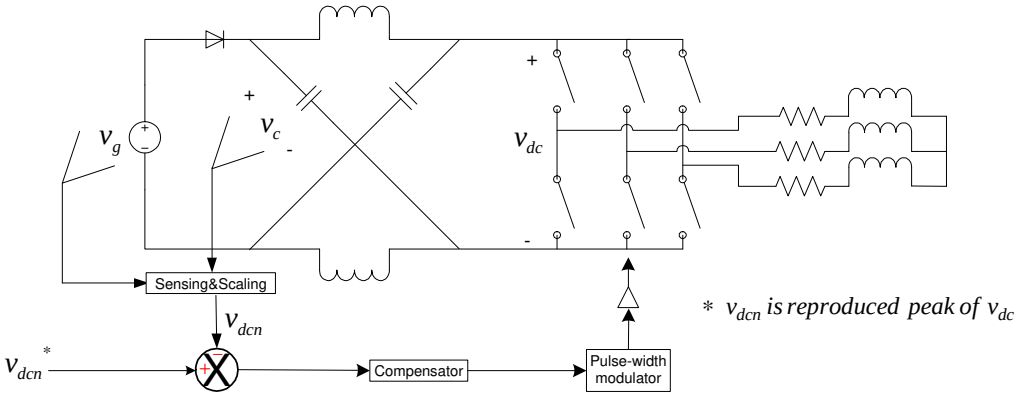


Figure 1.3 Control of the dc-link voltage by estimation without direct measurement

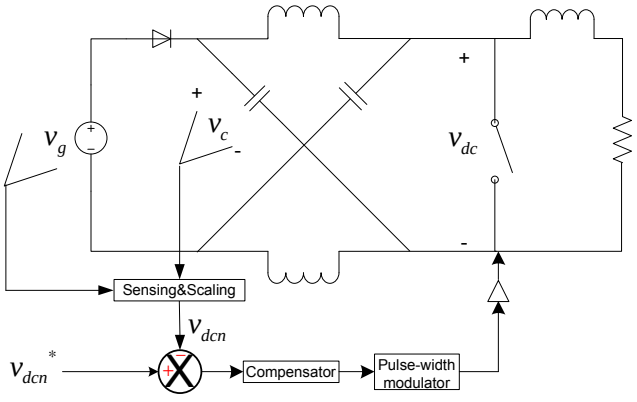


Figure 1.4 Simplified ZSC used for this research

1.5 Thesis Organization

The thesis introduction addressed the research trends in the area of power converters. A brief literature review about modeling and control of the ZSC is followed by definition of the closed loop control problem and explanation of the proposed solution.

Chapter II describes the basic architecture of a power converter and classification of different power converter topologies. Also, voltage conversion ratios and switching methods of basic DC/DC and DC/AC converters are reviewed in this chapter.

Chapter III presents the ZSC topology and its steady state operation together with the voltage conversion ratios. A literature review of the existing modulation and boosting strategies as well as possible application areas of the ZSC is also given.

In Chapter IV, the small signal model of the ZSC is derived using the state space averaging technique based on the derivations in the literature. Also the validity of the derived model is verified through simulation of the averaged and switching circuits.

Chapter V gives the definition and verification of the proposed control strategy and the design process of the closed loop compensator for VM control. In Chapter VI, the CPM model of the ZSC is derived and a closed loop controller is provided based on the derived model.

Chapter VII gives the performances of the designed controllers for both VM and CPM operations. Experimental setup is explained in detail and steady state operation results as well as line and load disturbance cases are presented. Chapter VIII concludes this thesis and presents future research topics on modeling and control of the ZSC.

CHAPTER II

POWER CONVERTERS

2.1 Introduction

Power converters are used for electrical power processing. They change the typical characteristics of electrical energy such as voltage level and frequency. Figure 2.1 shows the block diagram of a typical power converter. Here raw input power is processed according to the control command, which yields the desired form of output power. Control is invariably required in power converters. Generally the objective is to have a well regulated output voltage, in the presence of line and load variations. The line can be a constant DC source such as a battery or fuel cell or a periodic AC voltage current source such as the utility or output of a generator. The load can be a network composed of one or more of passive circuit elements or another electrical source, or an electromechanical energy conversion device. Input and output filters are combinations of energy storage elements like inductor (L) and capacitor (C), provide filtering to eliminate switching noise or Electromagnetic Interference (EMI). Although feedback is generally from load, it can also be from the switch network as well as input and output filters depending on the control algorithm.

In this chapter, a brief review of different power converter topologies that are widely used is given. After introducing the basic classification of power converters,

operating principles and steady state relations are given. Information given in this chapter can be regarded as a reminder and is well established in the power electronics literature. So, it is encouraged to inspect the given references for further details.

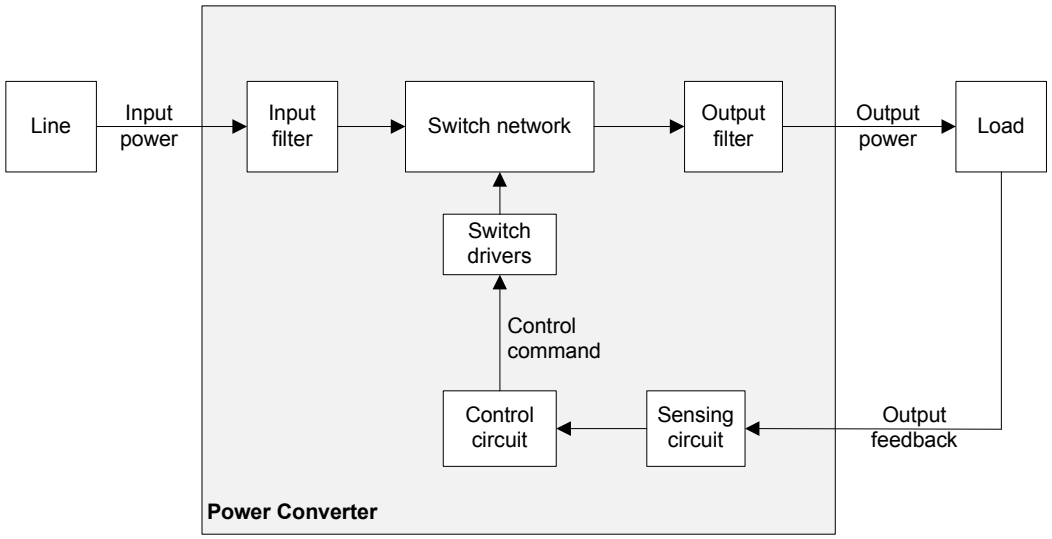


Figure 2.1 Block diagram of a typical power converter

2.2 Basic Power Converter Topologies

Although the basic architecture of a power converter is the same as in Figure 2.1 for most of the converters, many different topologies have been produced by manipulating the structures of the input filter, the output filter and the switch network [1-2]. Depending on the desired function of the power converter, other circuit elements that perform auxiliary functions (such as isolation and protection) can be added. Nevertheless this does not affect the main function of a power converter which is shaping the electrical energy to a certain form.

Power converters can be classified into four categories on the basis of the type of input line and desired load characteristics [3]:

1. DC/DC converters
2. DC/AC converters (inverters)
3. AC/DC converters (rectifiers)
4. AC/AC converters (cycloconverters or AC controllers)

Numerous converter topologies under each category are well defined in the literature in terms of their steady state operations, dynamic models and control schemes, and their applications. Following sections will give a brief review of some basic topologies under the categories of DC/DC converters and DC/AC converters regarding their relation to our research.

2.3 DC/DC Converters

Figure 2.2 shows the simplest form of a DC/DC converter. S_1 acts as a series element with an average voltage drop equal to the difference of the two terminal voltages (v_1 and v_2). Similarly S_2 acts as a shunt element with an average current equal to the addition of two terminal currents, regarding to the respective polarities. C and L are energy storage elements filtering i_1 and v_2, respectively. Input and output terminals are defined according to the power flow direction which is determined by how the switches are controlled [1,4].

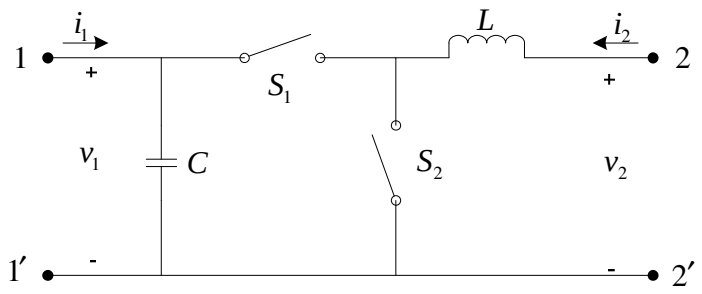


Figure 2.2 Basic topology for a DC/DC converter

Figure 2.2 is also known as the canonical switching cell which is the basic building block for all DC/DC converters. Figure 2.3(a) shows the canonical cell redrawn symmetrically with a single pole double throw (SPDT) switch. Different topologies produced using this cell differ in the way the external systems are connected to the cell. If node A or B is connected as common node; resulting structure is the direct converter (Figure 2.3(b)) or if node C is connected as common node; the circuit becomes the indirect converter (Figure 2.3(c)). The distinction between the direct and indirect converters comes from the fact that the direct converter has a direct DC path between the input and output terminals where in the indirect converter there is none. This points out the main difference among numerous DC/DC converter topologies.

The two well known examples of the direct converter are the *buck* and *boost* converters as shown in Figure 2.4. Here the only structural difference is the way the SPDT switch is implemented in the direct converter. Defining the duty ratio as the time that the controllable switch is on, conversion ratios for both converters can be derived as:

$$\frac{V_{out}}{V_{in}} = \frac{V_2}{V_1} = D \ \ (buck) \qquad \frac{V_{out}}{V_{in}} = \frac{V_1}{V_2} = \frac{1}{1-D} \ \ (boost) \tag{2.1}$$

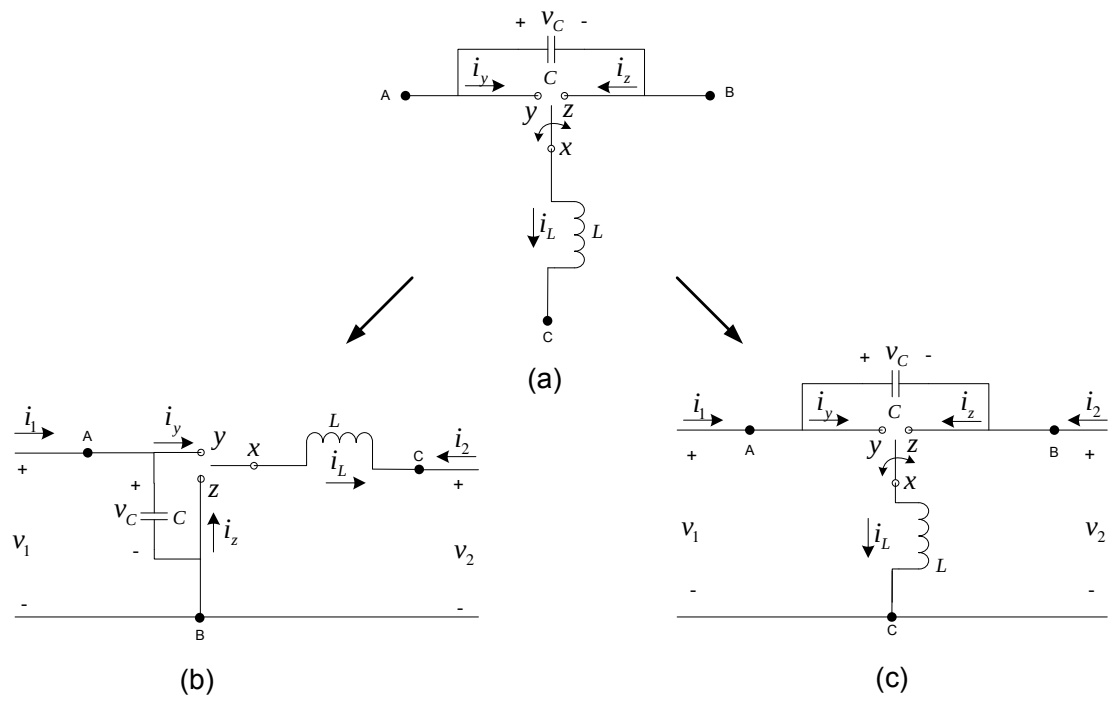


Figure 2.3 (a) the canonical switching cell (b) direct (c) indirect converters

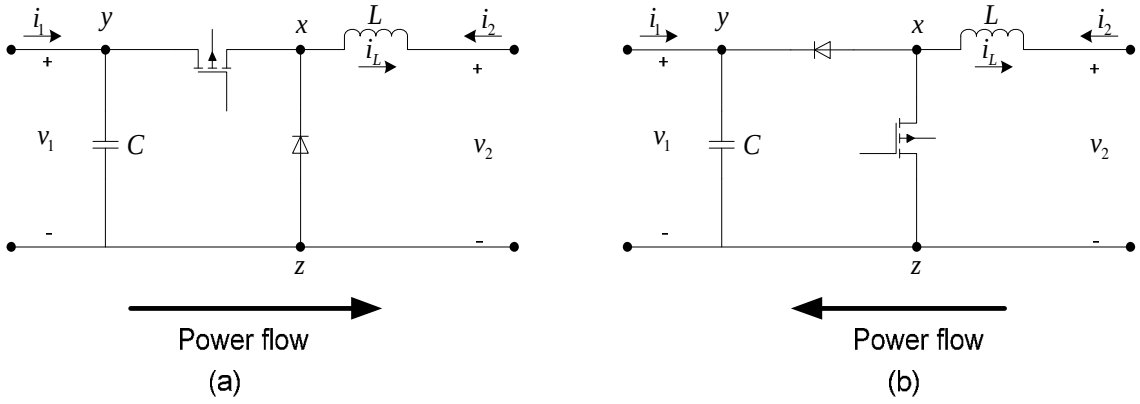


Figure 2.4 Switch implementations of direct converter (a) buck (b) boost

Switch implementation of the indirect converter can be realized as in Figure 2.5. Further modifications on this circuit result in well known topologies such as buck-boost

and cuk converters [1]. Conversion ratio of this circuit can be derived knowing that the average voltage across the inductor is zero over a switching cycle as:

$$\frac{V_{out}}{V_{in}} = \frac{V_2}{V_1} = -\frac{D}{1-D} \tag{2.2}$$

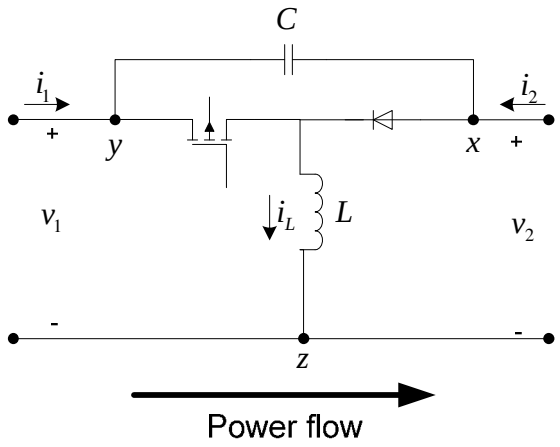


Figure 2.5 Switch implementation of the indirect converter

2.4 DC/AC Converters (Inverters)

A typical DC/AC converter system is shown in Figure 2.6. Two common types of DC/AC converters are single phase inverters and three phase inverters. Input is from AC source (voltage or current) and the output is desired to be a sinusoidal voltage or current with a zero DC component. The load can be a passive R-L-C network, an AC voltage sink, or an AC current sink. Control parameter can be an angle, a pulse width, a voltage or a current signal.

The simplest form of a DC/AC converter is shown in Figure 2.7(a), which is known as the single phase bridge. Single phase DC/AC conversion can be obtained by

alternately opening and closing the diagonal switch pairs, i.e. $S_1 - S_4$ or $S_2 - S_3$, respectively. Figure 2.7(b) shows the output voltage waveform, where either the input voltage or its negative counterpart is seen at the output depending on the switch states. Here the parameters of the AC voltage (its RMS value or the amplitude of its fundamental component) are constant [1].

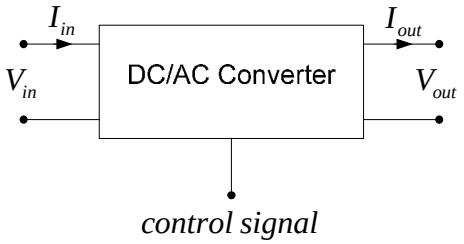


Figure 2.6 DC/AC converter block diagram

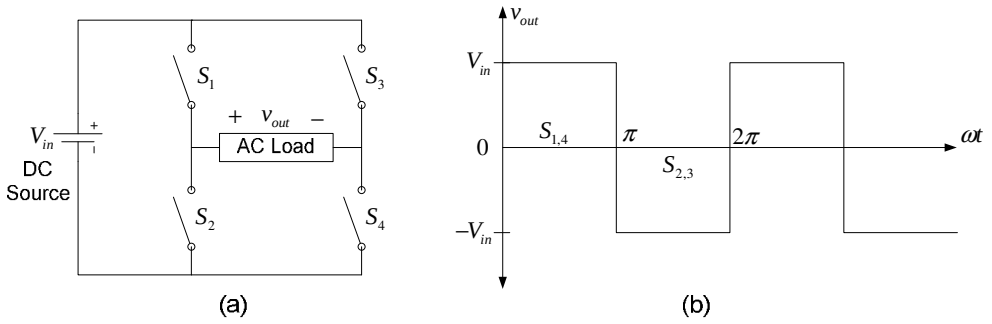


Figure 2.7 (a) Single phase bridge inverter (b) waveform of the output AC voltage

A common way of varying the AC voltage parameters is to introduce a third state which is called the zero state. The zero state can be obtained by closing either the upper leg switches ($S_1 - S_3$) or lower leg switches ($S_2 - S_4$). Figure 2.8(a) shows the output AC voltage of the single phase inverter in Figure 2.7(a) when the zero state is used to change

the AC voltage parameters. Different methods of harmonic cancellation at the output by introducing this zero state is explained in [1].

Pulse Width Modulation (PWM or wave-shaping) technique is also very common in DC/AC conversion. Using this high frequency switching technique, it is possible to eliminate the undesirable low frequency harmonics and high frequency switching harmonics are easy to filter. The output waveform of the single phase inverter in Figure 2.7(a) is shown in Figure 2.8(b) when PWM technique is used. Here two of the four switches ($S_1 - S_2$) are switched at high frequency and the other two ($S_3 - S_4$) are switched at low frequency. Low frequency variation of the fundamental component can be observed after proper filtering [1].

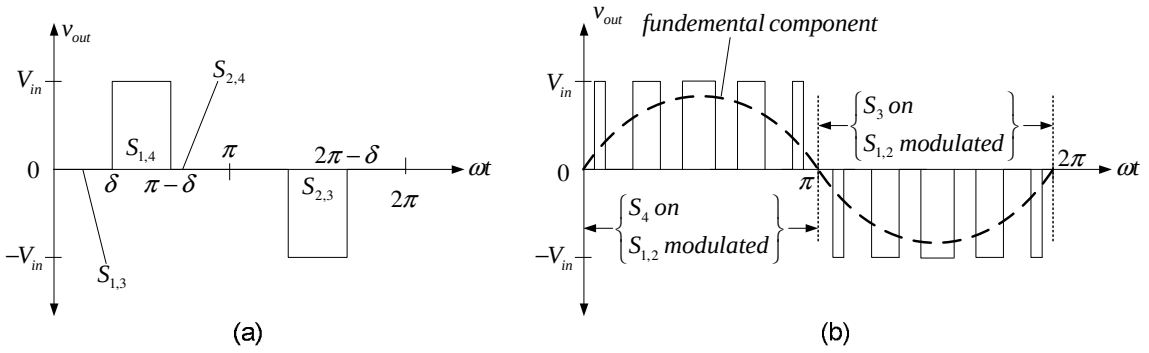


Figure 2.8 Output AC voltage (a) with zero state (b) with PWM control

Many applications in industry require three phase AC sources with varying frequencies. A three phase DC/AC converter can be obtained by replacing the single phase bridge with a three phase bridge which is shown in Figure 2.9(a). Figure 2.9(b) shows the corresponding phase-to-phase output voltage waveforms of the three phase bridge when the upper and lower leg switches are opened and closed accordingly.

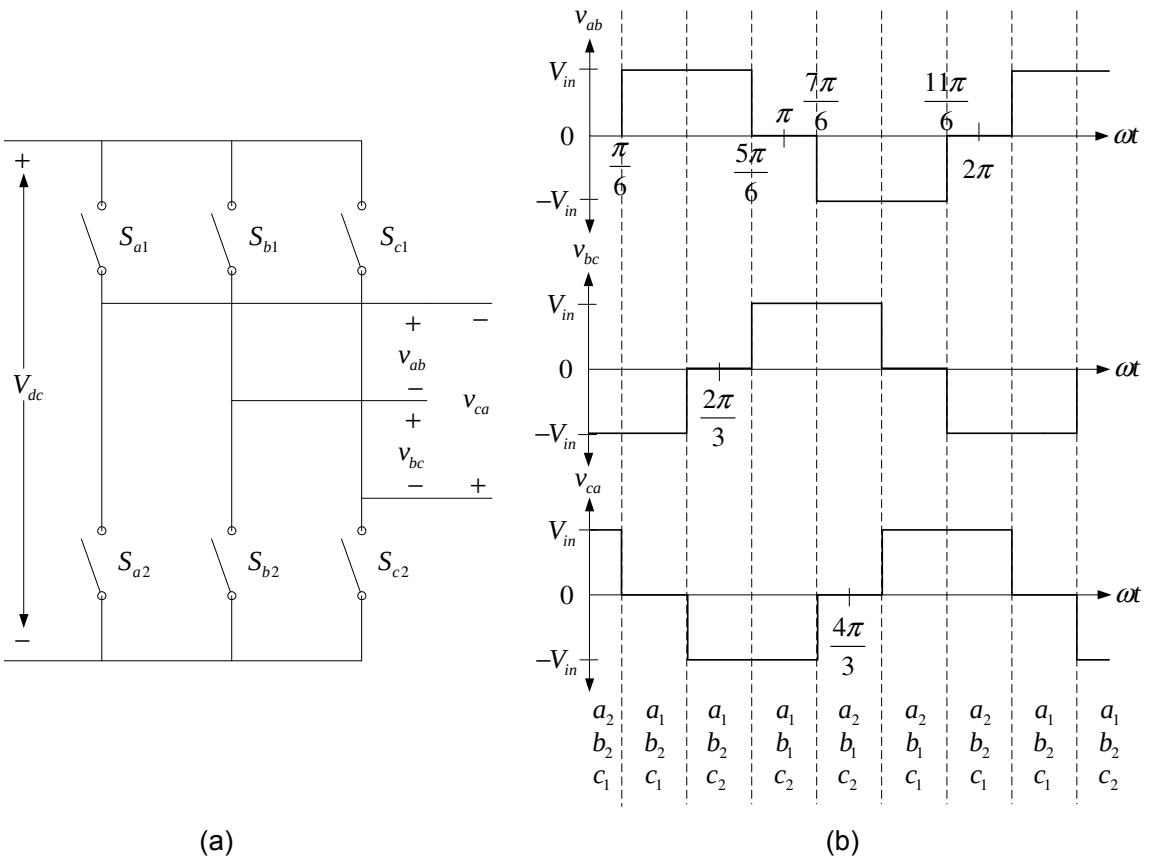
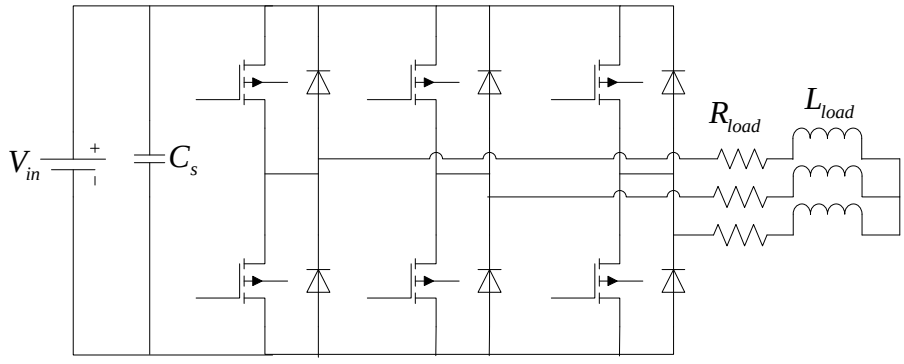
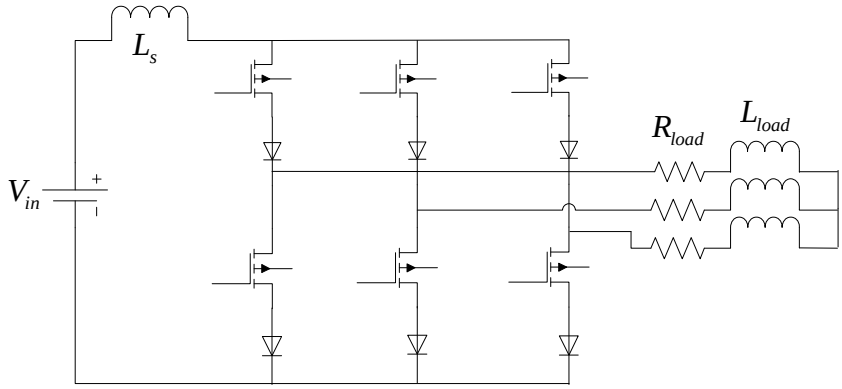


Figure 2.9 (a) 6-switch 3-phase bridge (b) phase-to-phase output waveforms and corresponding switch positions

Two basic types of DC/AC converters are voltage source inverter (VSI) and current source inverter (CSI) as shown in Figure 2.10. VSI is fed by a DC voltage source supported by a large capacitor. The DC voltage source can be a battery, fuel cell stack or an AC/DC converter. The bridge cascaded to the source is composed of switches with anti-parallel diodes allowing bidirectional current flow and unidirectional voltage blocking capability. Similarly a large inductor in series with a DC voltage source acts as a DC current source in CSI. Switch implementation is made with switches in series with diodes providing bidirectional voltage blocking and unidirectional current blocking [5].



(a)



(b)

Figure 2.10 Three-phase inverters distinguished by their sources (a) VSI (b) CSI

Both VSI and CSI has the following theoretical limitations which makes them hard to use for some applications without additional circuitry.

1. The VSI is a buck (down) inverter where AC output voltage cannot exceed DC input voltage. CSI is a boost (up) inverter where AC output voltage is always greater than the DC voltage feeding the inductor. For applications exceeding available voltage range an additional boost (or buck) DC/DC converter is needed. This increases the system cost and decreases the efficiency.

2. For a VSI, the upper and lower switches cannot be on simultaneously which may cause a short circuit. On the other hand for a CSI one of the upper switches and one of the lower switches have to be on to provide a path for the continuous input current. The VSI (CSI) requires dead time (overlap time) to provide safe commutation which causes waveform distortion.
3. In a CSI, switch implementation requires diodes in series with the switches. This prevents the use of low cost switches which come with anti-parallel diodes implementation, as is usually manufactured.

CHAPTER III

THE Z-SOURCE CONVERTER

3.1 Introduction

The Z-source converter (ZSC) is a new topology in power conversion, which has unique features that can overcome the limitations of VSI and CSI [5]. Figure 3.1 shows the ZSC implemented as a 3-phase DC/AC converter (inverter). Although DC/AC conversion is the most common application of the Z-source topology, it can also be applied to AC/DC and AC/AC power conversions [24-25]. The X shape impedance is the Z-source network which is composed of two split inductors and two capacitors to provide a coupling between the DC source and the inverter bridge.

The Z-source inverter (ZSI) has the unique buck-boost capability which ideally gives an output voltage range from zero to infinity regardless of the input voltage. This is achieved by using a switching state that is not permitted in the VSI which is called the "shoot-through" state. This is the state when both upper and lower switches of a phase leg are turned on. In a conventional VSI switching pattern, there are eight permissible switching states. Six of those switching states are called the "active" states where the load sees the input voltage and the remaining two states are called the "zero" states where either all the upper or all the lower switches are on and the load sees zero voltage.

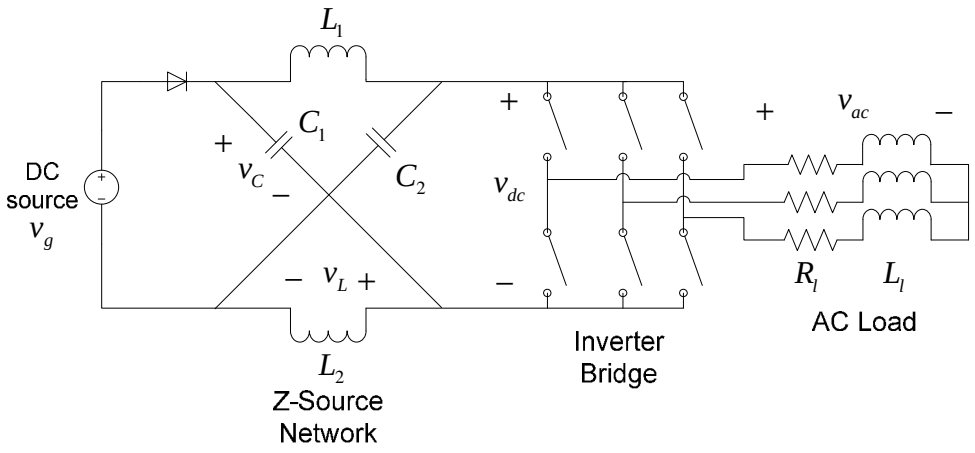


Figure 3.1 ZSC implemented as a three-phase inverter (ZSI)

Figure 3.2(a) shows the carrier based PWM switching pattern for a VSI. According to this switching method, the reference signals for the three phase voltages are compared to a triangular carrier signal. If a reference signal is greater than the carrier signal, the upper switch in the leg of the corresponding phase becomes on and the lower switch of the same phase leg becomes off and vice versa. All of the 8 permissible switching states of a VSI can be distinguished from Figure 3.2(a) including the two zero states. First zero state occurs when the carrier wave is greater than all of the reference signals, i.e. all the upper leg switches are on and the lower leg switches are off. The second zero state occurs when the carrier wave is smaller than all of the reference signals.

The shoot-through state can be distributed among the carrier based switching pattern of the VSI in Figure 3.2(a) without distorting the carrier based PWM signal generation. Figure 3.2(b) illustrates the addition of the shoot-through state as equally distributed amounts of time inside the zero states. It can be seen from Figure 3.2(b) that the active states for both carrier based PWMs are the same for the VSI and the ZSI. This

guarantees that the modulation index (M) which is defined as the ratio of the total active states to the whole period, is the same for both switching patterns.

Another advantage of the ZSI compared to the VSI appears in the practical implementation of the carrier based PWM switching pattern. For protection purposes it is necessary to put "dead times" during the transitions from one switching state to the other. This causes output waveform distortion. Due to the unique impedance network that ZSI uses, the dead times are not necessary.

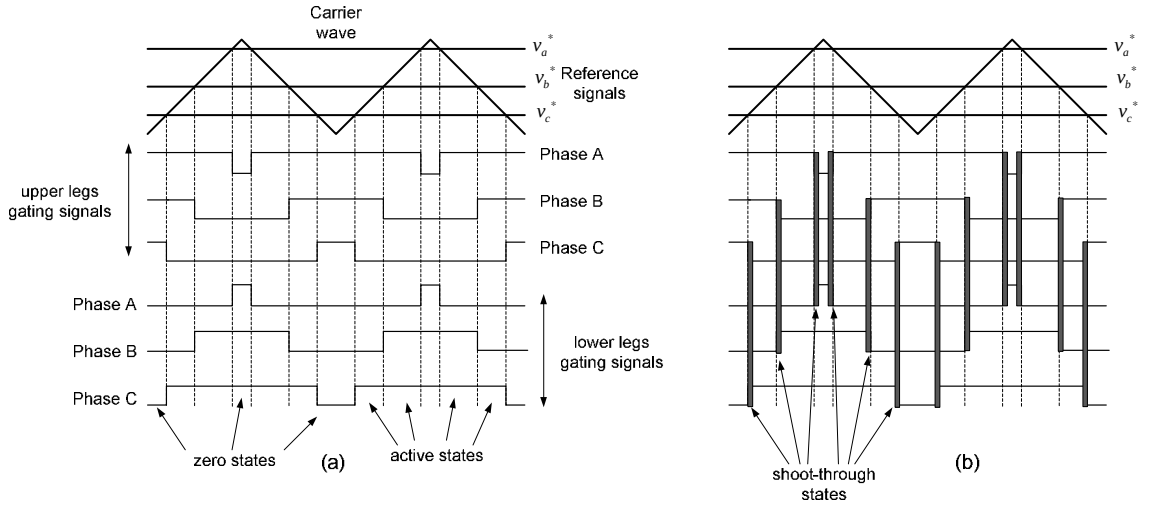


Figure 3.2 (a) Carrier based PWM for VSI (b) Modified carrier based PWM for ZSI

3.2 Steady State Operation

In order to do the steady state analysis and find the conversion ratio of the ZSC, we will reduce the circuit in Figure 3.1 to Figure 3.3. The idea behind this is that when we look from the Z-source network point of view, in the shoot-through state of Figure 3.2, the Z-source network is shorted and in the active state, the Z-source network sees the load. This behavior can be simplified using the circuit given in Figure 3.3. In this circuit,

when the parallel switch S_2 is on, the Z-source impedance network is shorted and the load sees zero voltage. Similarly, when S_2 is off, the Z-source network sees the load and active state occurs as in Figure 3.2(a). It can be observed that the dc-link voltage (v_{dc}) in Figure 3.3 has a pulsating nature. For simplification purposes, Z-source network parameters are selected as; $L_1 = L_2$ and $C_1 = C_2$ which makes the Z-source network symmetrical [8]. Accordingly, the capacitor and inductor voltages of the Z-source network become,

$$v_{C1} = v_{C2} = v_C \text{ and } v_{L1} = v_{L2} = v_L \tag{3.1}$$

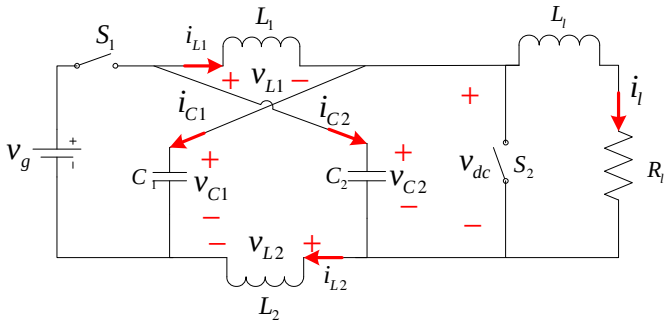


Figure 3.3 Simplified ZSC

In Figure 3.3, v_C is the capacitor voltage and v_L is the inductor voltage. Given that the converter is in the shoot-through state for an interval of T_o during a switching cycle T, from the equivalent circuit in Figure 3.4 we have,

$$\begin{aligned} v_L &= v_C \\ v_{dc} &= 0 \end{aligned} \tag{3.2}$$

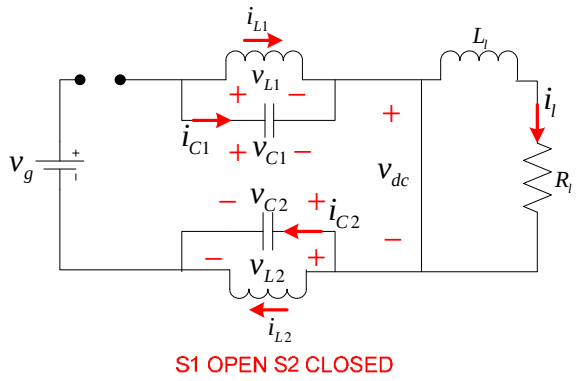


Figure 3.4 Shoot-through state of simplified ZSC

Similarly, if the converter is in the active state for an interval of T_1, during the switching cycle T, from the equivalent circuit in Figure 3.5 we have,

$$\begin{aligned} v_L &= v_g - v_C \\ v_{dc} &= v_C - v_L = 2v_C - v_g \end{aligned} \tag{3.3}$$

where v_g is the DC source voltage and $T = T_0 + T_1$.

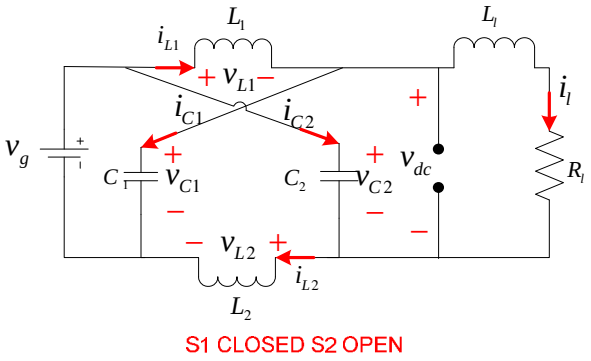


Figure 3.5 Active state of simplified ZSC

The average value of the voltage across an inductor for a switching period (T) is zero in steady state, so from Eq. (3.2) and Eq. (3.3) we have,

$$\frac{1}{T}\int_0^T v_L(t)dt = \frac{T_0 V_C + T_1(V_g - V_C)}{T} = 0 \tag{3.4}$$

or,

$$\frac{V_C}{V_g} = \frac{T_1}{T_1 - T_0} = \frac{1-D}{1-2D} \tag{3.5}$$

where $D = T_o / T$ is the shoot-through duty cycle, V_C is the steady state (DC) value of the capacitor voltage and V_g is the steady state value of the input voltage. The peak value (v_{dcn}) of the pulsating dc-link voltage (v_{dc}) is expressed in Eq. (3.3) and it can be rewritten in steady state as,

$$V_{dcn} = 2V_c - V_g = \frac{T}{T_1 - T_0}V_g = \frac{1}{1-2D}V_g = BV_g \tag{3.6}$$

where B is known as the boosting factor based on D, and V_{dcn} is the steady state value of the peak dc-link voltage. Eq. (3.6) gives the voltage conversion ratio of the ZSC. Since D is between zero and 0.5, B can take any value between one and infinity. The output peak phase voltage (V_{ac}) of the ZSI in Figure 3.1 can be expressed as,

$$V_{ac} = M\frac{V_{dcn}}{2} \tag{3.7}$$

where M is the modulation index of the inverter. Using Eq. (3.6), Eq. (3.7) can be rewritten as,

$$V_{ac} = MB\frac{V_g}{2} \tag{3.8}$$

Eq. (3.8) has an additional multiplication factor of B compared to the VSI voltage conversion ratio which gives the boosting capability to the Z-source inverter [5].

3.3 Modulation of the Z-Source Inverter

It was illustrated in Figure 3.2 that the shoot through states of the ZSC can be distributed among the PWM switching pattern of a VSI [5]. It was also mentioned that in order not to distort the output waveform, it is necessary to keep the active states the same as in the VSI PWM switching pattern. Possible switching state sequences and the respective carrier based implementations of the PWM switching of Z-source inverters with different number of output phases are explained in [26]. This section will summarize how to introduce the shoot-through states appropriately to the modulation of an H-bridge (single phase) Z-source inverter based on the explanations in [26].

Consider the H-bridge Z-source inverter in Figure 3.6 whose switching states are given in Table 3.1. The active and null states in which the two switches of a phase-leg are switched complementary, are common to both conventional VSI and the H-bridge Z-source inverter. However, the remaining three shoot-through states in which one phase-leg (H1 and H2) or two phase-legs (H3) are short-circuited, are unique to the H-bridge Z-source inverter [26].

Based on the discussion in the previous section and Table 3.1, it can be observed that when in a shoot-through state, the Z-source inductor currents are boosted but the inverter output voltage is kept at $0V$, similar to that of a null state where the AC load is short-circuited. Therefore, for a fixed frequency, inserting of shoot-through states within the null intervals with the active state intervals maintained constant will not alter the normalized volt–sec average per switching cycle. This feature allows all existing volt–sec PWM methods to be used for controlling a Z-source inverter with only minor modifications added to insert the shoot-through states [26].

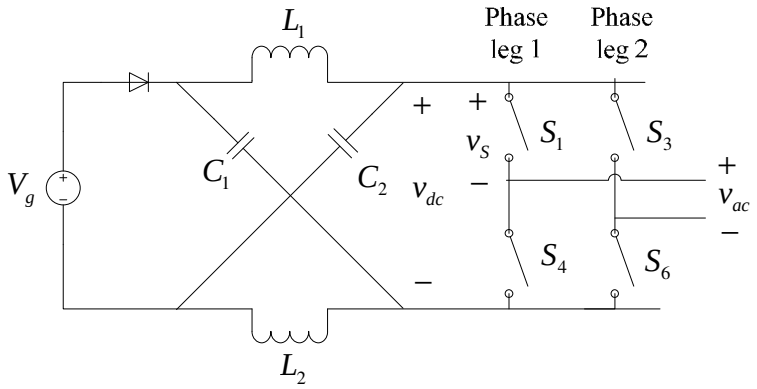


Figure 3.6 H-bridge (single phase) Z-source inverter

Figure 3.7 shows a possible PWM switching configuration of a conventional single-phase VSI and a single-phase Z-source inverter. For conventional VSI modulation, two state transitions occur per switching cycle (e.g., null{00} → active{10} → null{11}) with the active state centrally placed within the switching period to minimize the generated harmonic distortion [27].

Table 3.1 Switching States of the H-bridge Z-source inverter ($!S_x$ is complement of S_x)

State (output voltage)	S_1	S_3	S_4	S_6
Active {10} (non-zero)	1	0	0	1
Active {01} (non-zero)	0	1	1	0
Null {00} (zero)	0	1	0	1
Null {11} (zero)	1	0	1	0
Shoot-through H1 (zero)	1	1	S_3	$!S_3$
Shoot-through H2 (zero)	S_1	$!S_1$	1	1
Shoot-through H3 (zero)	1	1	1	1

For Z-source inverter modulation, additional shoot-through states are carefully added to the null intervals with the active interval kept constant and centrally placed within the switching period to retain all the harmonic benefits of central active state placement. The shoot-through states should preferably have the same time interval to minimize the size of the Z-source network inductors [5], and should be added immediately adjacent to the instants of state transitions of a conventional VSI to ensure a single device switching per state transition. Therefore, for a single-phase Z-source inverter with two state transitions per switching cycle, the number of equal-interval ($0.5T_o$) shoot-through states that can be inserted is two. Their inclusions are shown in Figure 3.7 [26].

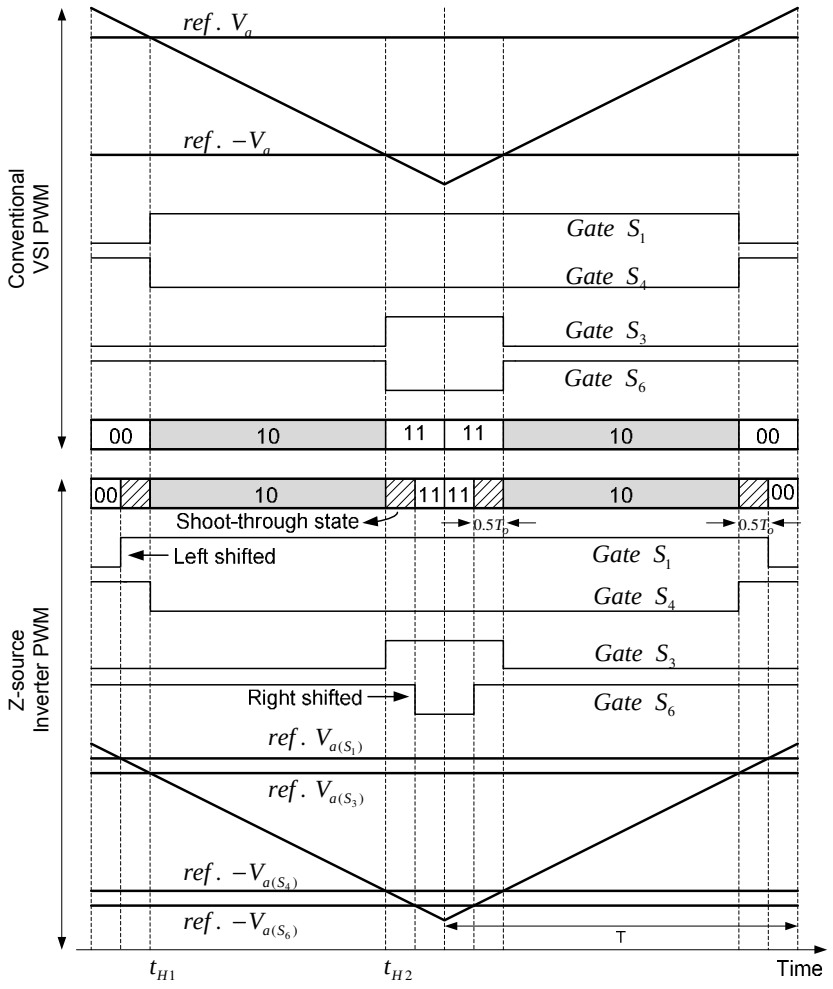


Figure 3.7 Modulation of H-bridge Z-source inverter

In order to build the preferred state sequence in Figure 3.7 through carrier-based implementation regarding to the reference/carrier comparison diagrams in Figure 3.7, the formulation of modulating reference signals are needed for carrier-based Z-source inverter modulation. For a conventional VSI, the reference signals used are $V_a = M\cos(\omega t)$ for modulating phase-leg $\{S_1, S_4\}$, and $-V_a$ for phase-leg $\{S_3, S_6\}$. In general, the first state transition during the falling carrier edge occurs when the maximum of the two signals $V_{\max} = \max(V_a, -V_a)$ crosses the falling slope of the carrier at time t_{H1}.

In order to insert a shoot-through state adjacent to this transition from $t_{H1} - 0.5T_o$ to t_{H1}, the upper (odd-numbered) and lower (even-numbered) switches of the relevant phase-leg should therefore be modulated using

$$\begin{aligned} V_{\max(SX)} &= V_{\max} + T_o / T \\ V_{\max(SY)} &= V_{\max} \\ \{X, Y\} &= \{1,4\} \text{ or } \{3,6\} \end{aligned} \tag{3.9}$$

where $V_{\max(SX)}$ causes the upper switch to turn ON at $t_{H1} - 0.5T_o$ and $V_{\max(SY)}$ causes the lower switch to turn OFF at t_{H1}. Obviously, these switching actions insert the desired shoot-through state H1, as illustrated in the lower half of Figure 3.7.

Following through similar analysis, the second shoot-through state H2 can be inserted from t_{H2} to $t_{H1} + 0.5T_o$ by using the following modified reference signals for controlling the other two switches

$$\begin{aligned} V_{\min(SX)} &= V_{\min} - T_o / T \\ V_{\min(SY)} &= V_{\min} \\ \{X, Y\} &= \{1,4\} \text{ or } \{3,6\} \end{aligned} \tag{3.10}$$

where $V_{\min} = \min(V_a, -V_a)$ represents the minimum of V_a and $-V_a$. Without modification, the same derived equations (3.9) and (3.10) can also be used for ensuring the correct insertion of shoot-through states during the rising carrier edge.

For a three-phase-leg VSI, both continuous switching (e.g., centered SVM) and discontinuous switching (e.g., 60^o–discontinuous PWM) are possible with each having

its own unique null placement at the start and end of a switching cycle and characteristic harmonic spectrum. Similar to the derivation of the PWM switching pattern for H-bridge Z-source inverter, it is possible to derive various PWM strategies for a three-phase-leg Z-source inverter [26].

3.4 Boosting Methods

In the previous section it was mentioned that the shoot-through states can be introduced into a VSI PWM switching pattern. This section gives a brief explanation of the possible boosting methods for a 3-phase Z-source inverter dc-link voltage (v_{dc}) based on [28] and [29].

In [5], a simple boosting method was used to control the shoot-through duty ratio. Figure 3.8 illustrates the simple boosting method that employs a straight line (V_P) equal to or greater than the peak value of the three phase references to introduce the shoot-through duty ratio in a traditional sinusoidal PWM. Here if the triangular carrier signal is greater than V_P or smaller than V_N, the Z-source inverter is in shoot-through state. The Z-source inverter maintains the six active states unchanged as in the traditional carrier based PWM control. For this simple boosting method, the obtainable shoot-through duty ratio decreases with the increase of the modulation index (M). The maximum shoot-through duty ratio of the simple boosting method is limited to $1-M$, thus reaching zero at a modulation index of one. In order to produce an output voltage that requires a high voltage gain, a small modulation index has to be used. However, small modulation indexes result in greater voltage stress on the devices [28].

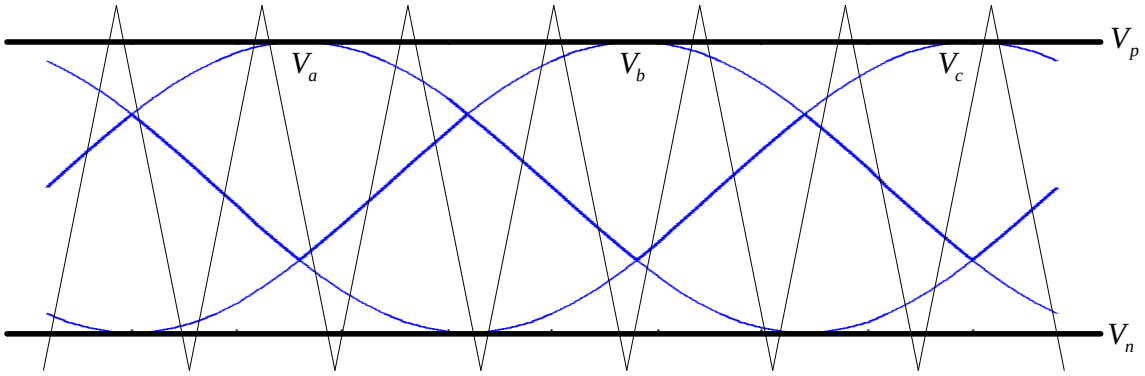


Figure 3.8 Simple boosting PWM generation waveforms of the ZSC

Based on Eq. (3.8), the voltage gain of the Z-source inverter can be written as

$$G = \frac{V_{ac}}{V_g / 2} = MB = \frac{M}{2M - 1} \tag{3.11}$$

As analyzed in [5], the voltage stress V_s (Figure 3.6) across the switches is BV_g. The voltage stress under simple boosting modulation method can be calculated by

$$V_s = BV_g = (2G - 1)V_g \tag{3.12}$$

The voltage stress across switches versus the voltage gain is plotted in Figure 3.9. Using the simple boosting method, the voltage stress across the switches is quite high, which will restrict the obtainable voltage gain because of the limitation of device voltage ratings [28].

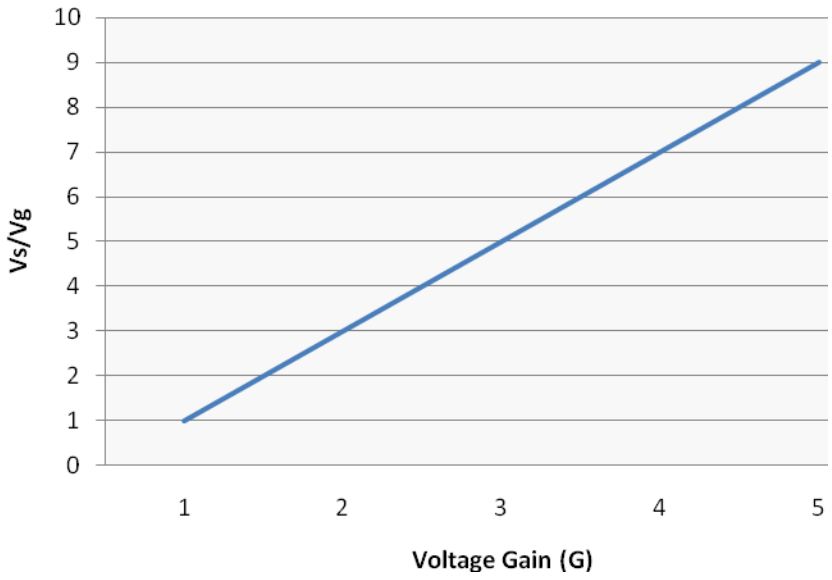


Figure 3.9 Switch voltage stress versus voltage gain in simple boosting method

Figure 3.10 shows the maximum boosting strategy explained in [28] as an alternative to the simple boosting method. It is quite similar to the traditional carrier-based PWM control method. This control method maintains the six active states unchanged and turns all zero states into shoot-through states. Thus maximum boosting factor (B) is obtained for any given modulation index without distorting the output waveform. As can be seen from Figure 3.10, the circuit is in the shoot through state when the triangular carrier wave is either greater than the maximum curve of the references (V_a, V_b and V_c) or smaller than the minimum of the references. The voltage stress for the maximum boosting method is derived in [28] as

$$V_s = BV_g = (\frac{3\sqrt{3}G}{\pi} - 1)V_g \tag{3.13}$$

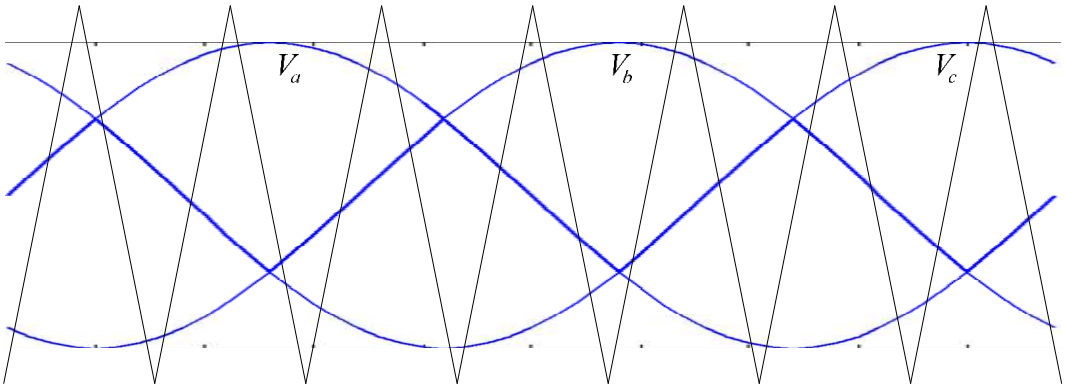


Figure 3.10 Maximum boosting PWM generation waveforms of the ZSC

The voltage stress versus the voltage gain for maximum boosting method is shown in Figure 3.11. Compared with the simple control method, shown in Figure 3.9, the voltage stress in maximum boosting method is much lower, which means that the inverter can be operated to obtain a higher voltage gain.

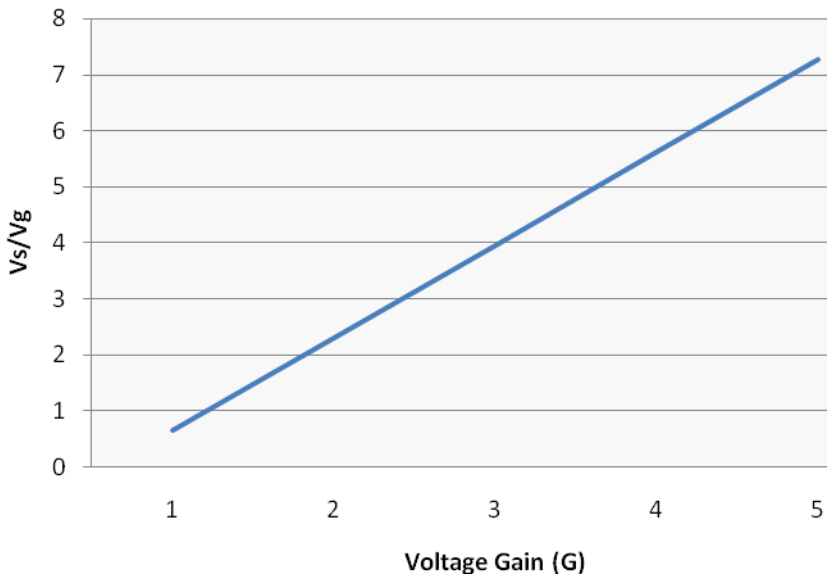


Figure 3.11 Switch voltage stress versus voltage gain in maximum boosting method

The maximum boosting method can achieve the minimum voltage stress across the switches. However, it has the drawbacks of low-frequency ripples on the Z-source network, which is shown in [29]. Another boosting method proposed to achieve maximum possible voltage boost/gain while maintaining a constant boost viewed from the Z-source network and producing no low-frequency ripples associated with the output frequency is explained in [29].

Figure 3.12 shows the sketch map of the constant boosting method proposed in [29], which achieves the maximum voltage gain while always keeping the shoot-through duty ratio constant. There are five modulation curves in this control method: three reference signals (V_a,V_b and V_c), and two shoot-through envelope signals (V_P and V_N). When the carrier triangle wave is higher than the upper shoot-through envelope V_P or lower than the bottom shoot-through envelope V_N, the inverter is turned to a shoot-through zero state. In between, the inverter switches in the same way as in the traditional carrier based PWM control.

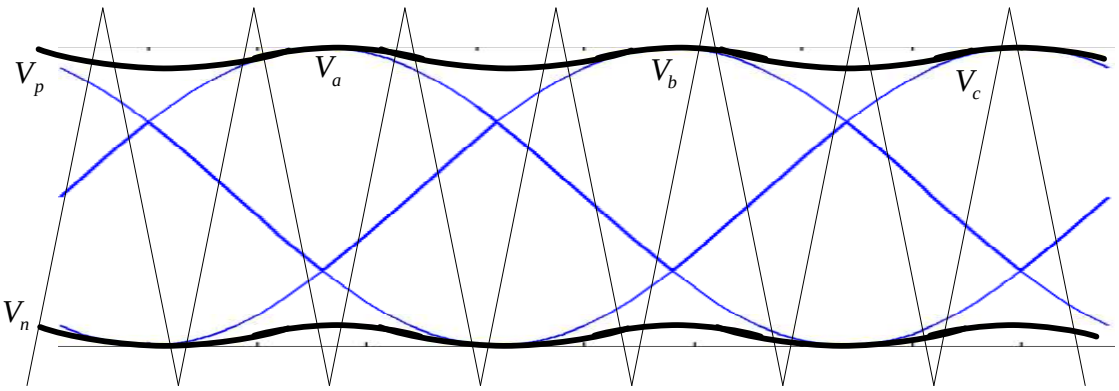


Figure 3.12 Constant boosting PWM generation waveforms of the ZSC

For the first half-period, [0, π/3] in Figure 3.12, the upper and lower envelope curves can be expressed by (3.14) and (3.15), respectively.

$$V_{P1} = \sqrt{3}M + \sin(\theta - \frac{2\pi}{3})M \qquad for\, 0 < \theta < \frac{\pi}{3} \tag{3.14}$$

$$V_{N1} = \sin(\theta - \frac{2\pi}{3})M \qquad for\, 0 < \theta < \frac{\pi}{3} \tag{3.15}$$

For the second half-period [π/3, 2π/3], the envelope curves are expressed by (3.16) and (3.17), respectively.

$$V_{P2} = \sin(\theta)M \qquad for\, \frac{\pi}{3} < \theta < \frac{2\pi}{3} \tag{3.16}$$

$$V_{N2} = \sin(\theta)M - \sqrt{3}M \qquad for\, \frac{\pi}{3} < \theta < \frac{2\pi}{3} \tag{3.17}$$

The voltage stress for the constant boosting method was derived in [29] as

$$V_s = BV_g = (\sqrt{3}G - 1)V_g \tag{3.18}$$

As can be seen from Figure 3.13, the constant boosting method has a much lower voltage stress across the devices than the simple boosting method, while having a slightly higher voltage stress than the maximum boosting method. The ideal voltage-stress ratio is one. The constant boosting method is highly desirable for applications requiring a voltage gain of two to three. Also the constant boosting method requires the minimum inductance and capacitance because the inductor current and the capacitor voltage contain no low-

frequency ripples associated with the output voltage, thus reducing the cost, volume, and weight of the Z-source network [29].

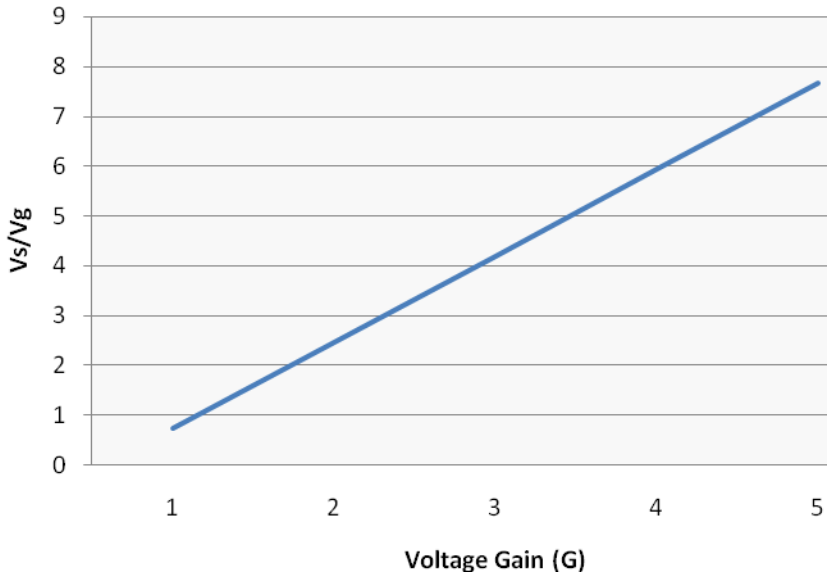


Figure 3.13 Switch voltage stress versus voltage gain in constant boosting method

3.5 Comparison of Traditional Inverters and ZSI

So far applications requiring conversion employed either traditional PWM inverters if the available input DC voltage is high enough or DC/DC boosted PWM inverters if the DC voltage is to be increased before the inversion process. Figure 3.14 shows the traditional and DC/DC boosted PWM inverters. Z-source inverter can replace both of these inverters in most of the applications. Also it has been shown in the literature that the Z-source inverter gave good results when compared to the traditional PWM inverters [30-31]. In [31], for purposes of comparison, an example of the total switching device power (SDP), the requirement of passive components, the constant power speed

ratio (CPSR), and the efficiencies of different inverter topologies for a fuel cell vehicle cell are given.

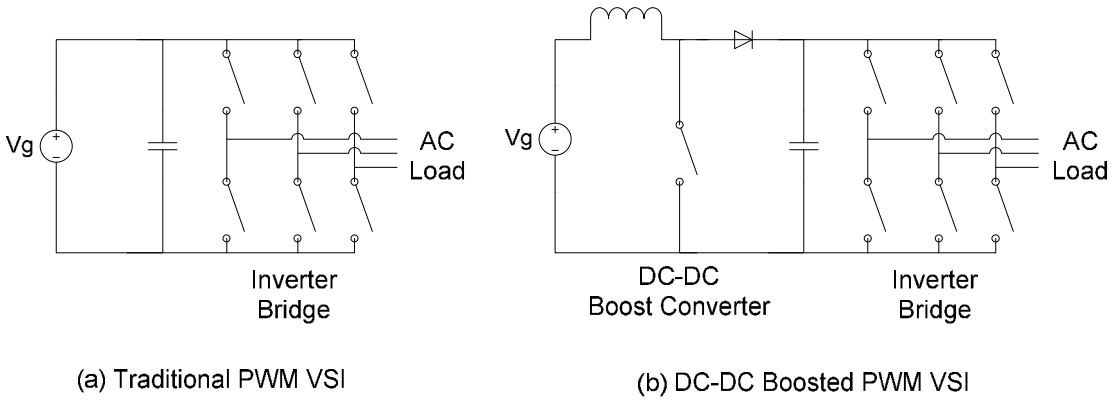


Figure 3.14 Commonly used PWM inverters

In the traditional PWM inverter, the DC bus voltage, which is also the output voltage of the fuel cell stack, varies with the load. The modulation index has to be controlled to achieve the required output voltage. The boost converter in the DC/DC boosted PWM inverter system boosts the DC voltage only when the required output voltage is higher than the fuel cell voltage. The Z-source inverter outputs a required voltage by adjusting the shoot through duty ratio with the restriction to keep the voltage across the switches not to exceed the limits [29].

The fuel cell vehicle example in [31] is one of the many applications that the traditional inverters and the Z-source inverter can be compared. Table 3.2 shows the SDP comparison of the three inverters. The Z-source inverter's average SDP is the lowest among the three, while the conventional PWM inverter's SDPs are the highest in both average and peak values. Usually, the selection of the switching device is based on the

RMS/average current rating, and also the average SDP is a measurement of thermal requirement.

Table 3.2 Switching device power comparison

Inverters	Total average SDP (kVA)	Total peak SDP (kVA)
Traditional PWM Inverter	207	650
DC/DC Boosted Inverter	207	470
Z-source Inverter	191	577

Table 3.3 shows the passive component comparison with the requirements to limit the inductor current ripple to be less than 10% of its average value, and capacitor voltage ripple less than 3% of the maximum voltage, 420 V at a switching frequency of 10 kHz. The Z-source inverter's two inductors can be built on one core to minimize the size and weight. In general, the required L and C of the Z-source inverter are slightly greater than those of the DC/DC boosted PWM inverter [31].

CPSR is limited mainly by available DC voltage of the PWM inverter. The fuel cell voltage decreases as the current drawn increases, which greatly limits the motor's power output and efficiency at high speed. Since the Z-source inverter can increase the available DC voltage together with the DC/DC boosted PWM inverter, it can also increase the CPSR over the conventional PWM inverter significantly. Efficiency is an important criterion for any power converter. High efficiency can reduce thermal requirements and cost. Three inverters were also compared in [31], in terms of their efficiencies. Z-source inverter provided higher efficiencies in most operation ranges.

Table 3.3 Required passive components

Inverters	Number of Inductors	L (μH)	Avg. Inductor Current (A)	Number of Capacitors	C (μF)	Capacitor RMS Current (A)	Capacitor voltage rating (V)
Traditional PWM Inverter	0	N/A	N/A	1	296	112	420
DC/DC Boosted Inverter	1	510	200	1	511	105	420
Z-source Inverter	2	339	200	2	428	110	420

It is also important to note that the comparison in [31] is a pure theoretical one. In practical cases, for DC/DC boosted PWM inverter, the associated cost and volume increase of extra heat sinking effort and gate drive for an extra switch are also significant. Also, great reliability enhancement of the Z-source inverter is a very important advantage. In general, the Z-source inverter is very competitive in low boost ratio range (1 to 2). In cases when a low input voltage is available, and boost ratio much higher than two is needed, the DC/DC boosted PWM inverter is the best configuration.

In [32], a design procedure of the traditional double stage DC/DC boosted PWM inverter and a single stage Z-source inverter, as a single phase photo-voltaic (PV) grid connected transformer-less power conditioner is given. The performances of both topologies are investigated. The energy storage elements and the efficiency of the converters are compared.

The conventional topology of PV power conditioning units (PCUs) is a combination of a boost converter and a current controlled VSI. The DC/DC converter performs a maximum power point tracking to achieve the highest possible energy from the PV-arrays. The full-bridge single phase inverter should have balanced switching to avoid DC offsets. Also, a transformer-less PV-PCU needs some protections to avoid the injection of DC current in faulty conditions. At high loads the efficiency is almost the same for both inverters, but at low loads the efficiency of the Z-source inverter drops more rapidly. It is due to higher circulating power in Z-source network. Both inverters have acceptable performance as a grid-connected PV-PCU. The Z-source inverter has one switch less than the DC/DC boosted PWM inverter but the DC/DC boosted PWM inverter has better efficiency at low loads [32].

3.6 Power Conditioning Applications

Renewable energy includes solar energy (PV), wind energy, bio-fuel, geothermal energy, hydrogen and fuel cells. These energy sources are renewable and utilization of these energy sources creates zero or little emissions. Furthermore, distributed generation (DG) systems using renewable energy have great potential to increase the grid reliability [33]. For renewable energy systems, the main challenge is the output voltage variation of the energy source. The ability to boost and buck input voltage makes the Z-source inverter very attractive for these applications.

Compared with the traditional systems, the Z-source PCUs does not need a bulky transformer or a DC/DC converter to boost the voltage in the circuit. Usually a transformer-less inverter can gain 2-3% in conversion efficiency. The switch in the

DC/DC converter will make the efficiency lower and the cost higher. Thus for the Z-source inverter system, the size and cost are minimized. Because no dead time is needed, the control accuracy and harmonics can also be improved. The Z-source inverter can have the minimum KVA requirement to meet the need of 1:2 output voltage ranges for most renewable energy sources [33].

A fuel cell is an electrochemical device that converts chemical energy directly into electric energy by reaction of hydrogen from the fuel and oxygen from the air. Figure 3.15 shows a fuel cell power utility system. The fuel cells produce water and heat by combining hydrogen with oxygen, and have 50% efficiency for only electricity but could reach 85% in the case of combined heat and power (CHP). Also, the fuel cells can be used for various applications such as stationary sites (buildings, hospitals, domestic utility, etc.), transportation (fuel cell vehicle), portable power (laptop, cell phone), and distributed power [37].

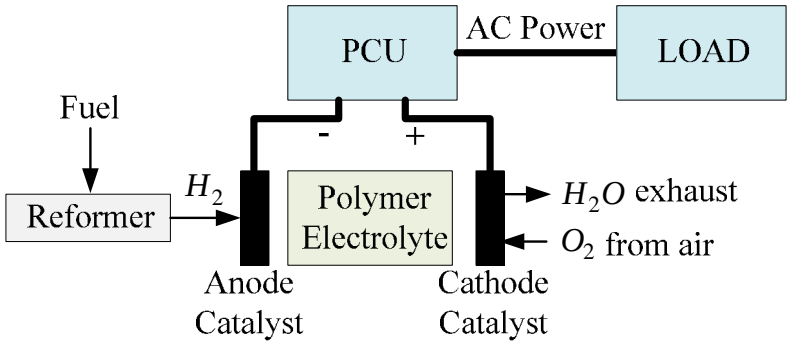


Figure 3.15 Configuration of a fuel cell system

The fuel cell voltage (and power) is determined by two main factors. First, the rate at which hydrogen flows through the fuel cell establishes the level of the V-I

polarization curve [33]. Second, the amount of current drawn by the inverter determines the point on this curve where the fuel cell will operate. Thus, by controlling the amount of current drawn by the inverter, the fuel cell voltage and power can be controlled [37].

Recently Z-source inverter has been applied to power conditioning of fuel cell based energy systems [16], [34-37]. In [34], a detailed design process of the Z-source inverter for fuel cell vehicles is provided. A DC rail clamp circuit is presented which helps in reducing the voltage overshoot. Also a thermal design is provided and a 3-D design method is reviewed.

[35] and [36] presents a Z-source inverter control strategy used to control the power flow from a fuel cell system to a motor and a battery for traction drive of fuel cell-battery hybrid vehicles. A new concept is revealed that substitutes a high voltage battery for one (or both) of the capacitors from the Z-source network which is shown in Figure 3.16. Figure 3.17 shows the power flow diagram of the traction drive system. In this application, Z-source inverter eliminates the need for a DC/DC boost converter.

Another comprehensive discussion of Z-source inverter as a PCU for the fuel cell systems is given in [16], which presents system modeling, modified space vector PWM implementation (MSVPWM), and control system design of a ZSC for fuel cells. The fuel cell based power generation system in [16] using the Z-source inverter is given in Figure 3.18. Here the fuel cell system is modeled by an *R-C* circuit including its voltage-current polarization characteristics. A discrete-time state space equation is given to implement digital control and a space vector pulse-width modulation technique is modified to realize the shoot-through vectors that boost the dc-link voltage.

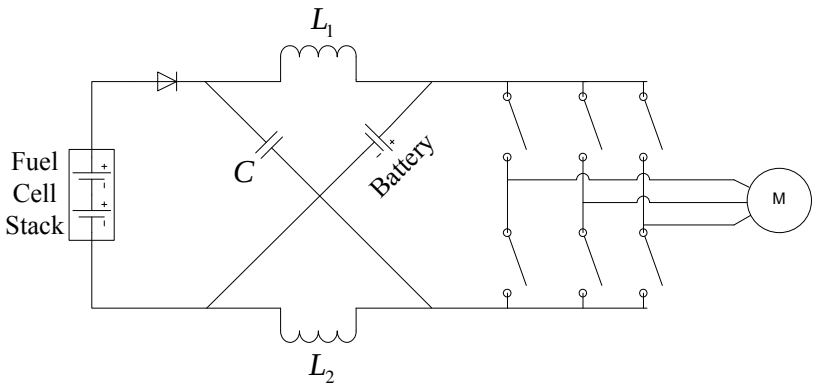


Figure 3.16 Fuel cell-battery hybrid vehicle system using Z-source inverter

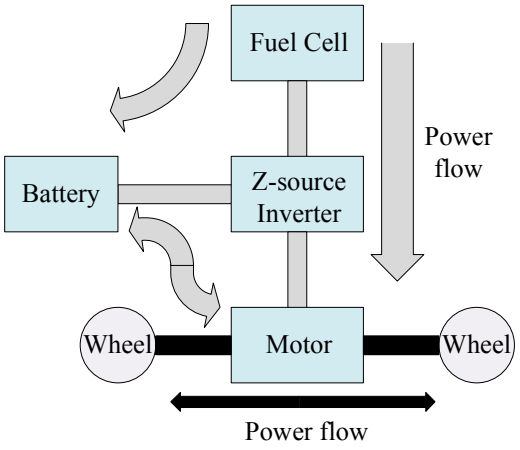


Figure 3.17 Block diagram of fuel cell based traction drive system

Z-source inverter based fuel cell PCU is shown in Figure 3.18. The fuel processor controls the reformer to produce hydrogen for power requested from the PWM inverter DSP controller. The controller monitors the stack current and voltage for proper operation of the fuel cell. The DSP controller communicates with the fuel cell processor to balance the power available from the stack with the power requested by the load, controls the ZSI, and senses output voltages and currents for a closed-loop control [16].

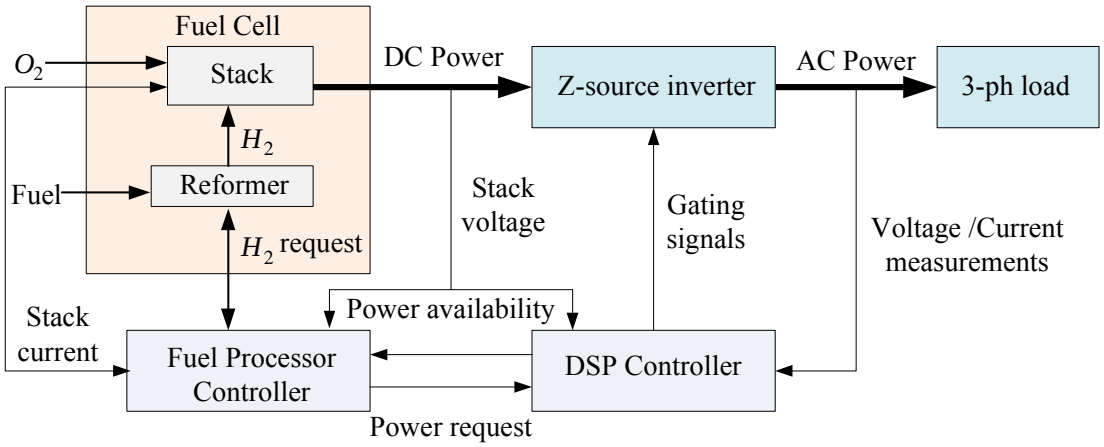


Figure 3.18 Fuel cell based power generation using Z-source inverter

3.7 Summary

This chapter is a review of the literature on the ZSC. First, a brief introduction, which discusses the basic properties of the ZSC is given. Then, the steady state relations are derived and voltage conversion ratio is given based on the simplified circuit of the ZSC. Next, a modified modulation technique given in the literature is summarized where the shoot-through states are distributed among the VSI PWM modulation pattern such that the active states are kept the same. Following that, three different boosting methods of the dc-link voltage are discussed where different results are shown in terms of the voltage stress and the maximum boosting that can be obtained. Then, the ZSC as an inverter is compared to the traditional inverters. Finally, power conditioning and utility interface applications of the Z-source inverter are discussed. It is concluded that the fuel cell applications are very suitable for this topology.

CHAPTER IV

DYNAMIC MODELING OF THE Z-SOURCE CONVERTER

4.1 Power Converter Modeling

Power converters require feedback control in order to keep the desired output voltage (current) values. This can be achieved through a controller circuit that can vary the converter control input such that the output voltage (current) is regulated around a reference value. The feedback control system composed of the power converter and the control circuit should be stable and the converter transient parameters such as percentage overshoot, settling time and steady state error should meet specifications. The design of such a control circuit requires an accurate dynamic model of the converter. This model should give an idea of how the output voltage of the converter is affected by the changes in the input voltage, the load current, or the duty cycle [2].

Modeling is the representation of a physical system using mathematical tools. In general, engineering models include significant system behaviors while neglecting the second order effects. This simplified system model gives a physical insight into the system dynamics and helps in designing a proper controller. Accuracy and complexity of the model are inversely related and depend on the level of the assumptions made. So far

different modeling techniques as well as various models with different levels of accuracy and complexity are used for power converters [1]-[2], [17]-[19]. The use of a model depends on the system design stage. For example, a model which gives good results for the computer simulation of the converter may not be a good choice for closed loop controller design [1].

For power converters, obtaining simplified models requires making assumptions and approximations. For instance, a capacitor shows parasitic resistive and inductive behaviors together with its capacitive behavior especially at high frequencies. These parasitic effects can be approximated by an Equivalent Series Resistance (ESR) and an Equivalent Series Inductance (ESL). However, some converter models use neither an ESR nor an ESL, but just model the capacitor as ideal. Such a model will help in calculations, but will not be able to guess any dynamics caused by the ESR or the ESL.

A common assumption in modeling of power converters is ignoring the switching ripple. Since power converters are high frequency switching circuits, in a well-designed converter operating in Continuous Conduction Mode (CCM), the switching ripple is low and the switching frequency is much higher than the natural frequencies of the converter filtering elements. Hence, a possible simplification of a power converter model could be ignoring the switching ripple and averaging the circuit waveforms over the switching period. Figure 4.1(a) shows both the actual and the averaged waveforms of a typical converter output waveform and Figure 4.1(b) shows the spectrum of this output waveform. For a well-designed converter, the high frequency components of the spectrum are small in magnitude compared to the low frequency components if the

switching ripple is small. Neglecting the switching ripple will keep the low frequency component of the waveform.

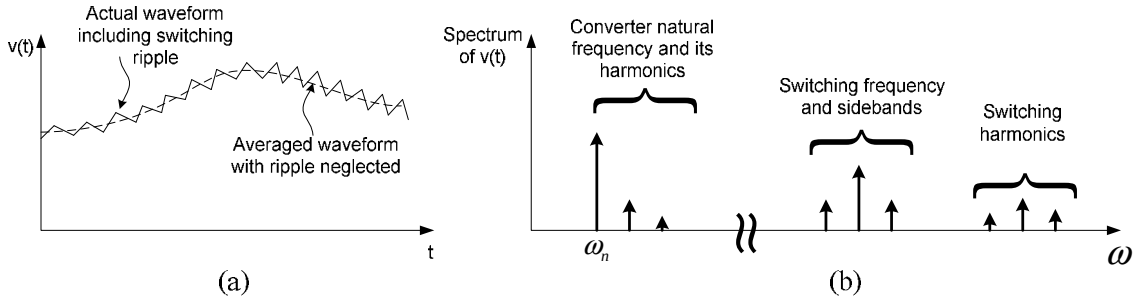


Figure 4.1 (a) A typical converter output waveform (b) spectrum of the output waveform

There are different modeling methods used in power electronics. Among those are circuit averaging method [17] and the state space averaging method [20-21]. Although the form of the end result is different for each method, they lead to the same model when ideal elements are considered [2]. In this chapter a small signal model for the ZSC will be derived based on the state space averaging technique and linearization of the state variables around their steady state values. The validity of the model is verified by comparing the simulation results for the dynamics of the switching converter with the converter state space averaged model.

4.2 State Space Averaging

State space modeling approach is commonly used in modeling of power converters [1-2], [20-21]. The state space description is a canonical form for writing the differential equations that describe a system. For a linear network, the derivatives of the state variables are expressed as linear combinations of the system independent inputs and

the state variables themselves. The physical state variables of a system are usually associated with the storage of energy, and for a typical converter circuit, the physical state variables are the independent inductor currents and capacitor voltages. At any given point in time the value of the state variables depend on the previous history of the system. To solve the differential equations of the system, the initial values of the state variables should be specified. In other words, if we know the state of a system, that is the values of all the state variables, at a given time t_o, and if we know the system inputs for $t \geq t_o$, then we can solve the system state equations to find the system waveforms at any future time. The state equations of a system can be written in the compact matrix form of Eq. (4.1):

$$\begin{aligned} K\frac{dx(t)}{dt} &= Ax(t) + Bu(t) \\ y(t) &= Cx(t) + Eu(t) \end{aligned} \tag{4.1}$$

Here, the state vector $x(t)$ is a vector containing all of the state variables, that is, the inductor currents and capacitor voltages. The input vector $u(t)$ contains the independent inputs to the system, such as the input voltage source. K is a matrix containing the values of capacitance and inductance, such that $Kdx(t)/dt$ is a vector containing the inductor voltages and capacitor currents in a power converter. Eq. (4.1) states that the inductor voltages and capacitor currents in a circuit can be expressed as linear combinations of the state variables and the independent inputs. The matrices A and B contain constants of proportionality [2].

It may also be desired to compute other circuit waveforms that do not coincide with the elements of the state vector $x(t)$ or the input vector $u(t)$. These are dependent

waveforms that can be expressed as linear combinations of the elements of the state vector and the input vector. They are combined in a vector $y(t)$, which is called the output vector. The matrices C and E contain constants of proportionality [2].

In Chapter II, basic DC/DC converter topologies such as buck and boost converters were discussed. Assuming continuous conduction mode (CCM), it was mentioned that, there are two subintervals for a power converter during a switching period. During each subinterval the converter reduces to a linear circuit. During the first subinterval, the converter can be expressed by the following state equations:

$$\left.\begin{aligned} K\frac{dx(t)}{dt} &= A_1 x(t) + B_1 u(t) \\ y(t) &= C_1 x(t) + E_1 u(t) \end{aligned}\right\} \qquad 0 \le t \le dT \tag{4.2}$$

Similarly, during the second subinterval, the converter can be expressed by the following state equations:

$$\left.\begin{aligned} K\frac{dx(t)}{dt} &= A_2 x(t) + B_2 u(t) \\ y(t) &= C_2 x(t) + E_2 u(t) \end{aligned}\right\} \qquad dT \le t \le T \tag{4.3}$$

Eqs. (4.2) and (4.3) constitute the state space model of the power converter. Using the state space model, the converter can be averaged over the switching cycle provided that the natural frequencies of the converter are much slower than the switching frequency. This is called the state space averaging and the results of it are the state space equations of the equilibrium (or steady state) and the AC small signal model [2]. The state space averaged model that describes the converter in equilibrium is

$$
\begin{aligned}
0 &= AX + BU \\
Y &= CX + EU
\end{aligned}
\tag{4.4}
$$

where the averaged matrices are

$$
\begin{aligned}
A &= DA_1 + D'A_2 \\
B &= DB_1 + D'B_2 \\
C &= DC_1 + D'C_2 \\
E &= DE_1 + D'E_2
\end{aligned}
\tag{4.5}
$$

The equilibrium DC components are

$$
\begin{aligned}
X &= equilibrium\,(dc)\,state\,vector \\
U &= equilibrium\,(dc)\,input\,vector \\
Y &= equilibrium\,(dc)\,output\,vector \\
D &= equilibrium\,(dc)\,duty\,cycle \\
D' &= 1 - D
\end{aligned}
\tag{4.6}
$$

Eq. (4.4) can be solved to find the equilibrium state and output vectors:

$$
\begin{aligned}
X &= -A^{-1}BU \\
Y &= \left(-CA^{-1}B + E\right)U
\end{aligned}
\tag{4.7}
$$

The state equations of the small signal AC model are

$$
\begin{aligned}
K\frac{d\hat{x}(t)}{dt} &= A\hat{x}(t) + B\hat{u}(t) + \left\{\left(A_1 - A_2\right)X + \left(B_1 - B_2\right)U\right\}\hat{d}(t) \\
\hat{y}(t) &= C\hat{x}(t) + E\hat{u}(t) + \left\{\left(C_1 - C_2\right)X + \left(E_1 - E_2\right)U\right\}\hat{d}(t)
\end{aligned}
\tag{4.8}
$$

where the quantities $\hat{x}(t), \hat{u}(t), \hat{y}(t)$, and $\hat{d}(t)$ in Eq. (4.8) are small AC variations around the equilibrium solution, or quiescent operating point defined by Eqs. (4.4) to (4.7) .

This section summarized the theoretical basis of modeling a power converter using state space averaging method. This method is well defined in the literature [2], [20-21]. So if we can write the converter state equations, i.e. Eqs. (4.2) and (4.3), then we can find the averaged DC and small signal AC models, by evaluation of Eqs. (4.4) to (4.7).

4.3 Small Signal Modeling of the ZSC

In Chapter III, the Z-source inverter was simplified to the circuit in Figure 3.3 (repeated in Figure 4.2(a)). The two switching states of the circuit in Figure 3.3 were given in Figure 3.4 (Figure 4.2(b)) and Figure 3.5(Figure 4.2(c)), where they were called "shoot-through" and "active" states, respectively. Active state is when the energy transfer occurs from the DC source as well as the Z-source inductors to the load. Shoot-through state is when the load and source sides are decoupled and the Z-source inductors are charged by the Z-source capacitors. The duty ratio d of switch S_2 is defined as the shoot-through duty ratio.

In this section, the state space model of the ZSC will be derived using the procedure explained in the previous section. This derivation is based on the assumptions of CCM operation and ideal lossless components [8]. It was also shown in [5] and [8] that if $L_1 = L_2 = L$ and $C_1 = C_2 = C$, the Z-source network is symmetrical and then $v_{C1}(t) = v_{C2}(t) = v_C(t)$ and $i_{L1}(t) = i_{L2}(t) = i_L(t)$.

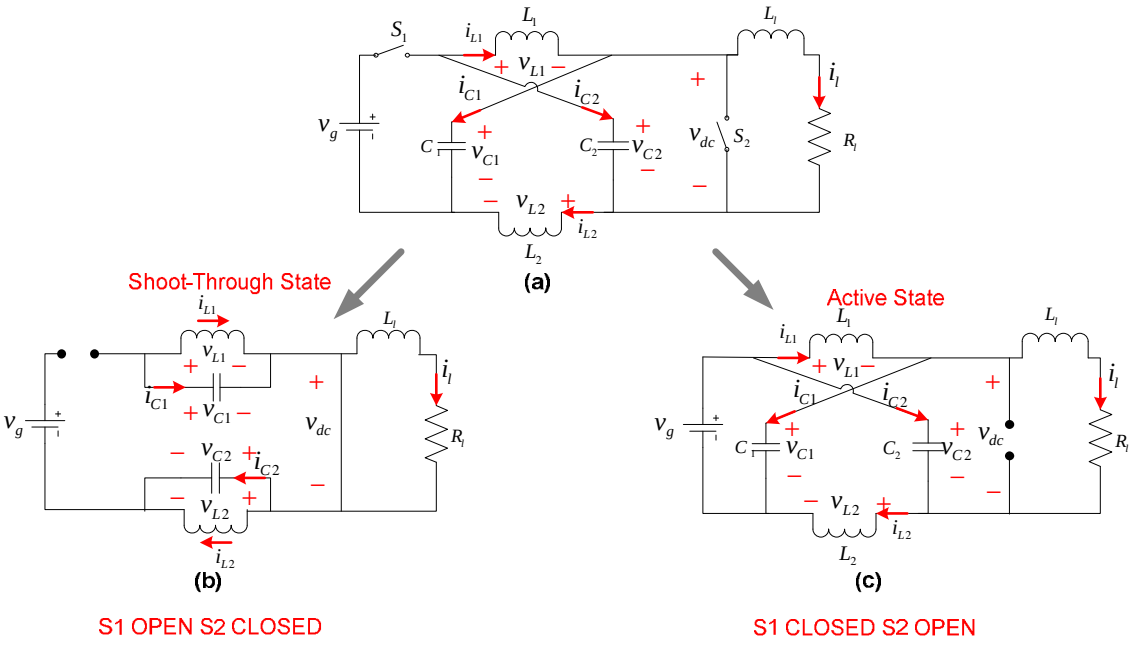


Figure 4.2 (a) Simplified circuit of the ZSC (b) shoot-through state (c) active state

The state variables of the ZSC are selected as the inductor current, the capacitor voltage and the load current (considering an inductive loading). These state variables can be defined as a vector in the form of

$$x(t) = [i_L(t) \quad v_C(t) \quad i_l(t)]^T \tag{4.9}$$

The state space representation during the shoot-through state in Figure 4.2(b) can be written in state space form $K\dot{x} = A_1 x + B_1 u$ given in Eq.(4.2) which is:

$$\begin{bmatrix} L_1 & 0 & 0 \\ 0 & C_1 & 0 \\ 0 & 0 & L_l \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_{L1}(t) \\ v_{C1}(t) \\ i_{Ll}(t) \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ -1 & 0 & 0 \\ 0 & 0 & -R_l \end{bmatrix} \begin{bmatrix} i_{L1}(t) \\ v_{C1}(t) \\ i_{Ll}(t) \end{bmatrix} \tag{4.10}$$

where, $K = \begin{bmatrix} L & 0 & 0 \\ 0 & C & 0 \\ 0 & 0 & L_l \end{bmatrix}$, $A_1 = \begin{bmatrix} 0 & 1 & 0 \\ -1 & 0 & 0 \\ 0 & 0 & -R_l \end{bmatrix}$ and $B_1 = \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix}$

Similarly, the state space representation during the active state in Figure 4.2(c) can be written in the form $K\dot{x} = A_2 x + B_2 u$ given in Eq.(4.2) or in open form,

$$\begin{bmatrix} \mathrm{L} & 0 & 0 \\ 0 & C & 0 \\ 0 & 0 & L_l \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_L(t) \\ v_C(t) \\ i_{L_l}(t) \end{bmatrix} = \begin{bmatrix} 0 & -1 & 0 \\ 1 & 0 & -1 \\ 0 & 1 & -R_l \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_C(t) \\ i_{L_l}(t) \end{bmatrix} + \begin{bmatrix} 1 \\ 0 \\ -1 \end{bmatrix} V_g \tag{4.11}$$

where, $A_2 = \begin{bmatrix} 0 & -1 & 0 \\ 1 & 0 & -1 \\ 0 & 1 & -R_l \end{bmatrix}$ and $B_2 = \begin{bmatrix} 1 \\ 0 \\ -1 \end{bmatrix}$

Equations (4.10) and (4.11) constitute the state space model of the simplified ZSC and they give the relations between the input and the state variables for both the shoot-through and the active states given in Figure 4.2(b) and Figure 4.2(c), respectively . As explained in the previous section, the state space model of the ZSC can be used for state space averaging and to find the state space equations of the equilibrium and the AC small signal [2], [20-21]. Eq. (4.12) gives the state space averaged model that describes the ZSC in equilibrium based on Eqs. (4.4) and (4.5).

$$\begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} 0 & D-D' & 0 \\ D'-D & 0 & -D' \\ 0 & D' & -R_l \end{bmatrix} \begin{bmatrix} I_L \\ V_C \\ I_l \end{bmatrix} + \begin{bmatrix} D' \\ 0 \\ -D' \end{bmatrix} V_g \tag{4.12}$$

Eq. (4.12) can be solved to find the equilibrium state vector. So the equilibrium values of the state variables can be found based on Eq. (4.7) as

$$V_C = \frac{D'}{D'-D} V_g \tag{4.13}$$

$$I_L = \frac{D'}{D'-D} I_l \tag{4.14}$$

$$I_l = \frac{V_c}{R_l} \tag{4.15}$$

In order to determine the dynamic behavior of the state variables, the input voltage and the shoot-through duty cycle will be perturbed around their steady state values and written as $v_g(t) = V_g + \hat{v}_g(t)$ and $d(t) = D + \hat{d}(t)$, where V_g and D are the steady state values, $\hat{v}_g$ and $\hat{d}$ are the perturbed values of the input voltage and the duty cycle, respectively. The resulting small signal perturbations in state variables will be represented as $x(t) = X + \hat{x}(t)$, where x represents the state variables defined in Eq. (4.9) and X represents the equilibrium values of the state variables in Eqs. (4.13), (4.14) and (4.15). The state equations of the small signal AC model can be found after linearizing the averaged model and subtracting the equilibrium values of the state variables. Using Eqs. (4.10) and (4.11) and based on Eq.(4.8), the state equations of the small signal AC model of the ZSC can be written in open form

$$\begin{aligned}
sL\hat{i}_L(s) &= (D-D')\hat{v}_C(s) + D'\hat{v}_g(s) + (2V_C - V_g)\hat{d}(s) \\
sC\hat{v}_C(s) &= (D'-D)\hat{i}_L(s) + (-2I_L + I_l)\hat{d}(s) - D'\hat{i}_l(s) \\
sL_l\hat{i}_l(s) &= 2D'\hat{v}_C(s) - D'\hat{v}_g(s) + (-2V_C + V_g)\hat{d}(s) - R_l\hat{i}_l(s)
\end{aligned} \tag{4.16}$$

Having the small signal equations and the steady state equations, we can construct the small signal circuit and derive the transfer functions. Three equivalent circuits are given in Figure 4.3 based on the three equations in Eq. (4.16). Each circuit has independent sources and sources whose values depend on voltages or currents elsewhere in the ZSC. For instance terms containing $\hat{d}(t)$ are represented as independent sources and terms containing $\hat{v}_C(t)$, $\hat{i}_L(t)$, $\hat{i}_l(t)$ or $\hat{v}_g(t)$ are dependent sources. Figure 4.3(a) shows a sub-circuit for the inductor current equation in Eq. (4.16). Similarly, Figure 4.3(b) and Figure 4.3(c) show the sub-circuits representing the capacitor voltage and load current small signal equations in Eq. (4.16), all of which are the state variables of the ZSC [8].

At the beginning of the small signal analysis, two sources of perturbations were identified, namely the shoot-through duty cycle ($\hat{d}(t)$) and the input voltage perturbations ($\hat{v}_g(t)$). It is known that the perturbation in a state variable can be expressed as the linear combination of all sources of small signal perturbations [2]. Hence the capacitor voltage small signal expression is,

$$\hat{v}_C(s) = G_{vg}(s)\hat{v}_g(s) + G_{vd}(s)\hat{d}(s) \tag{4.17}$$

and the inductor current small signal expression is,

$$\hat{i}_L(s) = G_{ig}(s)\hat{v}_g(s) + G_{id}(s)\hat{d}(s) \tag{4.18}$$

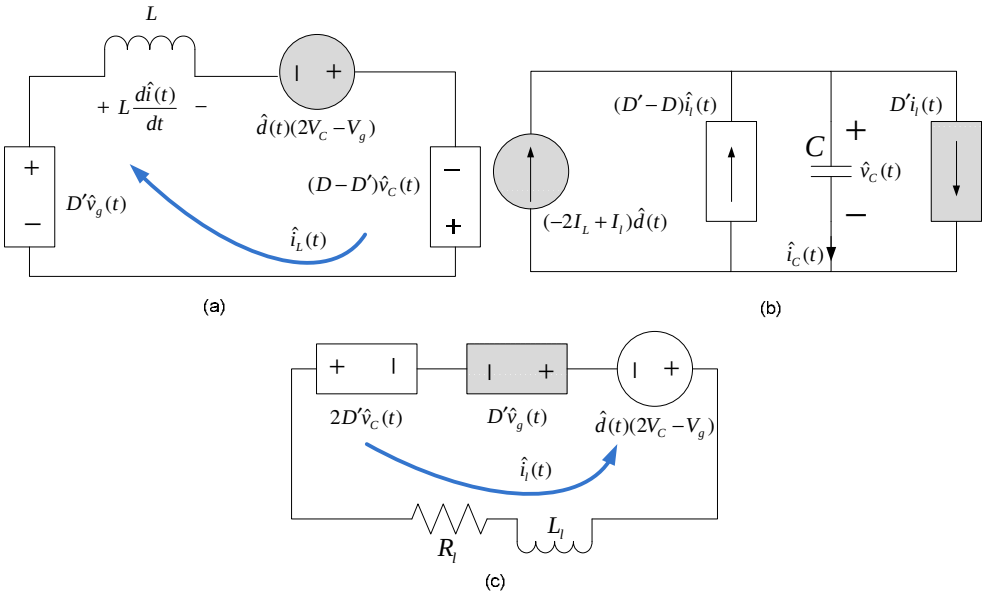


Figure 4.3 Small signal circuit of ZSC with inductive loading

where $G_{vg}(s)$ is the input-to-capacitor voltage transfer function given in Eq. (4.19) and $G_{vd}(s)$ is the control-to-capacitor voltage transfer function given in Eq. (4.20). Also $G_{ig}(s)$ is the input-to-inductor current transfer function shown in Eq. (4.21) and $G_{id}(s)$ is the control-to-inductor current transfer function shown in Eq. (4.22). Eqs. (4.19)-(4.22) represent the dynamic behavior of the ZSC in case of a small change in each source of perturbation.

$$G_{vg}(s) = \frac{\hat{v}_c(s)}{\hat{v}_g(s)}\bigg|_{\hat{d}(s)=0} = \frac{[D'(D'-D)L_l + D'^2 L]s + D'(D'-D)R_l}{L_l LCs^3 + R_l LCs^2 + [2D'^2 L + L_l(D-D')^2]s + R_l(D-D')^2} \quad (4.19)$$

$$G_{vd}(s) = \left.\frac{\hat{v}_c(s)}{\hat{d}(s)}\right|_{\hat{v}_g(s)=0}$$

$$= \frac{(-2I_L + I_l)L_l L s^2 + [(-2I_L + I_l)R_l L + (D' - D)(2V_c - V_g)L_l + LD'(2V_c - V_g)]s + (D' - D)(2V_c - V_g)R_l}{L_l LCs^3 + R_l LCs^2 + [2D'^2 L + L_l(D - D')^2]s + R_l(D - D')^2}$$

(4.20)

$$G_{ig}(s) = \left.\frac{\hat{i}_L(s)}{\hat{v}_g(s)}\right|_{\hat{d}(s)=0} = \frac{D'L_l LCs^2 + D'R_l LCs + D'^2 L}{L_l LCs^3 + R_l LCs^2 + [2D'^2 L + L_l(D - D')^2]s + R_l(D - D')^2} \quad (4.21)$$

$$G_{id}(s) = \left.\frac{\hat{i}_L(s)}{\hat{d}(s)}\right|_{\hat{v}_g(s)=0}$$

$$= \frac{(2V_c - V_g)L_l Cs^2 + [(2V_c - V_g)R_l C + (D - D')(-2I_L + I_l).L_l]s + D'(2V_c - V_g) + (-2I_L + I_l).R_l(D - D')}{L_l LCs^3 + R_l LCs^2 + [2D'^2 L + L_l(D - D')^2]s + R_l(D - D')^2}$$

(4.22)

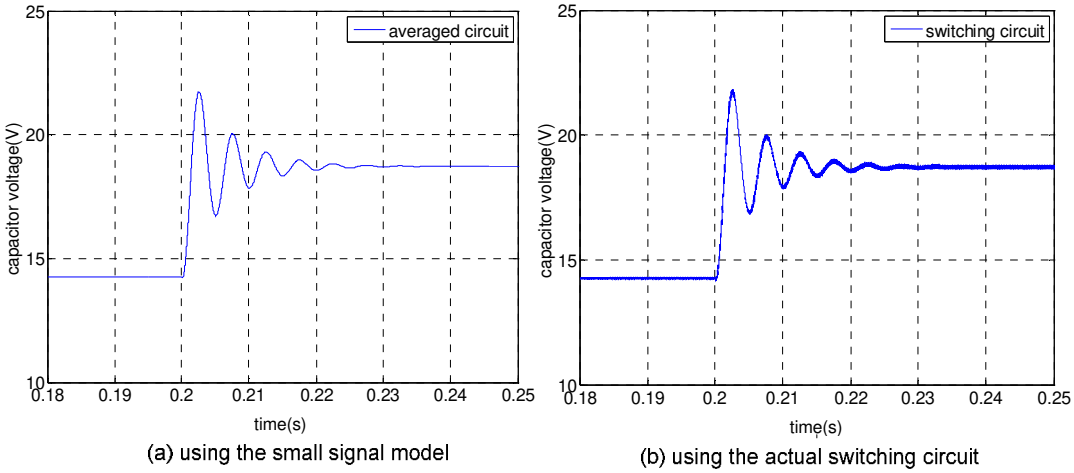
4.4 Model Verification

The effectiveness of the small signal model derived in the previous section can be verified by simulating and comparing the dynamics of the small signal circuit in Figure 4.3 with the dynamics of the actual switching circuit in Figure 4.2(a). The circuit parameters given in Table 4.1 are used as in [8] for verification purposes. Two cases are examined in the simulation and two state variables of the ZSC are compared, namely the capacitor voltage and the inductor current. Figure 4.4 and Figure 4.5 show the dynamics of the capacitor voltage and the inductor current waveforms obtained from both the averaged model and the switching circuit when there is a step increase of 10% in duty

cycle. Also Figure 4.6 and Figure 4.7 show the capacitor voltage and inductor current waveforms obtained from both averaged and switching circuits when there is a step increase of 8% in input voltage.

Table 4.1 Simulation parameters for model verification

Input Voltage, V_g	$12V$
Z-network inductance, L	$300\mu H$
Z-network capacitance, C	$360\mu F$
Load resistance, R_l	8.15Ω
Load inductance, L_l	$2mH$
Switching frequency, f_s	$20kHz$
Shoot-through duty cycle, D	0.2



(a) using the small signal model (b) using the actual switching circuit

Figure 4.4 Dynamics of the capacitor voltage due to a 10% step change in duty cycle

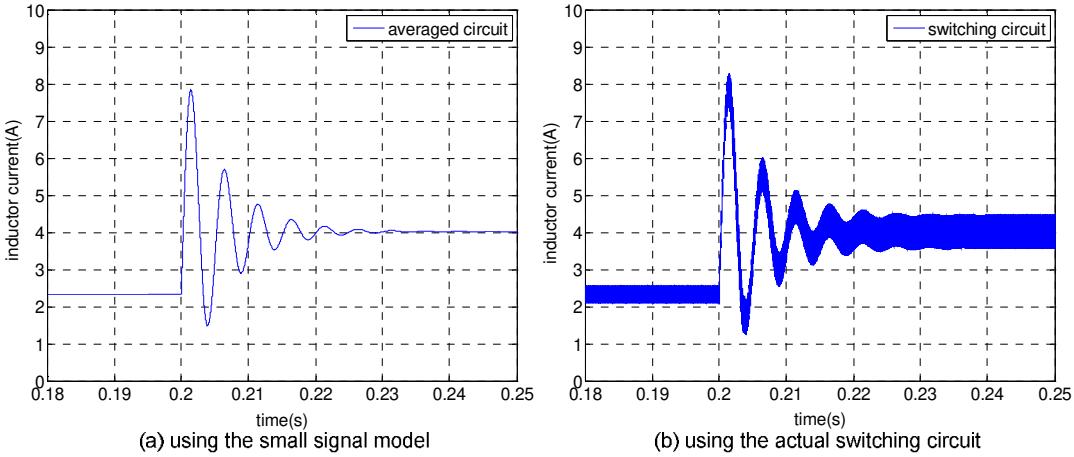


Figure 4.5 Dynamics of the inductor current due to a 10% step change in duty cycle

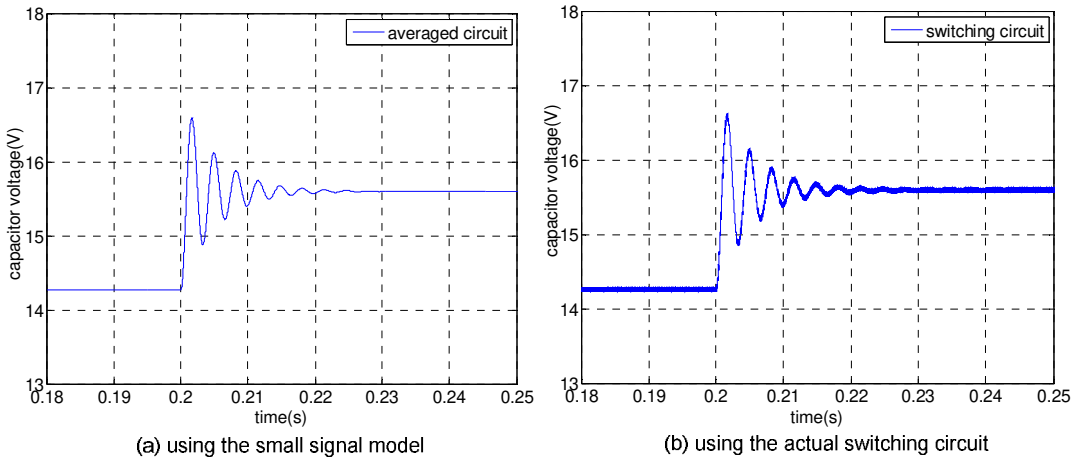


Figure 4.6 Dynamics of the capacitor voltage due to a 8% step change in input voltage

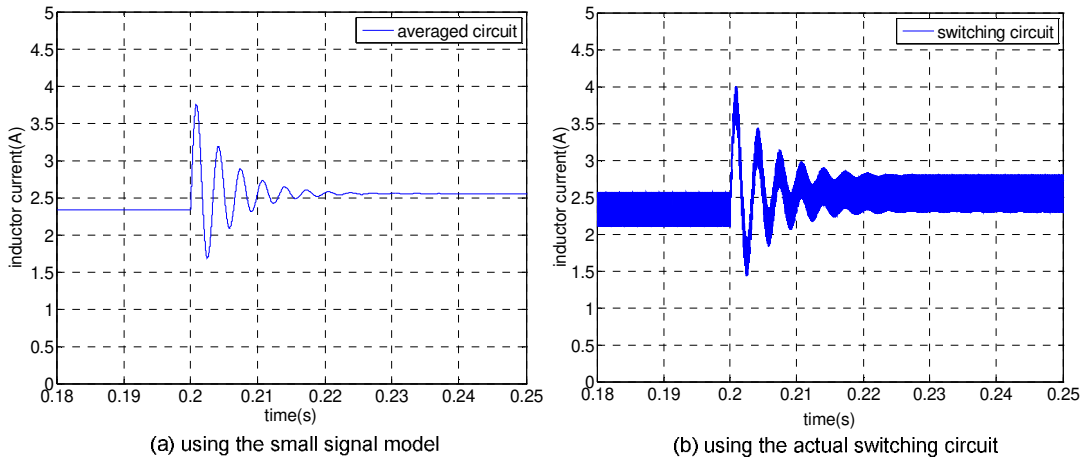


Figure 4.7 Dynamics of the inductor current due to a 8% step change in input voltage

Dynamics of both the averaged model and the switching circuit waveforms seen in Figure 4.4 through Figure 4.7 can be compared regarding to their step response parameters. Table 4.2 shows the approximate values of damped natural frequency (ω_d), peak time (t_p) and 2% settling time (t_s) obtained from the step responses in Figure 4.4 through Figure 4.7. For both cases of step changes in duty cycle and input voltage, waveforms from the averaged models show the same characteristics with their switching circuit counterparts. In all of the capacitor voltage and the inductor current waveform pairs, it can be observed that the averaged model waveforms and the switching circuit waveforms have the same ω_d, t_p and t_s. This shows that the model derived in the previous section is valid and the circuit in Figure 4.3 can be used as the small signal circuit of the simplified ZSC given in Figure 4.2(a).

Table 4.2 Obtained transient parameters from ZSC step responses

Transient parameters / Step responses	$\omega_d\ (rad/s)$	$t_p\ (ms)$	$t_s\ (ms)$
Figure 4.4(a) (averaged)	1256	2.5	~ 24
Figure 4.4(b) (switching)	1256	2.5	~ 24
Figure 4.5(a) (averaged)	1256	1.4	~ 24
Figure 4.5(b) (switching)	1256	1.4	~ 24
Figure 4.6(a) (averaged)	1852	1.6	~ 20
Figure 4.6(b) (switching)	1852	1.6	~ 20
Figure 4.7(a) (averaged)	1852	0.9	~ 20
Figure 4.7(b) (switching)	1852	0.9	~ 20

Transient parameters of the ZSC can be examined by comparing the transfer functions given in Eqs. (4.19)-(4.22) and the step responses given in Figure 4.4 through Figure 4.7. Table 4.3 shows the poles and zeros of the ZSC transfer functions when the parameters in Table 4.1 are used. For a transfer function representing the dynamic behavior of a system, each pole and zero has its own contribution to the transient response of that system. Poles and zeros in a transfer function have different effects to the transient behavior of a system depending on their positions on the pole-zero axis. Normally the transient behavior of a second order system is well defined if its transfer function can be obtained in the form of

$$\frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{4.23}$$

where ω_n is the undamped natural frequency and ζ is the damping ratio [22]. The characteristic equation is: $s^2 + 2\zeta\omega_n s + \omega_n^2$. The roots of this characteristic equation will give the expressions for the system poles as

$$s_{1,2} = -\zeta\omega_n \pm j\omega_n\sqrt{1-\zeta^2} \tag{4.24}$$

The s-plane representation of the poles in Eq. (4.24) can be plotted as in Figure 4.8, where τ is the system time constant and σ is the damping coefficient [23]. Based on Figure 4.8, critical transient parameters of a second order system can be derived as

$$t_p = \frac{\pi}{\omega_d} \tag{4.25}$$

$$t_s = \frac{4}{\tau} = \frac{4}{\zeta\omega_n} \tag{4.26}$$

where t_p is the peak time, t_s is the $\%2$ settling time [23].

Table 4.3 Poles and zeros of ZSC transfer functions

$G_{vd}(s)=\frac{\hat{v}_c(s)}{\hat{d}(s)}$	$\frac{(s+3489)\ (s-7253)}{(s+3746)\ (s^2+328.6s+1611000)}$
$G_{id}(s)=\frac{\hat{i}_L(s)}{\hat{d}(s)}$	$\frac{(s+511.4)\ (s+3802)}{(s+3746)\ (s^2+328.6s+1611000)}$
$G_{vg}(s)=\frac{\hat{v}_c(s)}{\hat{v}_g(s)}$	$\frac{(s+3396)}{(s+3688)\ (s^2+387.2s+3683000)}$
$G_{ig}(s)=\frac{\hat{i}_L(s)}{\hat{v}_g(s)}$	$\frac{(s+293.9)\ (s+3781)}{(s+3688)\ (s^2+387.2s+3683000)}$

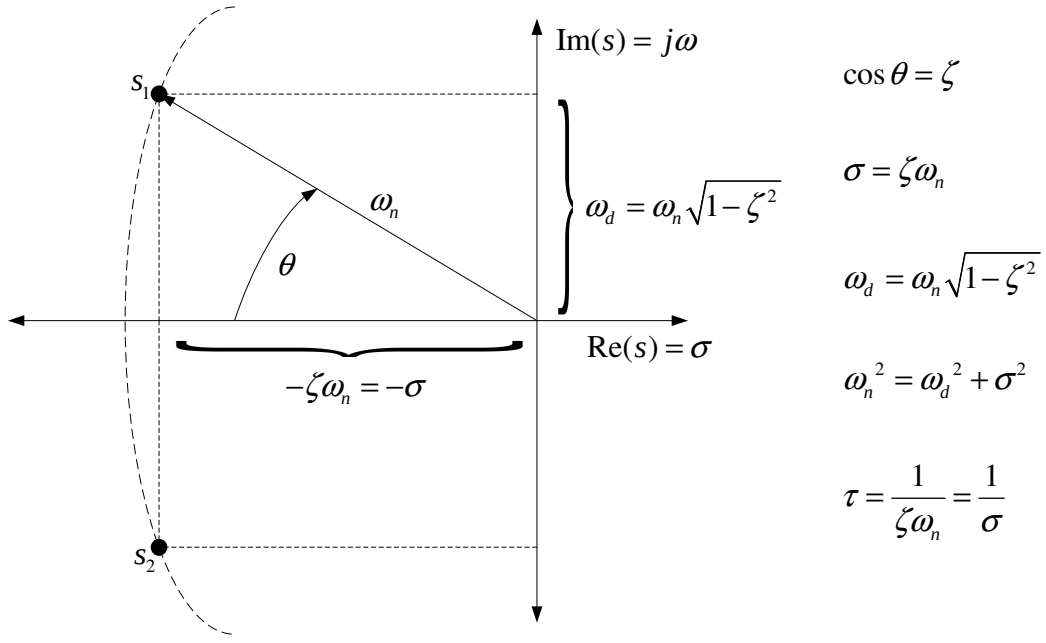


Figure 4.8 S-plane representation of the poles of a second order system

Based on the transient parameters given in Eqs. (4.25)-(4.26), the dynamics observed from the step responses in Figure 4.4 through Figure 4.7 can be related to their

respective transfer functions given in Table 4.3. However a comparison between Eq. (4.23) and the transfer functions in Table 4.3 shows that, in addition to the dominant second order expression $s^2 + 2\zeta\omega_n s + \omega_n^2$, the ZSC transfer functions have additional poles and zeros at higher frequencies. For example $G_{vd}(s)$ has a complex conjugate pole pair represented by the expression $(s^2 + 328.6s + 1611000)$ and a high frequency LHP pole represented by $(s+3746)$ in its denominator. Also it has a LHP zero and a RHP zero represented by $(s+3489)$ and $(s-7253)$, respectively. In order to have a comparison between the transfer functions in Table 4.3 and the step responses in Figure 4.4 through Figure 4.7, a "dominant pole-zero approximation" is needed for the transfer functions. This approximation rules can be summarized as follows [23]:

1. If a pole and a zero are near to each other and they are in the LHP of the s-plane they can be cancelled.

2. If the response of a pole decays very quickly, it can be ignored.

3. Poles nearest to the $j\omega$ axis are called "dominant poles" and should be retained.

4. A closed loop pole (zero) at $p_R(z_R)$ can be neglected in determining the transient parameters if $\zeta > 0.5$ and $|p_R| > 5\zeta\omega_n$ $(|z_R| > 5\zeta\omega_n)$.

All the ZSC transfer functions given in Table 4.3 have a pole and a zero that can be cancelled regarding to the above procedure. Also all the ZSC transfer functions have a second order expression in the denominator corresponding to a dominant complex conjugate pole pair. In addition all the step responses are underdamped since $0 < \zeta < 1$.

$G_{vd}(s)$ has a RHP zero which depresses the overshoot and causes the response to start in the reverse direction. Figure 4.9 shows the effect of the RHP zero on capacitor voltage after a step change in duty cycle. $G_{id}(s)$ and $G_{ig}(s)$ have LHP zeros at (s+511.4) and (s+293.9), respectively, which are not very far from the dominant pole locations. They cannot be ignored because their locations are not greater than their respective values of $5\zeta\omega_n$ which are $821.5\,rad/s$ for $G_{id}(s)$ and $968\,rad/s$ for $G_{ig}(s)$. So these LHP zeros may have a substantial effect on the transient parameters of their respective transfer functions. It was shown in [23] that a LHP zero whose value approaches to origin decreases the peak time and increases the overshoot.

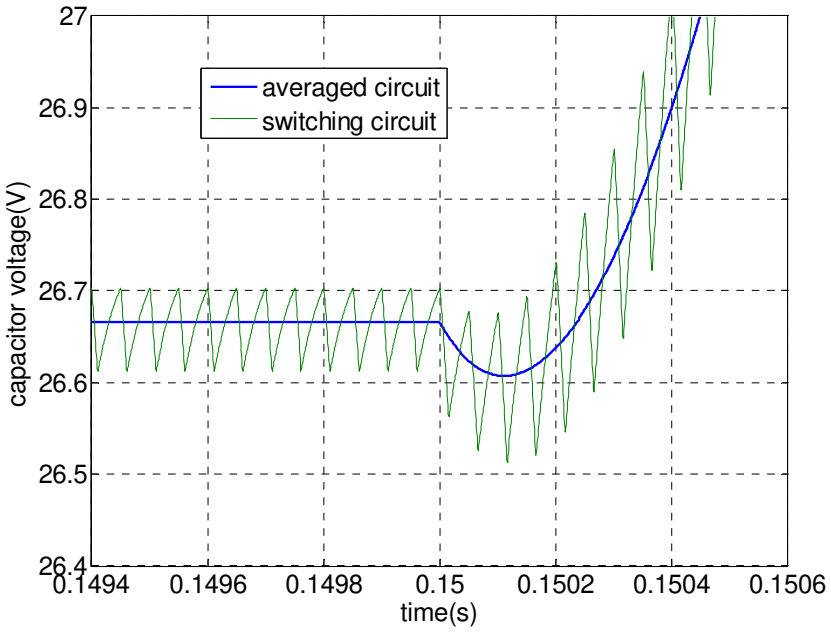


Figure 4.9 Effect of the RHP zero after a 10% step change in duty cycle

Table 4.4 shows some of the calculated transient parameters of the ZSC transfer functions given in Table 4.3. These calculations are based on Eqs. (4.25) and (4.26). The calculations neglected the effects of the zeros. These parameters can be compared to their obtained counterparts given in Table 4.2. It can be observed that the calculated and obtained ω_d and t_s are very close. Also the calculated and obtained t_p of $G_{vd}(s)$ and $G_{vg}(s)$ are close to each other. However there is a discrepancy between the calculated and obtained t_p values of $G_{id}(s)$ and $G_{ig}(s)$. It can be observed that the obtained values of t_p for both $G_{id}(s)$ and $G_{ig}(s)$ are smaller than the calculated ones. This clearly shows the substantial effect of the LHP zeros whose locations are close to the origin. It was observed in Table 4.3 that after the pole-zero cancellations, one LHP zero remains in the transfer functions of $G_{id}(s)$ and $G_{ig}(s)$. Also it was shown that they are smaller than $5\zeta\omega_n$ which makes their effect substantial. This effect can also be observed when we compare the calculated and obtained values of the percentage overshoot (P.O.). For a second order system, P.O. can be calculated using Eq. (4.27) [6], [22-23].

$$P.O. = 100e^{-\zeta\pi/\sqrt{1-\zeta^2}}\ \% \tag{4.27}$$

For $G_{id}(s)$ in Table 4.3, P.O. is calculated as 66% and obtained from Figure 4.5 as 235% For $G_{ig}(s)$ in Table 4.3, P.O. is calculated as 73% and obtained from Figure 4.7 as 493%. The LHP zeros in $G_{id}(s)$ and $G_{ig}(s)$ increases the P.O. substantially. The locations of the LHP zeros in $G_{id}(s)$ and $G_{ig}(s)$ are (s+511.4) and (s+293.9), respectively. This shows that the increasing effect becomes more severe when the LHP

zero approaches the origin. Another observation can be made about the depressing effect of the RHP in $G_{vd}(s)$. The P.O., calculated from $G_{vd}(s)$ in Table 4.3 is 66% and obtained from Figure 4.4 is 64%. The reason why the depressing effect is not severe can be explained by considering the location of the RHP zero. The RHP zero of $G_{vd}(s)$ in Table 4.3 is located at $7253 rad/s$ which is far greater than its $5\zeta\omega_n$ value which is $821.5 rad/s$. Finally, calculated and obtained P.O. of $G_{vg}(s)$ is 73%. This is expected because after the dominant pole zero approximation, only a second order expression remains in the denominator of $G_{vg}(s)$ which makes it similar to Eq. (4.23) without any additional effect of a pole or zero.

Table 4.4 Calculated transient parameters from ZSC transfer functions

Transient parameters / Step responses	$\omega_d\ (rad/s)$	$t_p\ (ms)$	$t_s\ (ms)$
$G_{vd}(s)=\dfrac{\hat{v}_c(s)}{\hat{d}(s)}$	1259	2.495	24.346
$G_{id}(s)=\dfrac{\hat{i}_L(s)}{\hat{d}(s)}$	1259	2.495	24.346
$G_{vg}(s)=\dfrac{\hat{v}_c(s)}{\hat{v}_g(s)}$	1909	1.646	20.661
$G_{ig}(s)=\dfrac{\hat{i}_L(s)}{\hat{v}_g(s)}$	1909	1.646	20.661

4.5 Summary

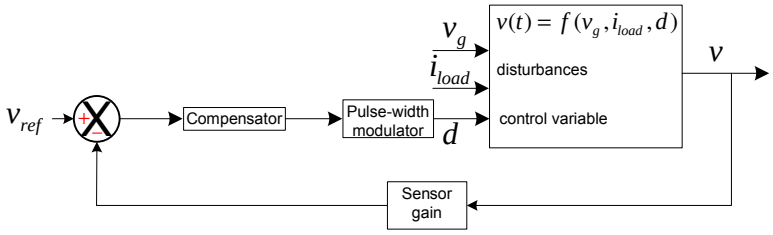
This chapter is about mathematical modeling of the dynamic behavior of the ZSC. First, an introduction is given about modeling in power converters. Then, state space averaging which is a common technique in modeling of the power converters is explained. After that the dynamic model of the ZSC is derived according to state space averaging and transfer functions are obtained. Finally, the validity of the ZSC small signal model is verified in two ways. First the simulated waveforms obtained from both the small signal circuit in Figure 4.3 and the switching circuit in Figure 4.2(a) are compared regarding to their transient parameters given in Table 4.2. Then the transfer functions derived in the previous section are used to calculate the transient parameters with the circuit parameters given in Table 4.1 inserted. The calculated and obtained transient parameters are compared and interpreted regarding to the "dominant pole-zero approximation" and existence of the LHP and RHP zeros. It is observed from the comparisons that the transfer functions derived in the previous section are able to explain the dynamics associated with the Z-source network. The discrepancies between the calculated and obtained values of the transient parameters are explained according the existence of the RHP and LHP zeros in the transfer functions. Based on the derived small signal model closed loop controllers can be designed and the dynamics associated with the ZSC can be improved.

CHAPTER V

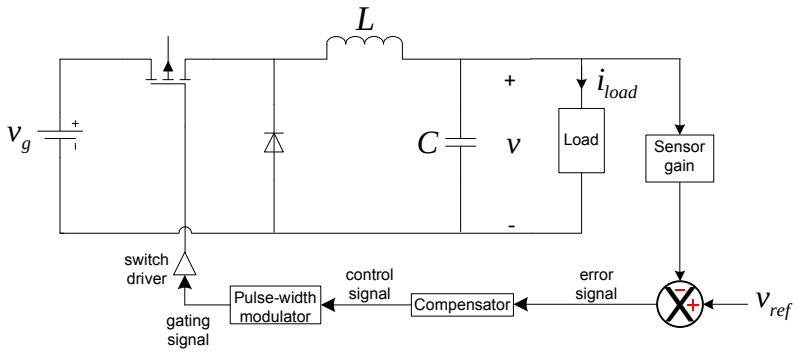
VOLTAGE MODE CONTROL

5.1 Introduction

In most of the power converters, the aim is to obtain a well regulated output voltage in spite of changes in the input voltage and the load current as well as circuit parameter values [2]. Figure 5.1(a) shows the block diagram of a typical voltage mode controlled power converter. Here the output voltage is measured through a sensor and compared to a reference voltage. The error is compensated through a compensator and the compensated error signal is used to produce the required gating signals through a pulse-width modulator. Negative feedback is required for automatic regulation of the output variable. In voltage mode (VM) control the aim is to make the value of the output voltage (v) times the sensor gain (H) equal to the reference voltage (v_{ref}) regardless of the disturbances (i_{load} *and* v_g) and variations in circuit parameters. The loop gain $T(s)$ is defined as the product of the small signal transfer functions of the forward and feedback loop elements. It is known that for a closed loop system, the disturbances are multiplied by a factor of $1/(1+T(s))$. So if the loop gain is large in magnitude then the effects of the disturbances on the output voltage is small [2].



(a) Single loop control functional block diagram



(b) Buck converter with single loop control

Figure 5.1 Voltage mode (single loop) control in power converters

Stability is an important issue in control of power converters. Adding a feedback loop may cause oscillations and overshoot depending on the compensation and converter parameters [6]. Generally simple phase margin method is sufficient for measuring the stability of a power converter.

5.2 VM Control of the ZSC

The closed loop VM control of peak dc-link voltage of the Z-source inverter has been studied in the literature [12-14]. The method proposed in [12] and [13] is called "indirect control". This method closes the control loop around the capacitor voltage in the Z-source network as shown in Figure 5.2. However, from the peak dc-link voltage

expression in Eq. (5.3), it is obvious that by controlling only the capacitor voltage, the dc-link voltage is open to disturbances coming from the input voltage. This effect could be transferred to the output side, which distorts the output voltage and increases the voltage stress across the switches. Figure 5.3 shows the simulated dc-link voltage waveform in case of step changes in input voltage when indirect control is used. It can be seen that the input disturbance affects the dc-link voltage and changes the peak value of it. Figure 5.4 shows the capacitor voltage where it is regulated around a steady state value.

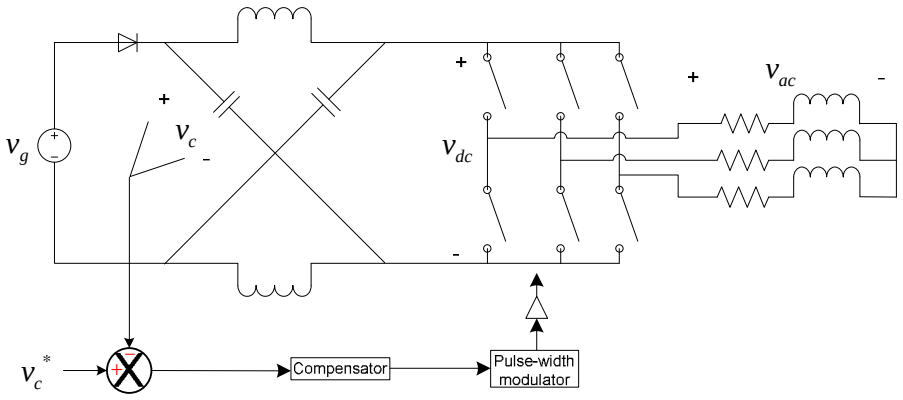


Figure 5.2 Indirect control of dc-link voltage of the Z-source inverter

The method proposed in [14] is called control of the peak dc-link voltage by direct measurement. This method uses a peak detection circuit to measure the peak dc-link voltage which has a pulsating waveform. This measurement is compared to the desired value of the peak dc-link voltage and the error is compensated through a compensator as in Figure 5.5. Using this method, it is possible to keep the peak dc-link voltage constant around a certain steady state value.

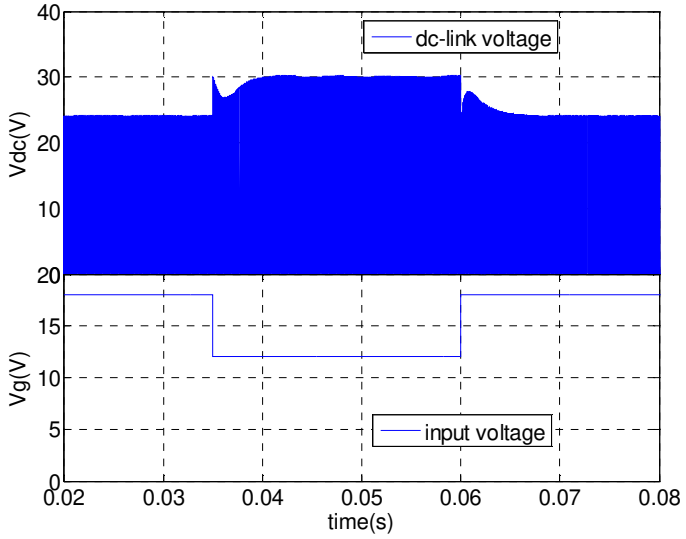


Figure 5.3 Effect of an input disturbance to dc-link voltage in indirect control

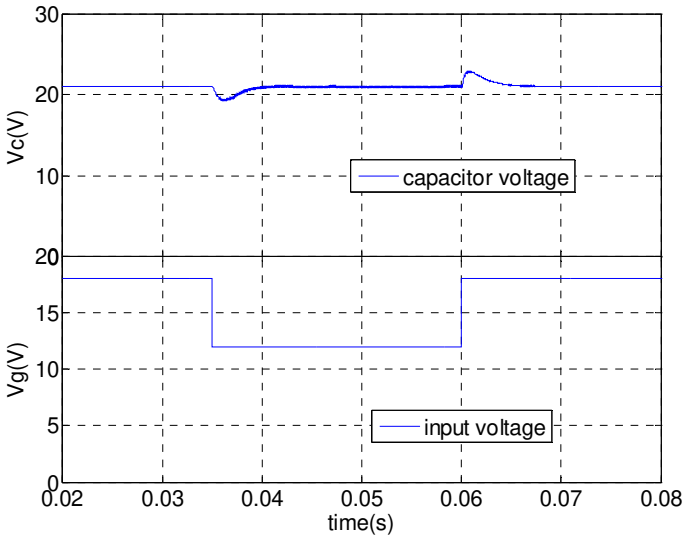


Figure 5.4 Effect of an input disturbance to capacitor voltage in indirect control

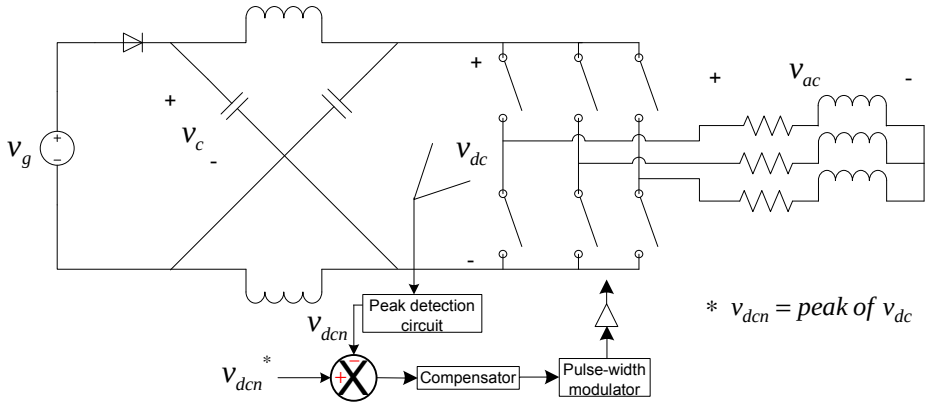


Figure 5.5 Control of the dc-link voltage of the Z-source inverter by direct measurement

In a traditional VSI, the magnitude of the output AC voltage depends on the inverter modulation index (M) and the magnitude of the dc-link voltage (v_{dc}) as in Eq. (5.1).

$$V_{ac} = M \frac{V_{dc}}{2} = M \frac{V_g}{2} \tag{5.1}$$

For a VSI, the dc-link voltage is equal to the dc-link capacitor voltage as shown in Figure 5.6. So if the input voltage is constant, the dc-link voltage is a constant and continuous signal.

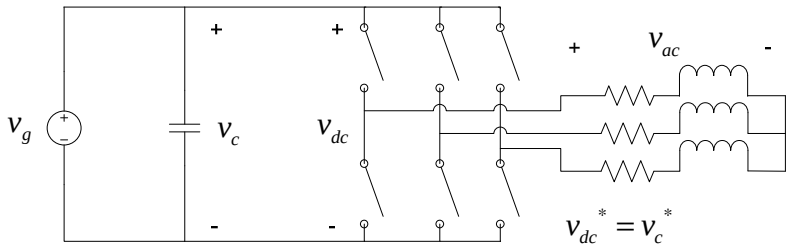


Figure 5.6 The dc-link voltage in a VSI

However, for the Z-source inverter, due to the impedance network between the input voltage and the inverter bridge, the dc-link voltage has a pulsating nature rather than a continuous one as shown in Figure 5.7. The magnitude of the output AC voltage depends on an additional parameter called the boosting factor (B) as in Eq. (5.2).

$$V_{ac} = M\frac{V_{dcn}}{2} = MB\frac{V_g}{2} \tag{5.2}$$

The expression of the dc-link voltage in the Z-source inverter was derived in Chapter III using the simplified version of the Z-source inverter given in Figure 3.3 (Figure 5.8) as in Eq. (5.3).

$$\begin{aligned} v_{dc} &= 0 && 0 < t < dT \\ v_{dc} &= v_{dcn} = v_C - v_L = 2v_C - v_g && dt < t < T \end{aligned} \tag{5.3}$$

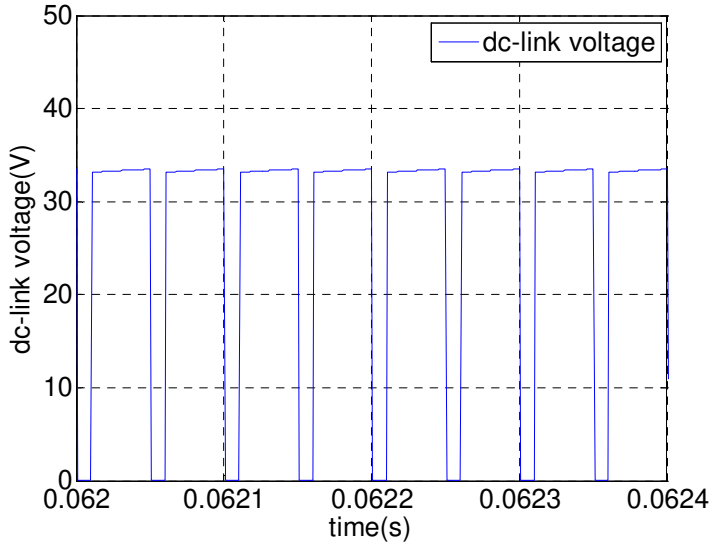


Figure 5.7 Typical dc-link voltage of a Z-source inverter

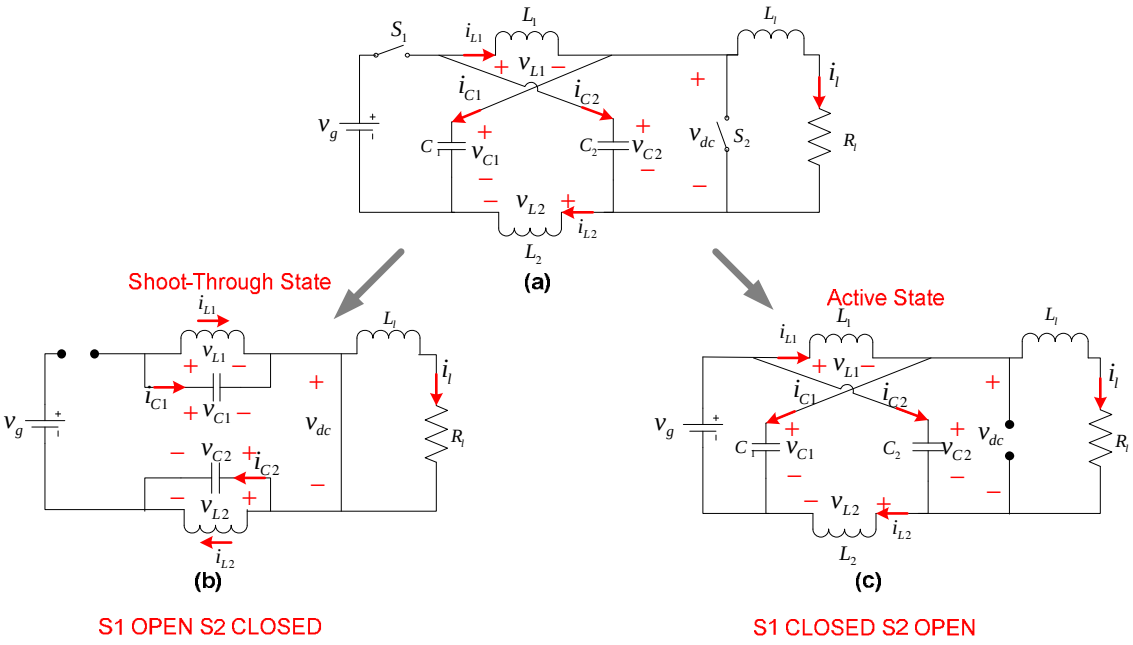


Figure 5.8 (a) Simplified circuit of the ZSI (b) shoot-through state (c) active state

Based on Eq. (5.3) and Figure 5.8, the dc-link voltage of the Z-source inverter is either zero when the inverter is in the shoot-through state, or a non-zero value when the inverter is in the active state. The non-zero value of the dc-link voltage (peak dc-link voltage) is a linear combination of the capacitor voltage which is a state variable and the input voltage ($v_{dcn} = 2v_C - v_g$). In steady state operation the capacitor voltage and the input voltage are continuous signals. Although the dc-link voltage (v_{dc}) itself is a pulsating waveform, the peak value of the dc-link voltage (v_{dcn}) can be obtained as a continuous signal since it is composed of two continuous signals.

The control method proposed in this research is based on direct control of the peak dc-link voltage without direct measurement. Instead of measuring the peak dc-link voltage itself, it is reproduced using the measurements of the capacitor voltage and the

input voltage according to the linear relation ($v_{dcn} = 2v_C - v_g$) as shown in Figure 5.9. As mentioned before, this reproduced signal (v_{dcn}) is a continuous signal but it has the same peak value with the peak dc-link voltage as seen in Figure 5.10. The VM control loop is closed around v_{dcn} by compensating the error signal coming from the difference between the desired and reproduced values of the peak dc-link voltage.

In order to prove the concept, the simplified ZSC circuit shown in Figure 5.11 is used both in simulations and experiments for this research. Figure 5.12 shows the simulated dc-link voltage waveform in case of step changes applied to the input voltage where the proposed control method is used. Compared to Figure 5.3 where indirect control is employed, proposed method keeps the dc-link voltage constant (or regulated) around a steady state value.

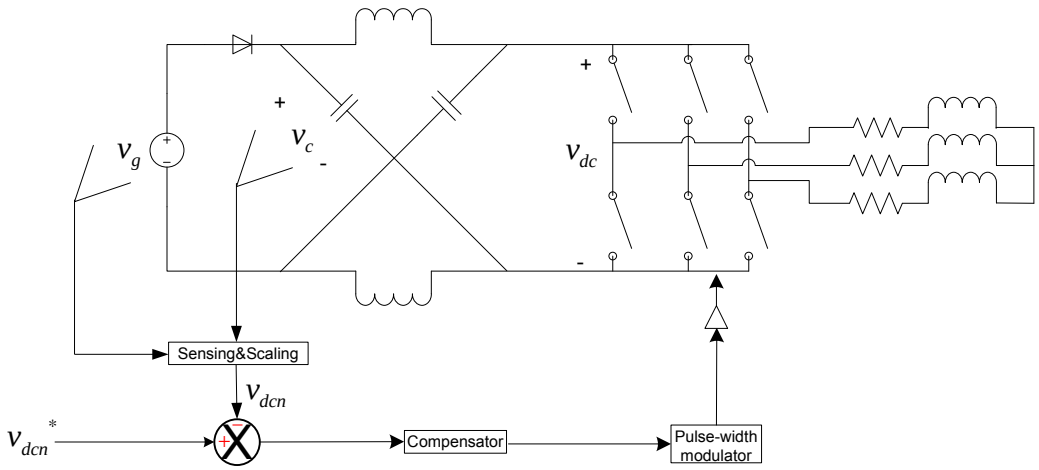


Figure 5.9 Control of the dc-link voltage by estimation without direct measurement

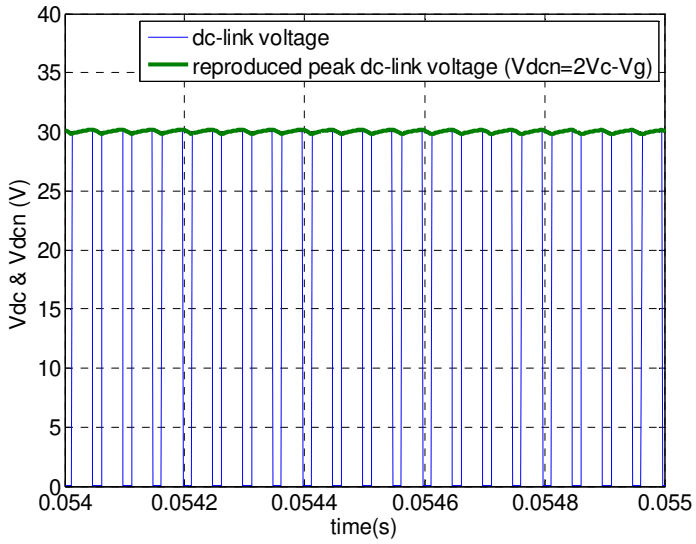


Figure 5.10 Simulated dc-link and reproduced peak dc-link voltages

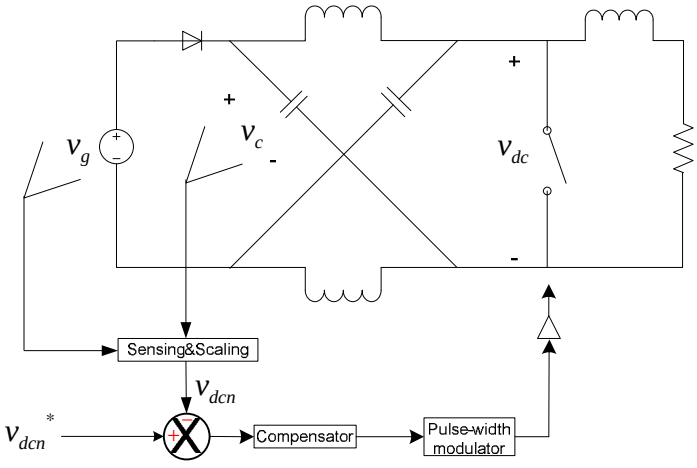


Figure 5.11 Simplified ZSC used for this research

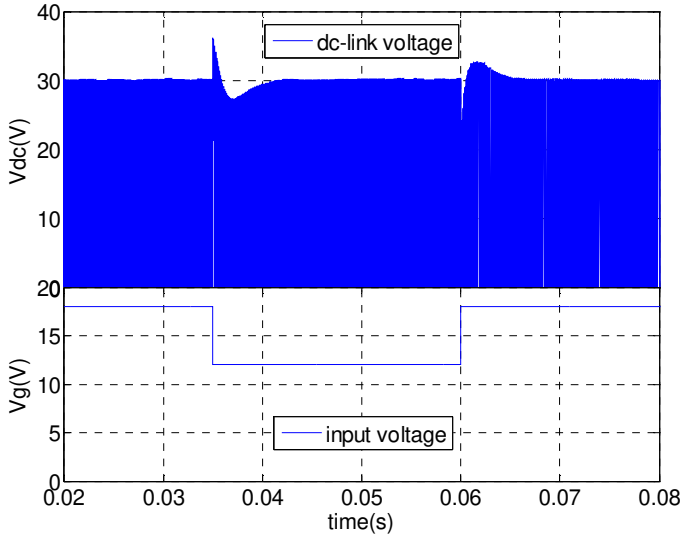


Figure 5.12 DC-link voltage in case of an input disturbance using proposed method

Compared to the direct measurement method in Figure 5.5 proposed in [14], the control method proposed in this research eliminates the use of a peak detection circuit. The sensing and scaling circuit used in Figure 5.11 is much more simpler than the peak detection circuit used in [14]. A disadvantage of the proposed method is that two measurements is required instead of one.

5.3 Compensator Design

The feedback control of a power converter requires that the output variable is well regulated around a steady state value achieving a good disturbance rejection. The output variable is generally the output voltage of the power converter. Output voltage of the buck converter (v) shown in Figure 5.1 is equal to the output capacitor voltage (v_c). As explained in Chapter IV, capacitor voltage and inductor current are used as state variables

in small signal modeling of the power converters. So for the buck converter in Figure 5.1, the output variable is actually a state variable and the transfer function required to design the compensator is the control-to-capacitor voltage (or duty cycle-to-capacitor voltage) transfer function.

The output variable of the Z-source inverter is the AC voltage at the output of the inverter bridge as shown in Figure 5.9. From Eq. (5.2) for a constant modulation index (M), the magnitude of the output AC voltage is directly related to the peak value of the dc-link voltage. Therefore the peak dc-link voltage can be chosen as the output variable in closed loop control of the Z-source inverter. In order to design the compensator the control-to-peak dc-link voltage transfer function should be determined. However, the state space averaging method explained in Chapter IV cannot be applied to the dc-link voltage due to its pulsating nature. The solution to this problem comes from the proposed control method shown in Figure 5.11 where the feedback loop is closed around the reproduced peak dc-link voltage ($v_{dcn} = 2v_C - v_g$). As explained in the previous section and shown in Figure 5.10, v_{dcn} is a continuous signal and has the same peak value with the dc-link voltage (v_{dc}). So the control-to-output (or control-to-peak dc-link voltage) transfer function required for compensator design can be derived using v_{dcn}. It was mentioned before that v_{dcn} is a linear combination of a state variable and an input variable. Therefore, the perturbation in v_{dcn} can be stated as the linear combination of the perturbations in the capacitor voltage and the input voltage as in Eq. (5.4) and Figure 5.13.

$$\hat{v}_{dcn} = 2\hat{v}_C - \hat{v}_g \tag{5.4}$$

The state space averaged model of the ZSC given in Chapter IV based on the derivations in [8] gives the small signal transfer functions of the converter state variables. The perturbation in the capacitor voltage is expressed in Eq. (4.17) which is repeated in Eq. (5.5).

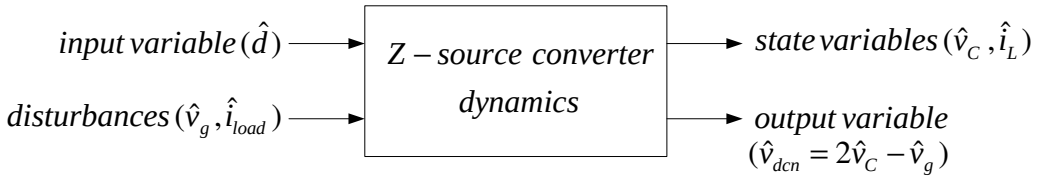


Figure 5.13 Small signal diagram of the ZSC dynamic model

$$\hat{v}_C(s) = G_{vd}(s)\hat{d}(s) + G_{vg}(s)\hat{v}_g(s) \tag{5.5}$$

G_{vd} and G_{vg} are the control-to-capacitor voltage and the input-to-capacitor voltage transfer functions, respectively. The small signal expression for v_{dcn} can be obtained by inserting Eq. (5.5) into Eq. (5.4),

$$\hat{v}_{dcn}(s) = G_{vnd}(s)\hat{d}(s) + G_{vng}(s)\hat{v}_g(s) \tag{5.6}$$

where,

$$G_{vnd}(s) = 2G_{vd}(s) \text{ and } G_{vng}(s) = 2G_{vg} - 1 \tag{5.7}$$

Eq. (5.7) gives the required transfer functions for designing the compensator in Figure 5.11. Here, $G_{vnd}(s)$ and $G_{vng}(s)$ are the control-to-peak dc-link voltage and input-to-peak dc-link voltage transfer functions, respectively.

The validity of the small signal expression in Eq. (5.4) and the transfer functions in Eq. (5.7) can be verified similar to the verification of the dynamic model of the ZSC given in Chapter IV. This time the simplified ZSC circuit given in Figure 4.2 (Figure 5.8) and the small signal averaged circuit given in Figure 4.3 are both simulated using the parameters given in Table 5.1.

Table 5.1 Circuit parameters used for this research

V_g	$R_{l\,nom}$	L_l	C	L	f_s
20V	10Ω	$680\mu H$	$470\mu F$	$452\mu H$	$20\,khz$

Figure 5.14 and Figure 5.15 show the response of the dc-link voltage (v_{dc}) and the averaged reproduced peak dc-link voltage ($\overline{v_{dcn}}$) signals to step changes in the shoot-through duty ratio (d) and the input voltage (v_g), respectively. Analysis of the response in both figures shows that the waveforms of v_{dc} obtained from the switching circuit and $\overline{v_{dcn}}$ obtained from the averaged circuit have the same dynamic behavior. It can be seen from Eq. (5.7) that G_{vnd} and G_{vd} have a linear relationship ($G_{vnd}(s) = 2G_{vd}(s)$) implying that they have the same dynamic behavior except their magnitudes are different. This can be observed by comparing Figure 5.14b and Figure 5.14d where both waveforms contain a damped oscillation at the time of the step change in the duty cycle. It can be seen from the two waveforms that the damped oscillation seen in the capacitor voltage waveform have the same characteristics with the damped oscillation seen in the dc-link voltage except the magnitude of the oscillation is halved in the former case.

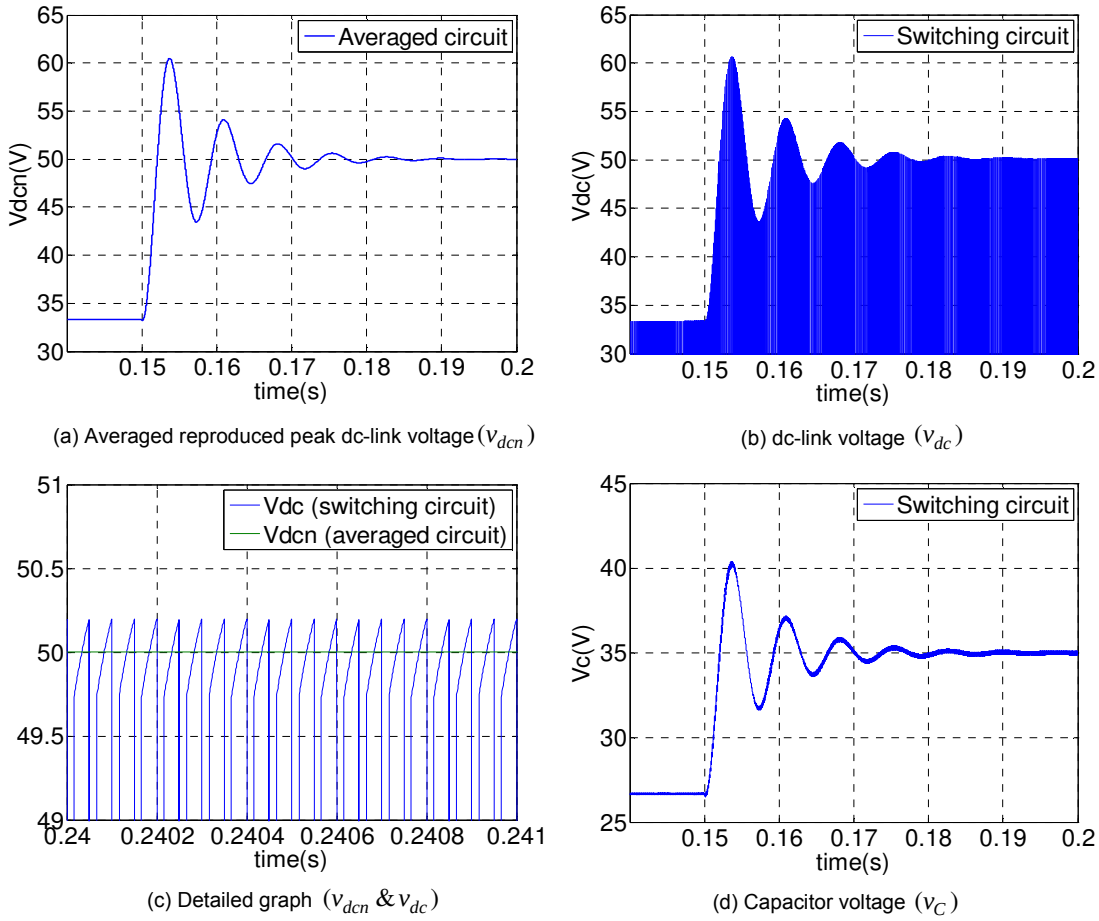


Figure 5.14 Simulation waveforms of switching and averaged circuits when subjected to a step change from 0.2 to 0.3 in d

Similarly, Figure 5.15b and Figure 5.15d show the effect of an input voltage step change in the dc-link voltage and the capacitor voltage, respectively. Here an initial dip is observed in the dc-link voltage waveform at the time of the step change, whose amount is the same with the amount of the step change. This initial dip is followed by a damped oscillation whose amplitude is two times the amount of the damped oscillation in the capacitor voltage. This is clearly seen in the expression of $G_{vng}(s) = 2G_{vg} - 1$.

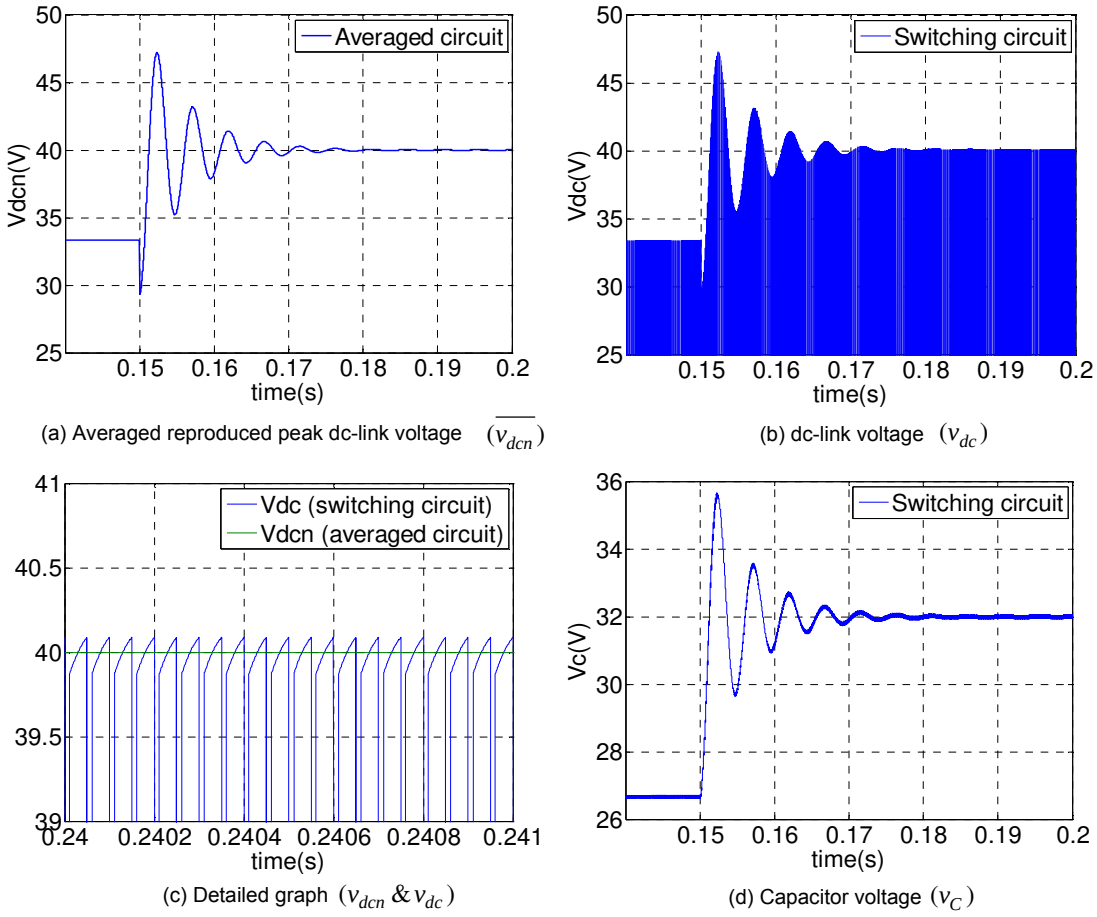


Figure 5.15 Simulation waveforms of switching and averaged circuits when subjected to a step change from 20V to 24V in V_g.

Similar to the analysis in Chapter IV, dynamics of $\overline{v_{dcn}}$, v_{dc} and v_C in Figure 5.14 and Figure 5.15 can be compared in terms of their transient parameters like damped natural frequency (ω_d), peak time (t_p), settling time (t_s) and percentage overshoot ($P.O.$). Table 5.2 shows some of the transient parameters obtained from the respective step responses.

Table 5.2 Obtained transient parameters from simulated ZSC step responses

Transient parameters / Step responses	$\omega_d\ (rad/s)$	$t_p\ (ms)$	$t_s\ (ms)$	$P.O.(\%)$
Figure 5.14 (a) ($\overline{v_{dcn}}$)	866	3.75	~ 30	63
Figure 5.14 (b) (v_{dc})	866	3.75	~ 30	63
Figure 5.14 (d) (v_C)	866	3.75	~ 30	63
Figure 5.15(a) ($\overline{v_{dcn}}$)	1307	2.33	~ 25	67.5
Figure 5.15(b) (v_{dc})	1307	2.33	~ 25	67.5
Figure 5.15(d) (v_C)	1307	2.33	~ 25	67.5

It can be clearly seen from the results that the averaged reproduced peak dc-link voltage ($\overline{v_{dcn}}$) has the same dynamic behavior with both the dc-link voltage (v_{dc}) and the capacitor voltage. This verifies that the reproduced continuous signal ($v_{dcn} = 2v_C - v_g$) can be used for designing the compensator for controlling the peak value of the dc-link voltage. As mentioned before the dc-link voltage has pulsating waveform and the state space averaging method cannot be applied directly to control its peak value. The results in Table 5.2 also prove that the relation ($G_{vnd}(s) = 2G_{vd}(s)$) is valid because the responses of $\overline{v_{dcn}}$ and v_C have the same transient parameters which implies that their poles and zeros are the same.

Another verification method used in Chapter IV was to compare the calculated and obtained transient parameters of the transfer function. This method can also be used for verification of G_{vnd} and G_{vng}. Table 5.3 shows the numerical counterparts of the reproduced peak dc-link voltage (v_{dcn}) transfer functions (G_{vnd} and G_{vng}) when the values in Table 5.1 are inserted. A dominant pole-zero approximation is not possible by direct pole-zero cancellation. However the locations of the high frequency (HF) LHP poles and zeros as well as the RHP zero in G_{vnd} are far greater than their respective values of $5\zeta\omega_n$ which are $650.25\,rad$ for $G_{vnd}(s)$ and $849.25\,rad$ for $G_{vng}(s)$. This implies that the effects of the HF poles and zeros will not be significant. This can be easily seen from the close values of the obtained (Table 5.2) and calculated (Table 5.4) transient parameters of G_{vnd} and G_{vng}.

Table 5.3 Reproduced peak dc-link voltage (v_{dcn}) transfer functions

$G_{vnd}(s) = \dfrac{\hat{v}_{dcn}(s)}{\hat{d}(s)}$	$\dfrac{(s+8729)\ (s-5659)}{(s+11730)\ (s^2+260.1s+769900)}$
$G_{vng}(s) = \dfrac{\hat{v}_{dcn}(s)}{\hat{v}_g(s)}$	$\dfrac{(s+6354)}{(s+11650)\ (s^2+339.7s+1744000)}$

The small signal expression given in Eq. (5.6) can be used to design compensators for VM control method. Figure 5.16 shows the control block diagram for VM control of the ZSC. In VM control, the peak dc-link voltage is estimated using $v_{dcn} = 2v_C - v_g$ and compared to the reference voltage (v_{ref}). The error is compensated through $G_c(s)$. The

control-to-capacitor voltage ($G_{vd}(s)$) and the input-to-capacitor voltage ($G_{vg}(s)$) transfer functions were derived and given in Eqs. (4.19) and (4.20).

Based on the small signal expression of the reproduced peak dc-link voltage given in Eq.(5.6), the VM compensator block (G_c) in Figure 5.16 is designed using the design specifications in Table 5.1. MATLAB/SISO Tool is used for compensator tuning and obtaining the Bode plots. For VM control, a PID compensator is used in which both compensator zeros are placed on the resonant poles of the control-to-reproduced peak dc-link voltage transfer function (G_{vnd}) of the ZSC as in Figure 5.17. The high frequency compensator pole is placed at 10 times the selected crossover frequency to obtain a wide bandwidth. In this design a phase margin of 44.3^o is obtained with a $1kHz$ crossover frequency. The transfer function of the designed compensator is given in Eq. (5.8).

Table 5.4 Calculated transient parameters from ZSC transfer functions

Transient parameters / Step responses	$\omega_d\,(rad/s)$	$t_p\,(ms)$	$t_s\,(ms)$	$P.O.(\%)$
$G_{vnd}(s)=\dfrac{\hat{v}_{dcn}(s)}{\hat{d}(s)}$	867	3.623	30.76	62.44
$G_{vng}(s)=\dfrac{\hat{v}_{dcn}(s)}{\hat{v}_g(s)}$	1309	2.399	23.55	66.54

$$G_c(s)=1.6\frac{(s+1180)(s+1180)}{s(s+62800)} \tag{5.8}$$

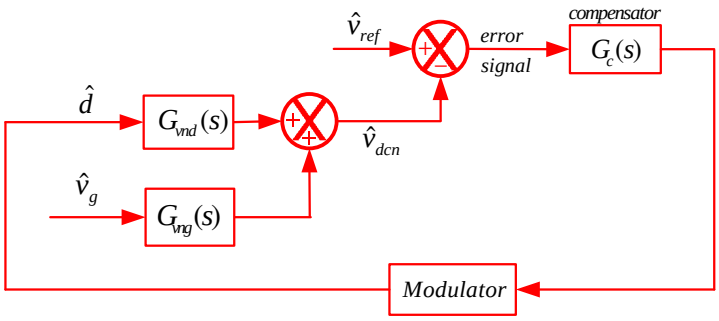


Figure 5.16 VM control of v_{dcn}

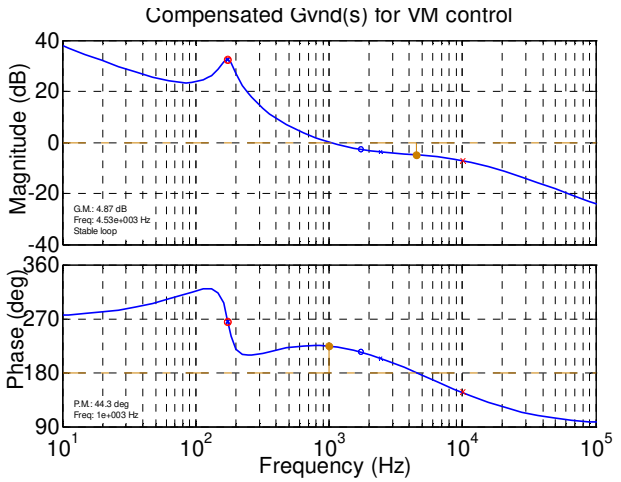


Figure 5.17 Magnitude and phase plots of VM controlled ZSC

5.4 Summary

This chapter first gave a brief introduction on voltage mode (VM) control in power converters. Then the research that is done so far on VM control of the ZSC is reviewed. Next the control method proposed in this research is explained and the verification is done by comparison of the simulated waveforms and the transient parameters. Finally, the designed compensator for the VM control loop is given.

CHAPTER VI

CURRENT PROGRAMMED MODE CONTROL

6.1 Introduction

VM control is achieved by direct choice of the on/off time of the switch (duty ratio) according to the compensated error signal. Current Programmed Mode (CPM) control is another scheme in which the output voltage is controlled by controlling the inductor current [2]. Figure 6.1 shows the block diagram of a CPM controlled buck converter. The control input is a current reference and the switching pattern is determined such that the inductor current follows this current reference. The current reference is the compensated error signal coming from the difference between the converter output voltage and the reference voltage which is the same architecture for VM control. Generally, the switch current is measured instead of the inductor current since they have the same peak value. Figure 6.2 shows the waveforms of typical switch current and current reference signals. In CPM control, the inductor current rises with some positive slop until it hits the reference current which turns the switch off. This time the inductor current decreases until the next cycle.

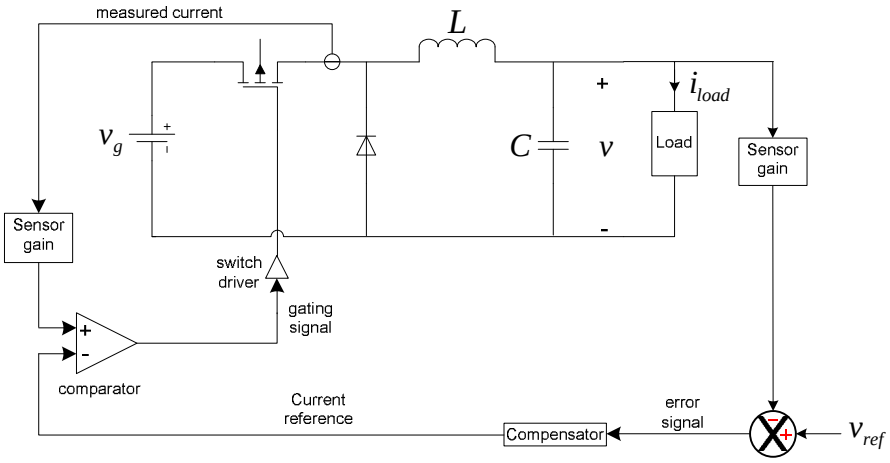


Figure 6.1 CPM control of buck converter

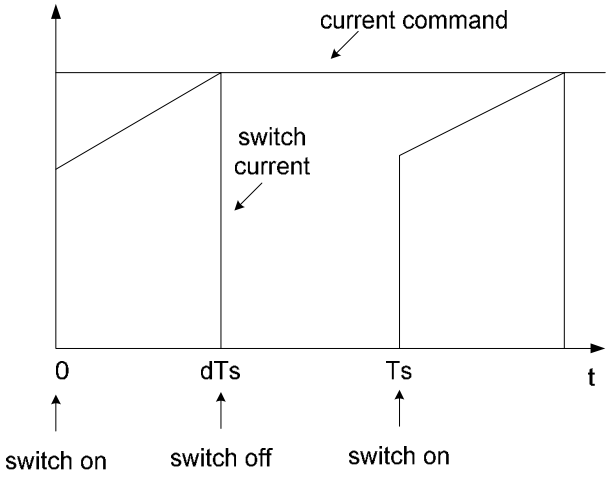


Figure 6.2 Switch current and current command

The advantage of CPM control is that it simplifies the dynamics of the converter by reducing the number of poles in the control-to-output transfer function. Actually for a converter having a second order filtering, this pole goes to high frequencies near the switching frequency [7]. In CPM control it is generally possible to obtain a stable output voltage with a simpler compensator compared to VM control. Although additional

circuitry is required for measuring the switch current in CPM control, this may also be required in VM control for current limiting purposes.

A disadvantage of CPM control is the sensitivity of the sensed current to switching noise in the converter. This noise may appear as a spike in the sensed current which may turn off the switch before it reaches the current command. Another critical issue for CPM control is the stability problem appearing for duty cycles greater than 0.5. This requires the addition of a stabilizing ramp signal to the sensed current which also improves noise susceptibility. Figure 6.3 shows the addition of the stabilizing ramp to the current command.

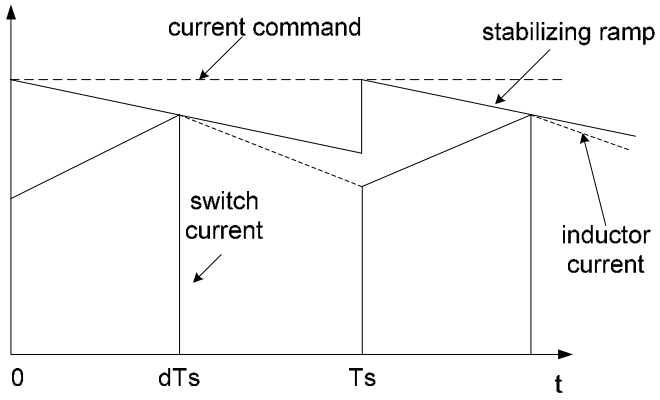


Figure 6.3 Addition of the stabilizing ramp to the current command

6.2 CPM Control of the ZSC

The dynamics of the ZSC shows a non-minimum phase behavior due to the RHP zero appearing in the control-to-capacitor voltage transfer function given in (4.20). The effect of this non-minimum phase behavior is seen when the compensator for the VM control was being designed in Chapter V where limited phase margin was obtained. It is

explained in [7] that the compensation of the converters containing RHP zeros may be easier if CPM control is used. In CPM control, dynamics of the converter gets simpler due to the fact that the pole coming from the inductor is pushed to high frequencies (half the switching frequency). Physically the inductor current follows the reference current produced by the outer loop such that it behaves like a current source. If the variations in the reference current produced by the outer loop are slower compared to the inner current loop speed than the assumption of inductor current equals to the reference current becomes valid [1]. In CPM, the duty cycle becomes an auxiliary variable implicitly determined by the inductor current, so the state equations derived in Chapter IV (repeated in Eq. (6.1)) can be solved for the duty cycle to obtain the new control rule for CPM control of ZSC.

$$\begin{aligned} sL\hat{i}_L(s) &= (D-D')\hat{v}_C(s) + D'\hat{v}_g(s) + (2V_C - V_g)\hat{d}(s) \\ sC\hat{v}_C(s) &= (D'-D)\hat{i}_L(s) + (-2I_L + I_l)\hat{d}(s) - D'\hat{i}_l(s) \\ sL_l\hat{i}_l(s) &= 2D'\hat{v}_C(s) - D'\hat{v}_g(s) + (-2V_C + V_g)\hat{d}(s) - R_l\hat{i}_l(s) \end{aligned} \tag{6.1}$$

Assuming that the inductor current follows the reference current ($\hat{i}_L = \hat{i}_{ref}$),

$$\hat{d}(s) = \frac{sL\hat{i}_{ref}(s) - (D-D')\hat{v}_c(s) - D'\hat{v}_g(s)}{2V_c - V_g} \tag{6.2}$$

By inserting Eq. (6.2) into Eq. (6.1), we can obtain the new state equations for CPM control of ZSC as in Eq. (6.3),

$$\begin{aligned} \hat{i}_l(s)[sL_l + R_l] &= \hat{v}_c(s) - sL\hat{i}_{ref}(s) \\ sC\hat{v}_c(s) &= [(D-D') - sL\frac{I_L}{V_c}]\hat{i}_{ref}(s) + \frac{I_L}{V_c}(D-D')\hat{v}_c(s) + \frac{I_L}{V_c}D'\hat{v}_g(s) - D'\hat{i}_l(s) \end{aligned} \tag{6.3}$$

The first equation in Eq. (6.3) shows the effects of the changes in v_C and i_{ref} to i_l and the second equation shows the effects of changes in i_{ref}, i_l and v_g to v_C. The changes in i_{ref} are independent variations, while the changes in i_l, v_g and v_C depend on the circuit parameters. A CPM small signal circuit based on Eq. (6.3) is given in Figure 6.4, where $D' = 1 - D$. D, V_C and I_L are the steady state values of d, v_C and i_L, respectively. Based on this circuit and Eq. (6.3), CPM control-to-capacitor voltage (G_{vi}) and input-to-capacitor voltage (G_{vg}) transfer functions are given in Eq. (6.4) and Eq. (6.5), respectively. The characteristic equation of both the transfer functions given in Eqs. (6.4) and (6.5) are second order. Compared to VM control, the order of the system is reduced by one. This can be observed from the small signal circuit in Figure 6.4 where two sub-circuits exist, one for each state variable.

It should be noted that although the dynamics of the inductor current seems to be disappeared in the CPM model, it actually exists in the high frequencies. More accurate models for CPM control of power converters are derived in the literatures [2] and [7]. In CPM an inherent oscillation phenomenon exists due to the HF inductor pole. This brings a sub-harmonic oscillation problem with it if the duty cycle is greater than 0.5. For ZSC, since the duty cycle is naturally limited to 0.5, addition of the compensating ramp for the oscillation problem as in Figure 6.3 is not necessary.

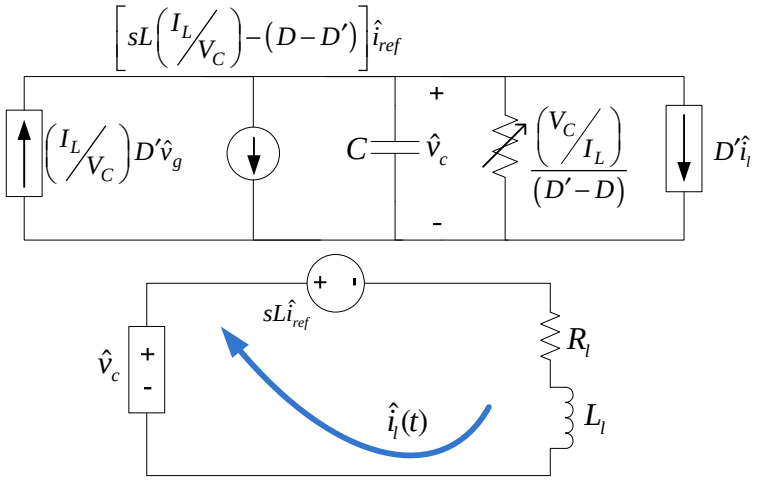


Figure 6.4 CPM small signal circuit of ZSC

$$G_{vi}=\left.\frac{\hat{v}_c(s)}{\hat{i}_{ref}(s)}\right|_{\hat{v}_g(s)=0}=\frac{-s^2LL_l(I_L/V_c)-s(LR_lI_L/V_c-L_l(D'-D)+LD')+R_l(D'-D)}{s^2L_lC+s(R_lC+L_l(D'-D)I_L/V_c)+(D'+(D'-D)R_lI_L/V_c)} \quad (6.4)$$

$$G_{vg}=\left.\frac{\hat{v}_c(s)}{\hat{v}_g(s)}\right|_{\hat{i}_{ref}(s)=0}=\frac{(sL_l+R_l)D'I_L/V_c}{s^2L_lC+s(R_lC+L_l(D'-D)I_L/V_c)+(D'+(D'-D)R_lI_L/V_c)} \quad (6.5)$$

6.3 Compensator Design

Figure 6.5 shows the CPM controlled simplified ZSC. Similar to the VM control case the output variable to be controlled is the peak value of the dc-link voltage. But it was explained in Chapter V that the dc-link voltage has a pulsating nature and is not suitable for direct use for control. The reproduced peak dc-link voltage ($v_{dcn}=2v_C-v_g$) defined and used for VM control, can also be used for closing the outer loop in CPM control of the ZSC. The reference current (i_{ref}) for the inner current loop is produced by comparing the desired and measured values of the reproduced peak dc-link voltage (v_{dcn})

and compensating the error signal through the outer voltage loop compensator. Inner loop should be fast enough to keep the inductor current equal to the reference current, so the current sensor gain which behaves like a proportional controller is enough for inner loop compensation. Figure 6.6 shows the small signal block diagram of Figure 6.5, where G_{cv} is the outer voltage loop compensator and G_{ci} is the inner current loop compensator.

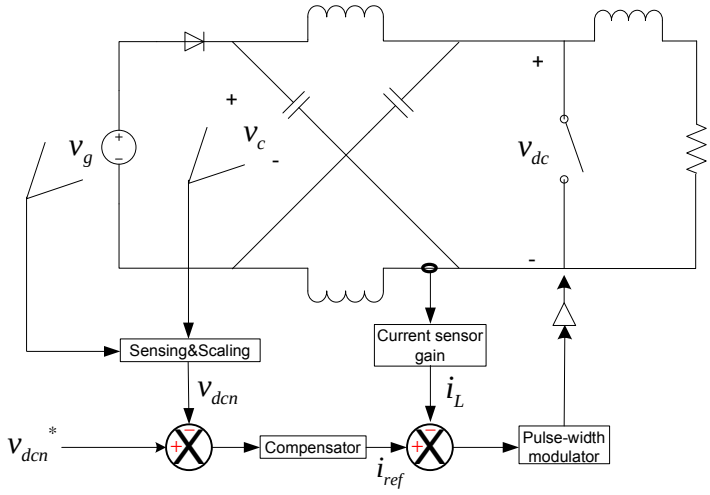


Figure 6.5 CPM control of simplified ZSC

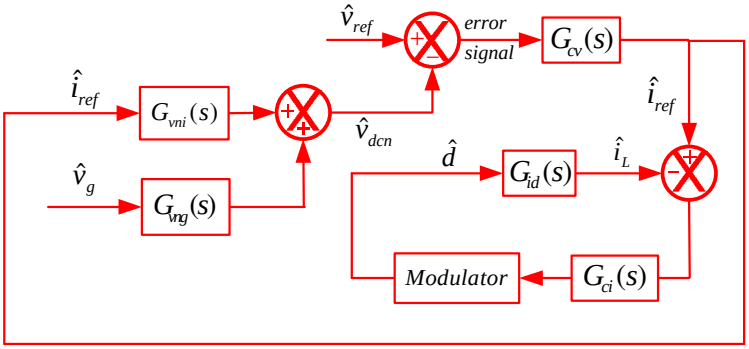


Figure 6.6 Small signal block diagram of CPM control of ZSC

The small signal expression for the reproduced peak dc-link voltage ($v_{dcn} = 2v_C - v_g$) was obtained in Chapter V by direct perturbation as $\hat{v}_{dcn} = 2\hat{v}_C - \hat{v}_g$. Based on this small signal expression and similar to VM control, Eq. (6.6) can be used for designing the outer loop compensator for CPM control, where $G_{vni}(s)$ and $G_{vng}(s)$ are the control-to-reproduced peak dc-link voltage and the input-to-reproduced peak dc-link voltage transfer functions for CPM, respectively.

$$\hat{v}_{dcn}(s) = G_{vni}(s)\hat{i}_{ref}(s) + G_{vng}(s)\hat{v}_g(s) \tag{6.6}$$

where,

$$G_{vni}(s) = 2G_{vi}(s) \; and \; G_{vng}(s) = 2G_{vg} - 1 \tag{6.7}$$

Using the same circuit parameters with the VM control case given in Table 5.1, the pole and zero locations of G_{vni} can be obtained as in Eq. (6.8). The RHP zero which appeared in the control-to-reproduced dc-link voltage transfer function for VM control case also appeared here. The locations of the LHP pole and two zeros are far from the single pole location. This implies that the dynamics of the ZSC will be dominated by this single pole.

$$G_{vni} = \frac{\hat{v}_c(s)}{\hat{i}_{ref}(s)} = \frac{\text{(s-14760) (s+22050)}}{\text{(s+14490) (s+432)}} \tag{6.8}$$

Due to the simpler dynamics of the CPM controlled ZSC compared to the VM control case, a PI controller is employed for the outer loop compensation. Zero of the compensator is selected close to the single pole location and a HF pole which is around

10 times the crossover frequency is employed to get a wide bandwidth. In this design a PM of 71^o and a crossover frequency of $1kHz$ is obtained. Eq. (6.9) gives the transfer function of the designed outer loop compensator. Figure 6.7 shows the magnitude and phase plots of the compensated ZSC. Compared to the VM controlled case it can be observed that the compensation is easier in CPM controlled ZSC.

$$G_c(s) = 82000\frac{(s+700)}{s(s+62800)} \tag{6.9}$$

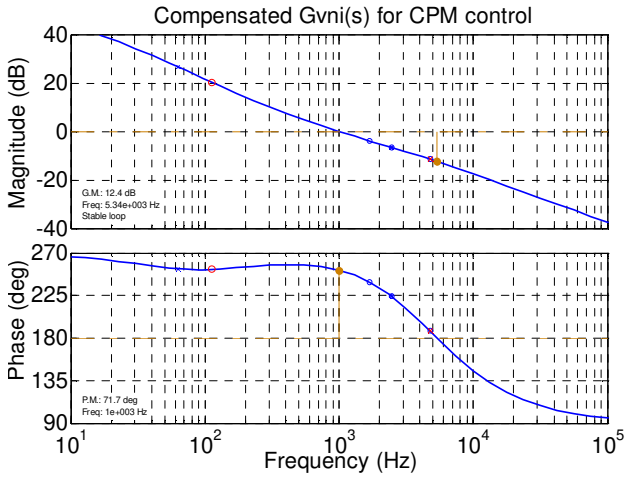


Figure 6.7 Magnitude and phase plots of CPM controlled ZSC

6.4 Summary

CPM is a common control method for power converters. It simplifies the dynamics of the converter and allows easier compensation especially for converters with RHP zeros. In this chapter, a CPM model for the ZSC has been derived together with the small signal circuit and the transfer functions. Based on the derived model an outer loop compensator has been designed.

CHAPTER VII

SIMULATION AND EXPERIMENTAL RESULTS

7.1 Introduction

Testing the operation of electrical circuits through simulations and experiments is essential to verify their theoretical analysis and design. The experimental verification becomes more important for power converters due to real life facts like component non-idealities, noise-sensitivity of the control circuit, parasitic effects etc. Experimental operations of the traditional power converter topologies like buck, boost or flyback have been realized by many engineers and described in the literature. However, since ZSC is a new power converter topology in the literature of power electronics, the experimental verifications for this topology are limited to the papers written so far. So, an important part of this research is building the ZSC and comparing both the simulated and experimental waveforms. The ZSC with the circuit non-idealities has been simulated using MATLAB-SIMULINK. Then, the real circuit is implemented using analog controllers. Steady state operation results as well as the closed loop control results using both VM and CPM controls are obtained. The performances of the designed controllers are tested by applying line and load disturbances. Experimental setup is described and the results are presented in the following sections.

7.2 Experimental Setup

Figure 7.1 shows the block diagrams for both VM and CPM controlled simplified ZSCs. The experimental setup is composed of four basic circuits:

- Sensing and scaling circuit
- Control circuit (VM or CPM)
- Gate driver circuit
- Power circuit

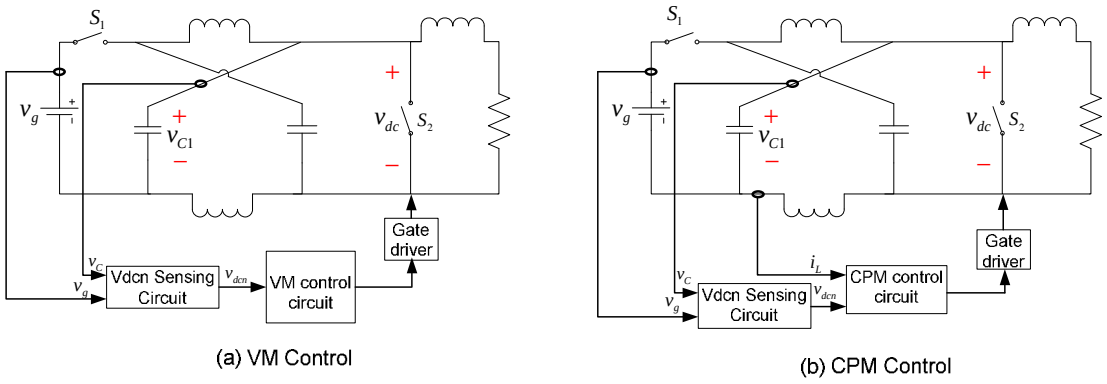


Figure 7.1 Experimental block diagrams of both VM and CPM controlled ZSC

The schematic representation of the sensing and scaling circuit is shown in Figure 7.2. The input voltage (v_g) and the capacitor voltage (v_c) are measured from the power circuit. The measured voltages are scaled down to suitable values for op-amp operation. OPA177GP is used as a subtracter to obtain the reproduced peak dc-link voltage ($v_{dcn} = 2v_c - v_g$).

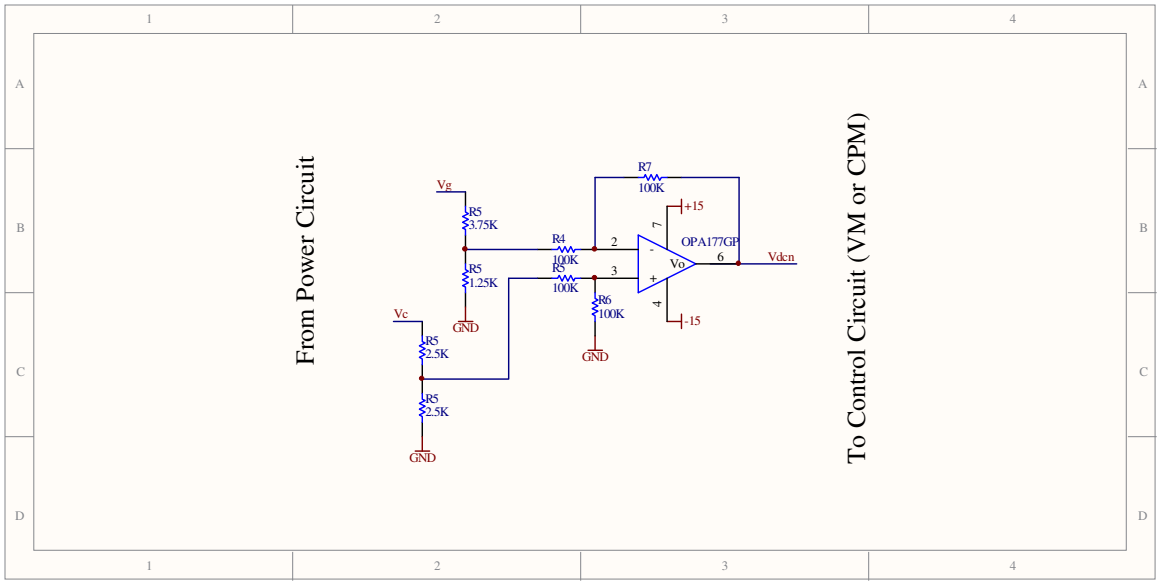


Figure 7.2 Sensing and scaling circuit

Figure 7.3 shows the implemented VM control circuit. The reproduced peak dc-link voltage (v_{dcn}) obtained from the sensing and scaling circuit is received as an input to the error amplifier inside the PWM control chip (TL594). This chip produces a 5V reference signal which can be used for obtaining the error signal for the output voltage regulation. The error signal is compensated using an R-C network built around the error amplifier as shown in Figure 7.4 whose transfer function is

$$\frac{\hat{V}_{comp}}{\hat{V}_{dcn}} = \frac{Cz}{C_P}\frac{(s+1/R_1C_Z)(s+1/R_fC_f)}{s(s+1/R_f(C_fC_p/(C_f+C_p)))} \tag{7.1}$$

Based on the VM controller designed in Chapter V and given in Eq. (5.8), the circuit parameters of the VM compensator have been selected as shown in Table 7.1. Maximum shoot-through duty cycle has been limited to 40% using the Dead Time Control (DTC)

feature of TL594. The output PWM signals are sent to the gate driver circuit through a BJT transistor inverter.

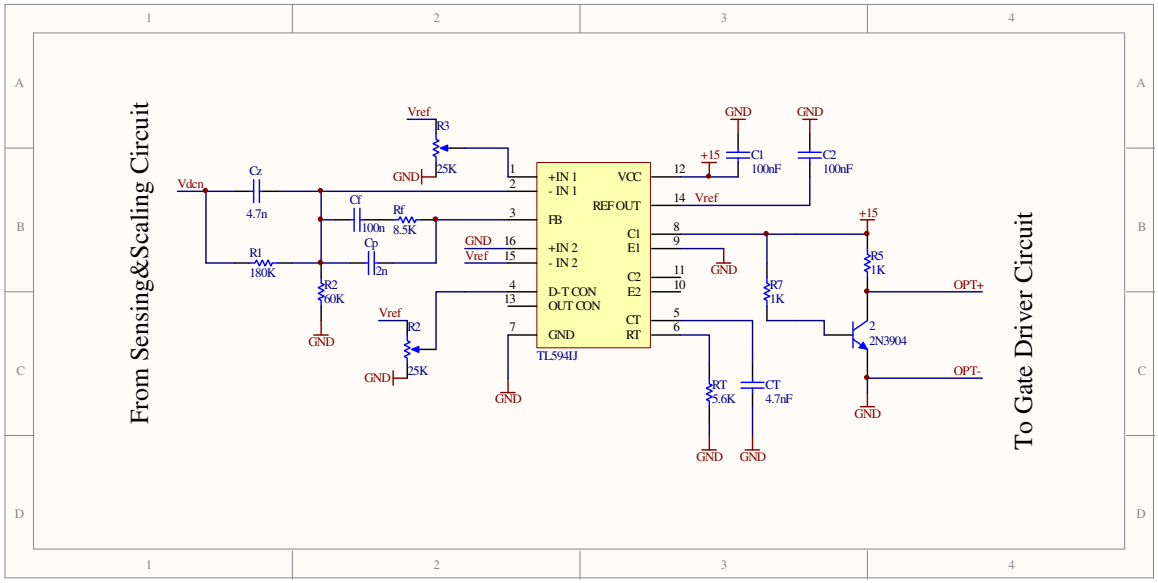


Figure 7.3 VM control circuit

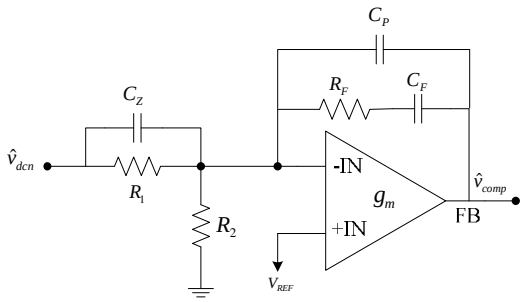


Figure 7.4 PID compensator used in VM control circuit

Table 7.1 Circuit parameters used for the VM compensator

R_1	R_2	C_z	R_f	C_f	C_p
180KΩ	60KΩ	4.7nF	8.5KΩ	100nF	2nF

Figure 7.5 shows the implemented CPM control circuit. In CPM mode, VM control circuit is replaced with this circuit. Similar to the VM control circuit, the reproduced peak dc-link voltage ($v_{dcn} = 2v_c - v_g$) coming from the sensing and scaling circuit is received as an input to the error amplifier inside the CPM PWM chip (UC2844). A 2.5V reference signal is produced internally by UC2844 which is compared to the measured v_{dcn} . The error is compensated through a PI compensator network built around the error amplifier which is shown in Figure 7.6 and Eq. (7.2). The compensator network parameters in Table 7.2 are selected based on the designed CPM controller given in Eq. (6.9). The compensated error signal is used as the current command for the inner inductor current loop. The inductor current is sensed using LEM LA-55P hall sensor. After scaling and filtering, the sensed current is received as an input by UC2844 and compared to the current command which produces the gating signals at the output. Those gating signals are sent to the gate driver circuit.

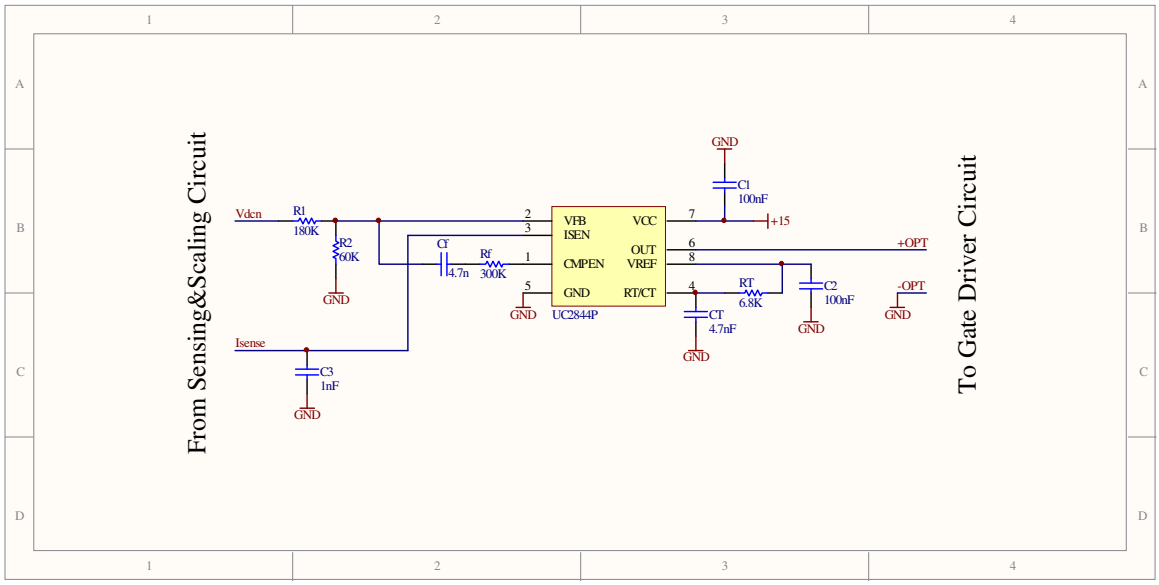


Figure 7.5 CPM control circuit

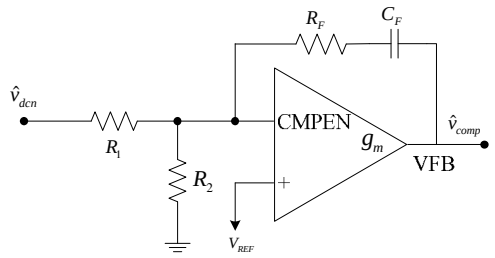


Figure 7.6 PI compensator used in CPM control circuit

$$\frac{\hat{v}_{comp}}{\hat{v}_{dcn}} = \frac{R_f}{R_1}\frac{(s+1/R_fC_f)}{s} \tag{7.2}$$

Table 7.2 Circuit parameters used for the CPM compensator

R_1	R_2	R_f	C_f
180KΩ	60KΩ	300KΩ	4.7nF

Figure 7.7 shows the gate driver circuit together with the power circuit. The PWM signals coming from the control circuit (VM or CPM) are isolated through an optocoupler (TLP550) for separating the control and power grounds. UC3705 is used as the MOSFET driver. The power circuit components are selected to minimize the parasitic effects. Switches S1 and S2 are realized using low voltage drop 40CPQ080 schottky rectifier and low on resistance IRF2807 MOSFET, respectively. Table 7.3 shows the component non-idealities and Figure 7.8 shows the picture of the experimental setup.

Table 7.3 Component non-idealities for simulation and experiments

$ESR(L)$	$ESR(C)$	$R_{on}(S2)$	$V_D(S1)$
0.023Ω	0.11Ω	0.013Ω	$0.61V$

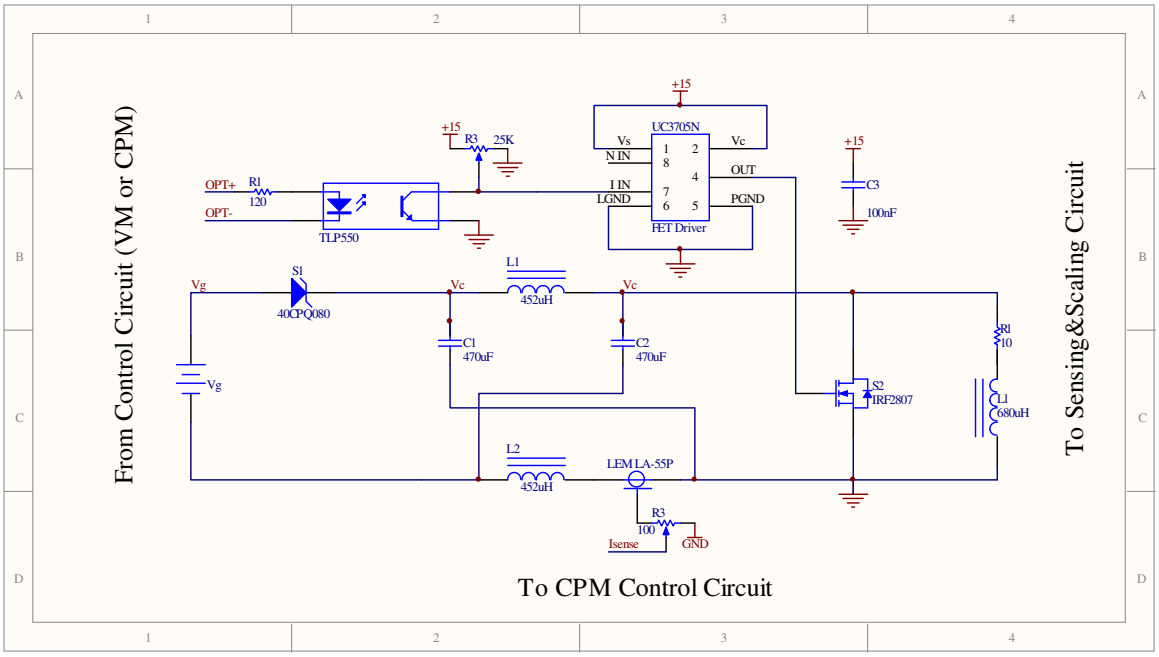


Figure 7.7 Power and gate driver circuit

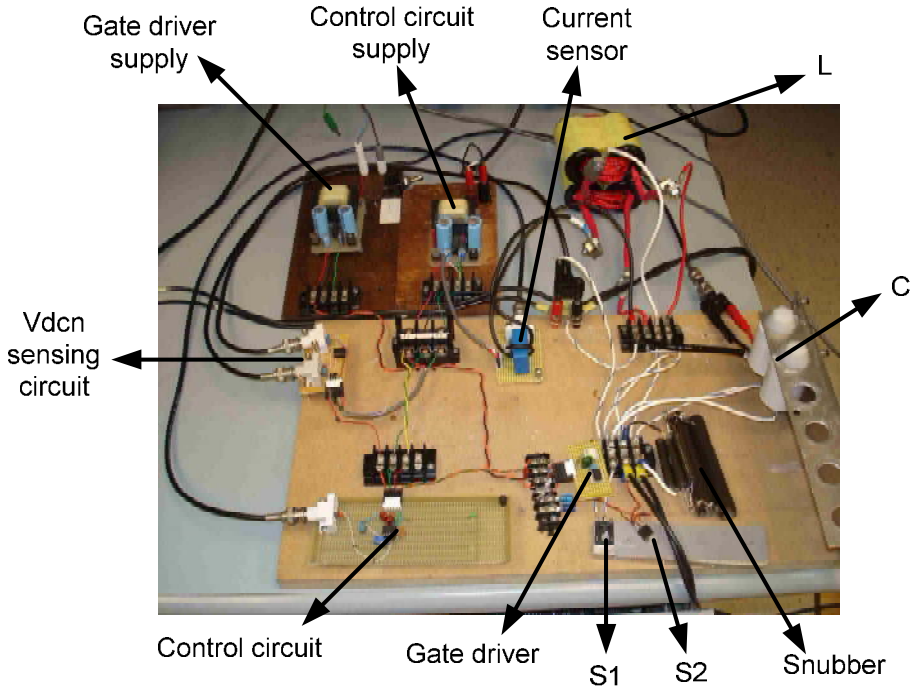


Figure 7.8 Picture of the experimental setup

7.3 Steady State Operation Results

Steady state operation of the ZSC is verified through both simulation and experiments. The experimental setup shown in Figure 7.1 is operated as open loop and critical waveforms are captured. Also the same circuit including the non-idealities given in Table 7.3 is simulated using MATLAB/SIMULINK and the same waveforms with the same scaling are obtained for comparison with the experimental results. Also, calculations are carried out using the ideal circuit voltage and current conversion ratios. Figure 7.9 shows the steady state waveforms of the dc-link voltage (V_{dc}). In Figure 7.9(b) the experimental waveform of V_{dc} is given together with the gating signal. When the gating signal is a non-zero value, the parallel switch (S_2) in Figure 7.1 becomes on and shorts the dc-link and the load. When the gating signal becomes zero, S_2 becomes off and a non-zero dc-link voltage appears across the load. The peak dc-link voltage is boosted to $36.2V$ from a $20V$ input voltage (V_g). The theoretical calculation of peak V_{dc} based on the ideal circuit agrees well the results ($1/(1-2D)V_g = 37.03V$), where $D = 0.23$.

Figure 7.10 shows the steady state capacitor voltage (V_C) waveforms. The effect of the non-idealities can be seen on the waveforms where a voltage drop occurs on the capacitor ESR producing a small square wave on top of the V_C waveform. From the ZSC circuit in Figure 7.1, it can be observed that V_C is equal to the average of V_{dc} since the average value of the inductor voltage over a switching period is zero. Calculation of V_C

can be done using the calculated peak V_{dc} ($V_C = (1-D)V_{dc} = 28.5V$). The measured value of V_C is $27.2V$.

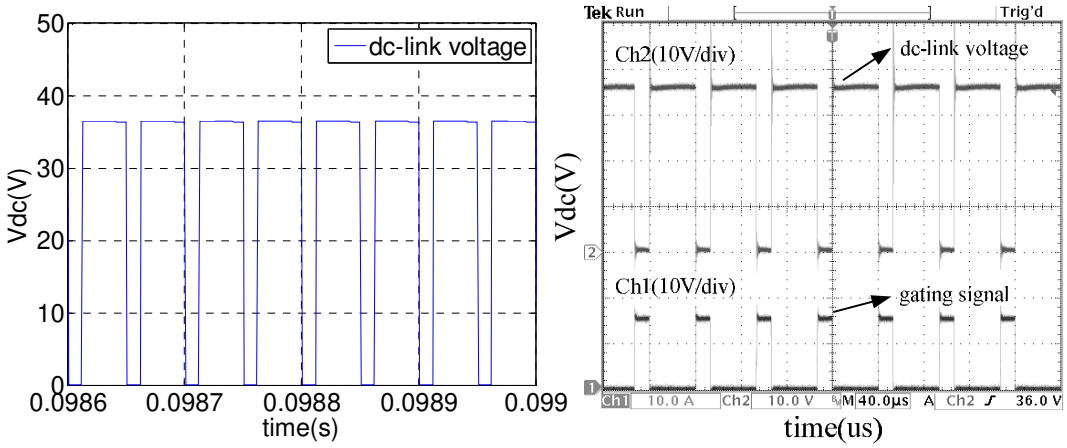


Figure 7.9 DC-link voltage in steady state

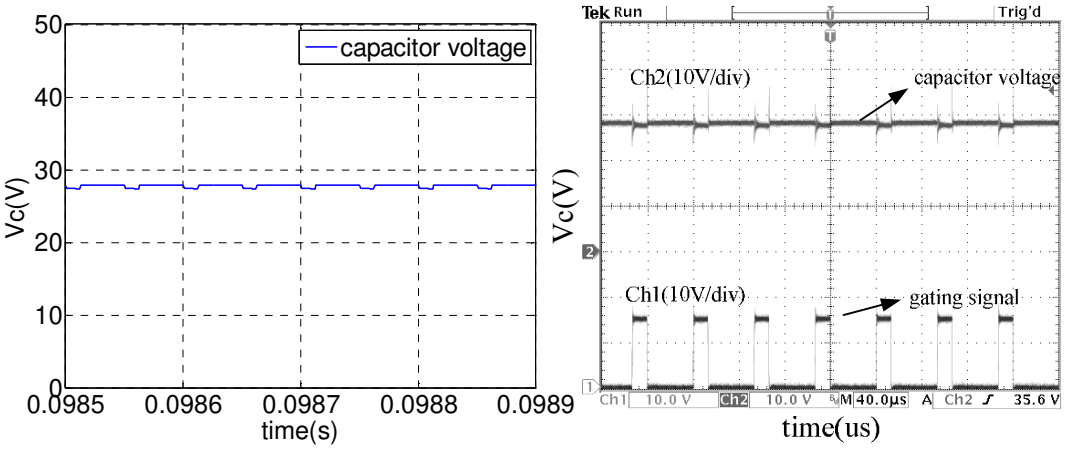
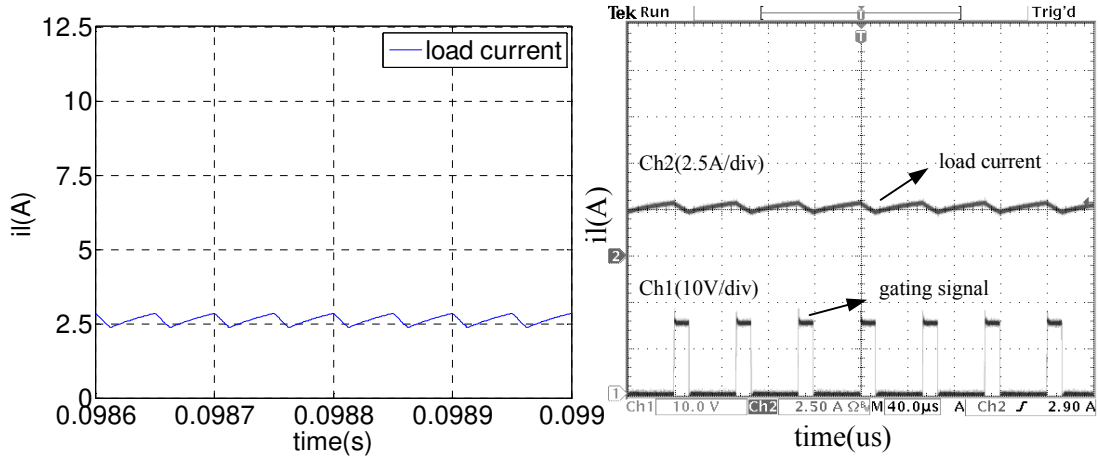


Figure 7.10 Capacitor voltage in steady state

Figure 7.11 shows the simulation and experimental waveforms of the load current (i_l). Together with the gating signal it can be observed that when S_2 is on, i_l decreases

since the load sees zero voltage. Similarly when S_2 is off, i_l increases due to the non-zero dc-link voltage. The average value of i_l can be calculated based on the ideal circuit using the calculated value of V_C ($i_l = V_C / R_l = 2.85A$), where R_l is the load resistance with a nominal value of 10Ω. The measured value of i_l is $2.72A$.



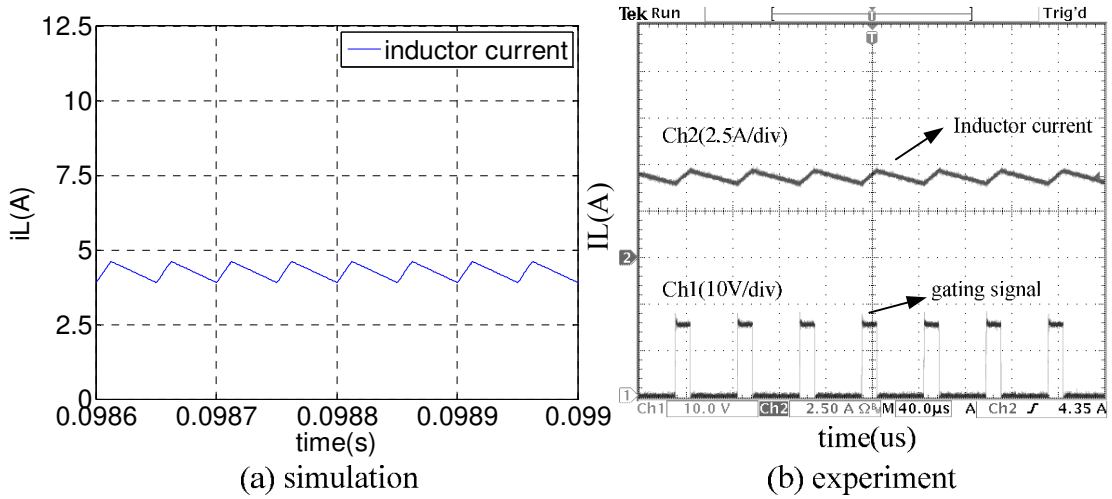
(a) simulation (b) experiment

Figure 7.11 Load current in steady state

Figure 7.12 shows the steady state inductor current (I_L) waveforms. When the parallel switch S_2 is on, the Z-source capacitors charge the inductors and I_L increases. When S_2 is off, the energy stored in the inductors discharges over the load decreasing I_L. The steady state relation between I_L and i_l can be obtained as: $I_L = (1-D)/(1-2D)i_l$, which is based on ideal components. Using this relation, I_L can be calculated as $4.06A$ where it is measured as $4.3A$ from the results.

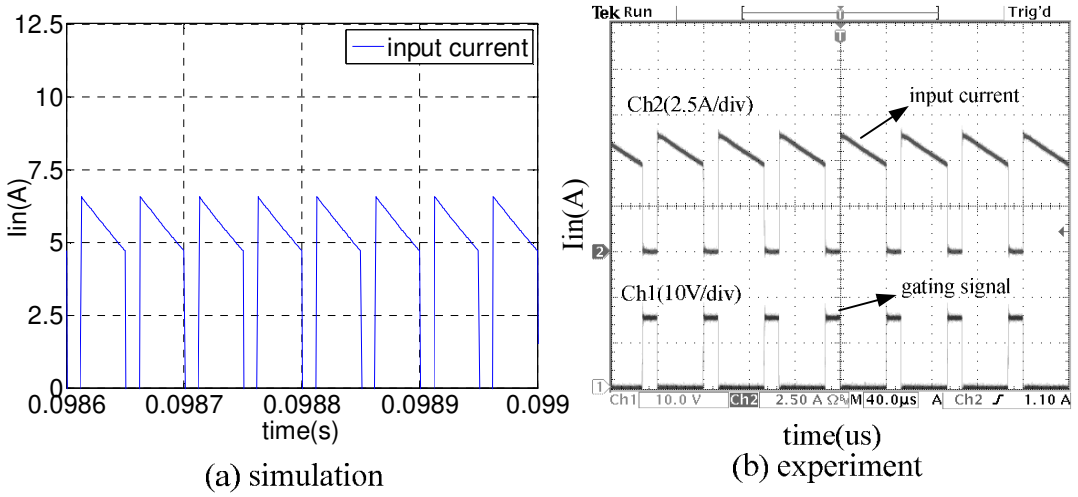
Figure 7.13 shows the simulated and experimental waveforms of the input current (I_{in}). I_{in} has a pulsating nature due to the input diode (S_1). When a non-zero gating

signal is applied to S_2 as shown in Figure 7.13(b), S_1 becomes reverse biased and when S_2 is off, S_1 becomes forward biased. The average value of I_{in} is equal to the average value of I_L, since the average value of the current going into the capacitor is zero in steady state. So $I_{in} = I_L/(1-D) = 5.28$. From the experimental waveform I_{in} is measured as $5.7A$.



(a) simulation (b) experiment

Figure 7.12 Inductor current in steady state



(a) simulation (b) experiment

Figure 7.13 Input current in steady state

It can be observed from the steady state waveforms of the ZSC that the simulation of the non-ideal circuit gives the same results with the experiments. This shows that the ZSC operates as expected in the theoretical analysis. Due to the high current and noisy nature of power converters, generally it is hard to obtain exact matching of the simulation and experimental results.

7.4 VM and CPM Control Results

After obtaining the steady state results, feedback loops has been closed around the power circuit for both VM and CPM controls as in Figure 7.1. The closed loop controllers designed in Chapters V and VI for both VM and CPM controlled cases has been built around the respective PWM chips as explained in Section 7.2. In order to verify the effectiveness of the designed controllers using the proposed control method, line and load disturbance rejection performance of the VM and CPM controlled ZSC is tested using both simulation and experiments. The disturbances are produced using mechanical single pole double throw (SPDT) switches. For the case of line disturbance, the input voltage (V_g) is increased by 20% with a step change from $20V$ to $24V$ as shown in Figure 7.14, where the peak dc-link voltage is regulated around $36V$. An input capacitor is employed to maintain the continuity of the input voltage. The load disturbance is produced by decreasing the load resistance from 12Ω to 7Ω.

Figure 7.15 shows simulation (left) and experimental (right) results when the VM controlled ZSC is subjected to a line disturbance. A 10% overshoot is observed during the transient stage. The reason for the overshoot is the RHP zero in G_{vnd} [9], which makes

it difficult to get enough phase margin for a response without any overshoot. Figure 7.16 shows a better line disturbance rejection for CPM without any significant overshoot. In CPM, since the order of the system is reduced by one, it is easier to get a higher phase margin than in VM control case [7]. Figure 7.17 shows the detailed pictures of the two line disturbance cases. It can be observed that the step changes in the input voltage include certain dynamics due to the practical limitations such as the mechanical SPDT switch and non-ideal source. Those dynamics may also have contributed to the dc-link voltage transient responses for both cases.

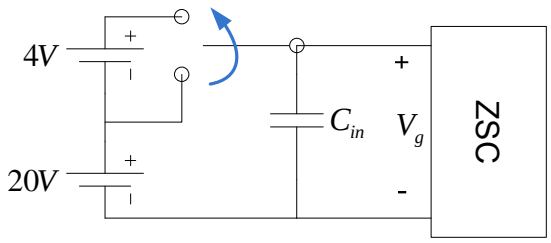
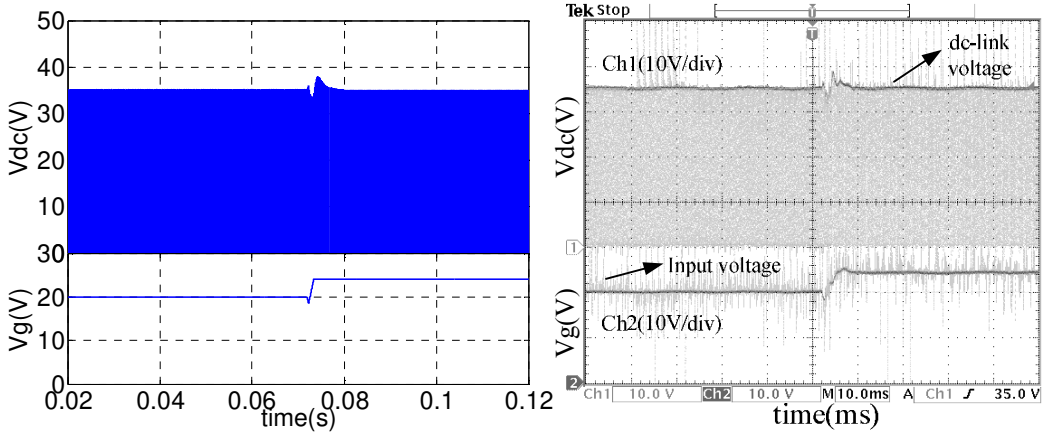
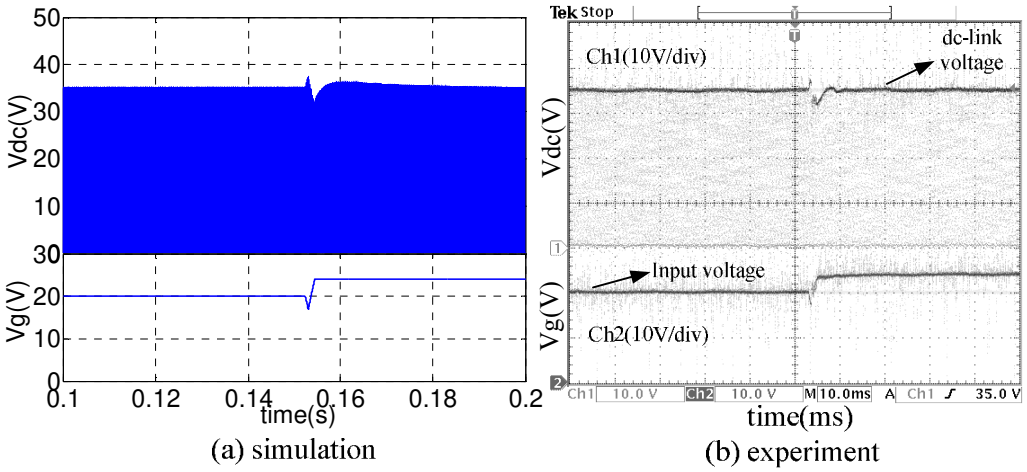


Figure 7.14 Realization of line disturbance using SPDT switch



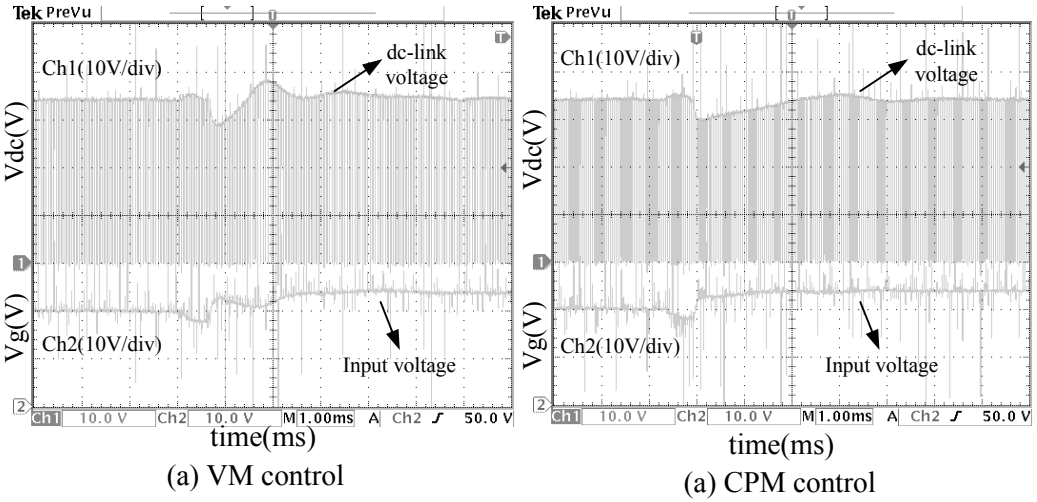
(a) simulation (b) experiment

Figure 7.15 Line rejection performance of VM controlled ZSC (20% increase in V_g)



(a) simulation (b) experiment

Figure 7.16 Line rejection performance of CPM controlled ZSC (20% increase in V_g)

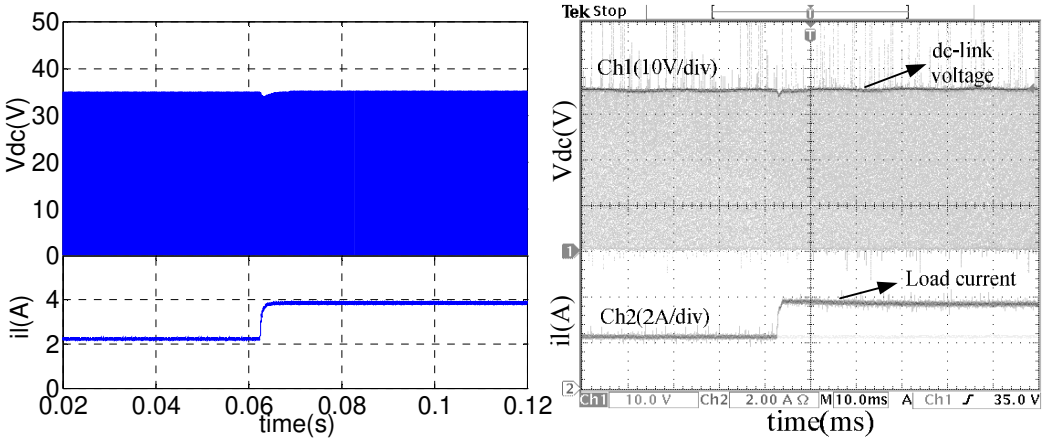


(a) VM control (a) CPM control

Figure 7.17 Detailed pictures of line disturbance rejection

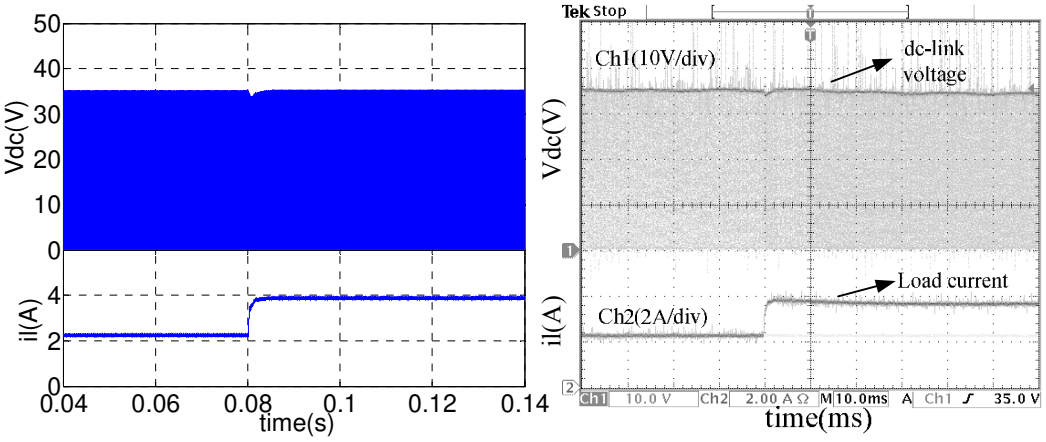
Figure 7.18 and Figure 7.19 show the load disturbance rejection case for VM and CPM controls, respectively. In this case both control methods show similar dynamic behaviors with very good transient responses. This can be explained by the definition of the dc-link voltage (v_{dc}). The peak value of v_{dc} was shown to be $2v_C - v_g$ in Chapter III. It can be observed from this expression that any change in input voltage has a direct

effect on the peak of v_{dc}, where changes in the load does not have a direct effect. Load changes are compensated by changing the capacitor voltage (v_C) to regulate the peak of v_{dc}, regarding that the input voltage (v_g) is constant. So it is easier for the controller to compensate for the load disturbances compared to the line disturbances.



(a) simulation (b) experiment

Figure 7.18 Load rejection performance of VM controlled ZSC (70% increase in i_l)



(a) simulation (b) experiment

Figure 7.19 Load rejection performance of CPM controlled ZSC (70% increase in i_l)

7.5 Summary

This chapter is dedicated to the simulation results and experimental verifications. The experimental setup is explained through the schematics of each circuit. The steady state operation of the ZSC is verified by comparing the simulation and experimental results. The results are also compared to the calculations based on the ideal voltage and current conversion ratios and the small deviations are interpreted considering the circuit non-idealities. After having the steady state results, the closed loop controllers have been implemented for the ZSC in both VM and CPM. In order to evaluate the performance of the VM and CPM controlled ZSC, line and load disturbances are applied. The experimental results and the non-ideal circuit simulation results showed to be comparable. It is observed from the results that the CPM control gives better line disturbance rejection than the VM control where both methods gave successful results in load disturbance rejection.

CHAPTER VIII

CONCLUSIONS AND FUTURE WORK

8.1 Conclusions

Systems involving power converters are becoming more common in applications like alternative energy sources and hybrid electric vehicles (HEV). Efficiency, low cost and reliability are major objectives for power electronics designers. Classical power converter topologies still give satisfactory results and their performances are being improved by advanced control techniques. New topologies in power conversion are also being introduced and give better results in some applications. The Z-source converter (ZSC) is a new power conversion topology that is very promising in power conditioning of alternative energy sources and applications like HEVs and utility interfacing. Unique buck and boost capability of the ZSC allows a wider input voltage range and eliminates the usage of DC/DC boost stage which improves overall efficiency. Also, the shoot-through state is allowed and the system reliability is improved.

This research is a continuation of the effort on modeling and control of the ZSC that has been achieved so far in the literature. The accuracy of the small signal model derived in the literature has been verified by comparing the simulation results of the

small signal and switching circuits. Additionally, critical time response parameters are calculated using dominant pole-zero approximation and compared to their measured counterparts from the simulated switching and small signal circuit waveforms.

In this research a new method for controlling the peak value of the dc-link voltage is proposed and its validity is verified. The proposed control method is based on reproducing the peak dc-link voltage from the measured values of the capacitor voltage and the input voltage and controlling the peak dc-link voltage based on this reproduced voltage without direct measurement. The control law and the new transfer functions for the proposed control method are derived based on the small signal model and verified by comparing the simulated waveforms of both the small signal and switching circuits. Also, a small signal model of the ZSC is derived for current programmed mode (CPM) operation. The proposed method is applied to both voltage mode (VM) and CPM controlled ZSC. The controllers are designed for both cases. An experimental setup is implemented including both the open loop ZSC circuit and the VM and CPM control circuits. The operation of the ZSC and the effectiveness of the designed controllers using the proposed control method are verified by comparing the simulation and experimental results. The steady state operation of the ZSC is found as expected regarding to the theoretical analysis. CPM control gave better line disturbance rejection compared to the VM controlled case. Both VM and CPM controls gave very good dynamic response for the load disturbance rejection case. In all cases including the steady state operation, simulation and experimental results showed to be comparable.

8.2 Future Work

The following research is suggested for the ZSC as a continuation of this research.

- In this research the experimental verifications are carried out using the simplified ZSC. The Z-source inverter (ZSI) can be implemented by replacing the parallel switch with an inverter bridge.

- A fuel cell system can be used as the input source and effectiveness of the proposed control method can be verified.

- The small signal model used in this research assumed ideal components. A new model including the non-idealities can be derived for more accurate transfer functions.

- The dynamic model of the ZSC can be implemented in discrete time and a DSP based digital controller can be designed which may give more freedom in choosing the compensator parameters.

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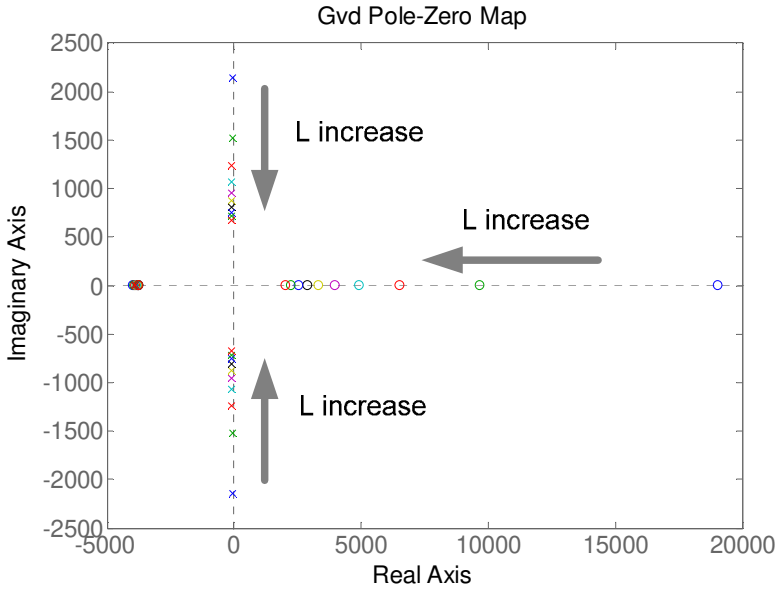
APPENDICES

APPENDIX A

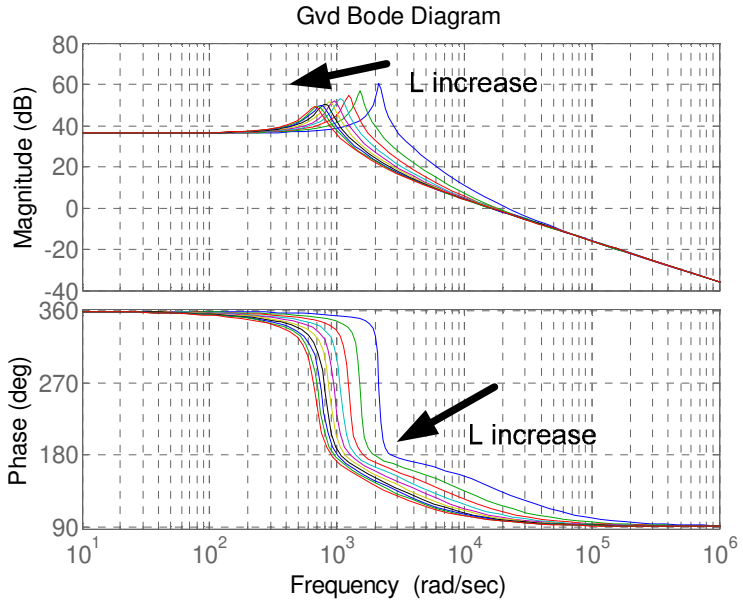
PARAMETER SWEEPING

In Chapter IV, a small signal averaged model of the ZSC is derived and its validity is verified by comparing the simulation waveforms of both the switching circuit and the averaged model. It was shown in Figure 4.4 - Figure 4.7 that certain dynamics exist associated with the converter state variables. It can be seen from the converter transfer functions given in Eqs. (4.19)-(4.22) that these dynamics are related to circuit parameters such as Z-source inductance (L), Z-source capacitance (C), load resistance (R_l), load inductance (L_l) and shoot-through duty cycle (D). However, it is hard to distinguish how each parameter affects the converter dynamics. A method commonly used to see how variations in circuit elements or changes in operating points can affect system transfer functions and converter transient behavior is parameter sweeping [8]-[9]. In this section, pole-zero maps as well as magnitude and phase plots of the control-to-capacitor voltage transfer function ($G_{vd}(s)$) of the ZSC given in Eq. (4.19) are analyzed based on sweeping different circuit parameters of the ZSC. Since $G_{vd}(s)$ is used for controller design, it is selected for parameter sweep analysis. However other transfer functions could be analyzed using the same method. The circuit parameters given in Table 4.1 are used.

Figure A.1 shows the pole-zero map and Bode diagrams of $G_{vd}(s)$ when the Z-source network inductance value is swept from $100\mu H$ to $1000\mu H$ with $100\mu H$ steps. $G_{vd}(s)$ expression given in Eq. (4.19) has a second order numerator and a third order denominator implying two zeros and three poles. From the pole-zero map, it can be seen that $G_{vd}(s)$ has a complex conjugate pole pair at low frequencies. Also a pole, a Right Half Plane (RHP) zero and a Left Half Plane (LHP) zero are observed at a higher frequency compared to the converter natural frequency. The locations of the LHP pole and LHP zero seems very close. Arrows on Figure A.1(a) show the movement of converter poles and zeros as the Z-source network inductance is swept through the above mentioned range of values. As the inductance increases the complex conjugate poles and the RHP zero approach the origin. Magnitude and phase plots in Figure A.1(b) confirm the decrease in resonant frequency. From the phase plot the effect of the decrease in RHP zero frequency is seen as a drop in the available phase at frequencies higher than the resonant frequency. Magnitude plot shows the increase in damping as the inductance increases. Figure A.2(a) shows the pole-zero map of $G_{vd}(s)$ when the Z-source network capacitance is swept from $100\mu F$ to $1000\mu F$ with $100\mu F$ steps. It can be observed that $G_{vd}(s)$ zeros are not affected from the change in capacitance value but the complex conjugate poles move towards the origin which means the converter natural frequency decreases. Also from the magnitude bode diagram in Figure A.2(b) it can be seen that the damping factor slightly decreases as the capacitance is increased. Selection of inductor and capacitor values is important in ZSC design. Although large values of these elements may give better ripple performance, this may slow down the system response and make the controller design harder due to the RHP zero.

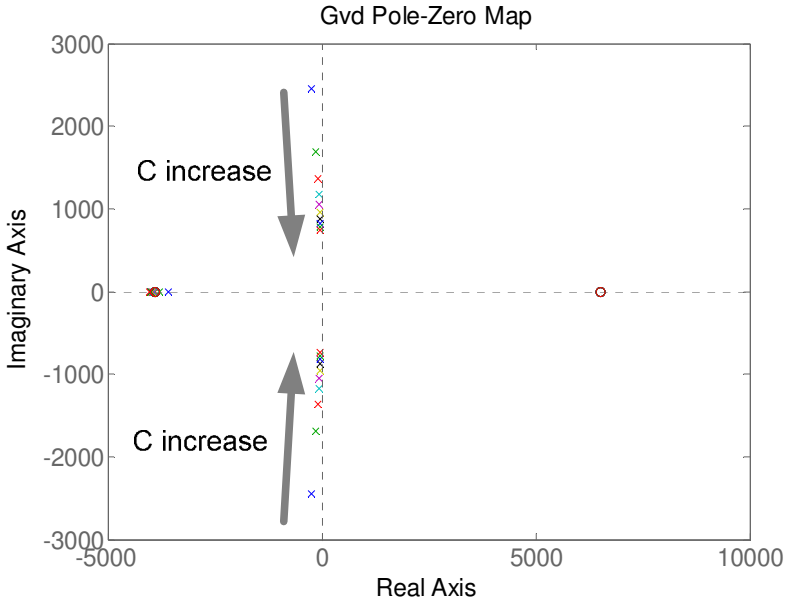


(a) pole-zero map

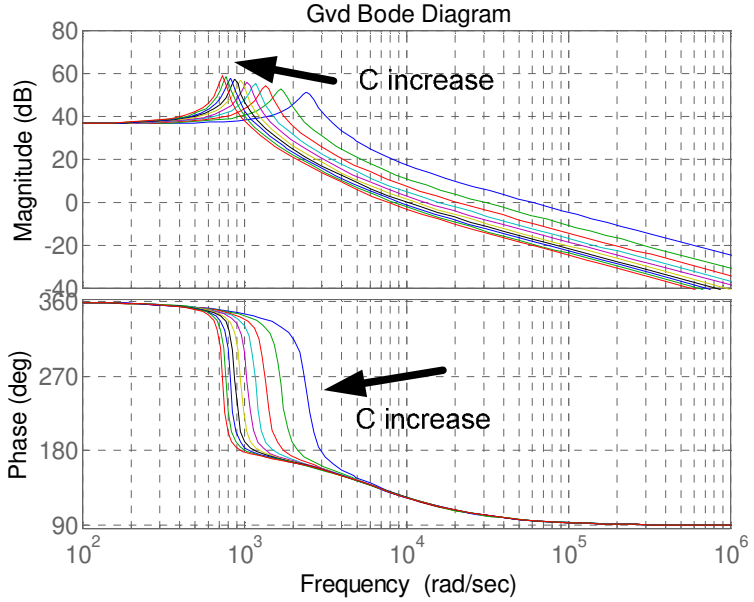


(b) Bode plots

Figure A.1 Effect of inductor variation on ZSC dynamics ($100\mu H - 1000\mu H$)



(a) pole-zero map



(b) Bode plots

Figure A.2 Effect of capacitance variation on ZSC dynamics ($100\mu F - 1000\mu F$)

Figure A.3 shows the pole-zero map and Bode diagrams of $G_{vd}(s)$ when the shoot-through duty cycle D is swept from 10% to 40% with 3% steps. It can be observed that the natural frequency decreases as D is increased. Also the RHP zero approaches to the origin which makes the non-minimum phase effect more severe. It is known that there is trade-off between close-loop output responses and the zero direction of the open-loop system. The trade off becomes severe if the RHP zero is close to the origin. So, the achievable control performance is degraded as the RHP zero moving closer to the origin [8]. So, it is important that the effect of the shoot-through duty cycle as well as other circuit parameters to RHP zero direction to be taken into consideration in both converter power stage and controller design.

It is known that change in load parameters also affects the dynamic behavior of a power converter [2]. Parametric sweep of load variables helps designers to see converter characteristics at different loading scenarios. This can be seen from Figure A.4 and Figure A.5 where the load resistance (R_l) is swept between $4\Omega - 30\Omega$ with 3Ω steps and load inductance (L_l) is swept between $200\mu H - 2000\mu H$ with $200\mu H$ steps. Sweeping R_l effects the zeros and the high frequency pole of $G_{vd}(s)$ such that an increase in R_l moves them away from the origin. It can be observed form Figure A.4 (b) that the natural frequency does not change when R_l is changed. Increasing L_l turns the load into a current source. From Figure A.5 it can be observed that as L_l increases, the LHP zero and the high frequency pole approach to the origin. However, the locations of the zero and the pole on the LHP stay close to each other which cancels their effects. Also, the change in L_l does not affect the critical system parameters such as system frequency,

damping and RHP zero location. As a result ZSC dynamics is not affected by L_l significantly.

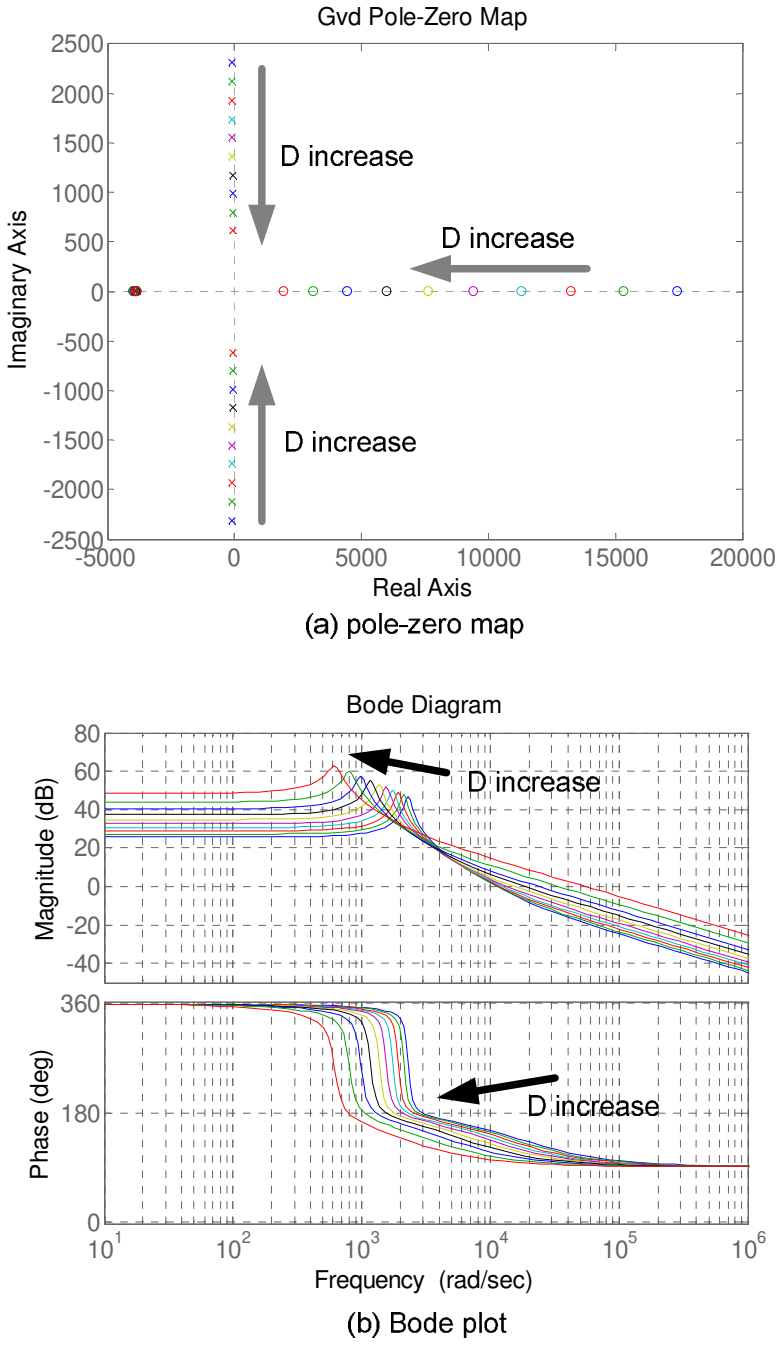
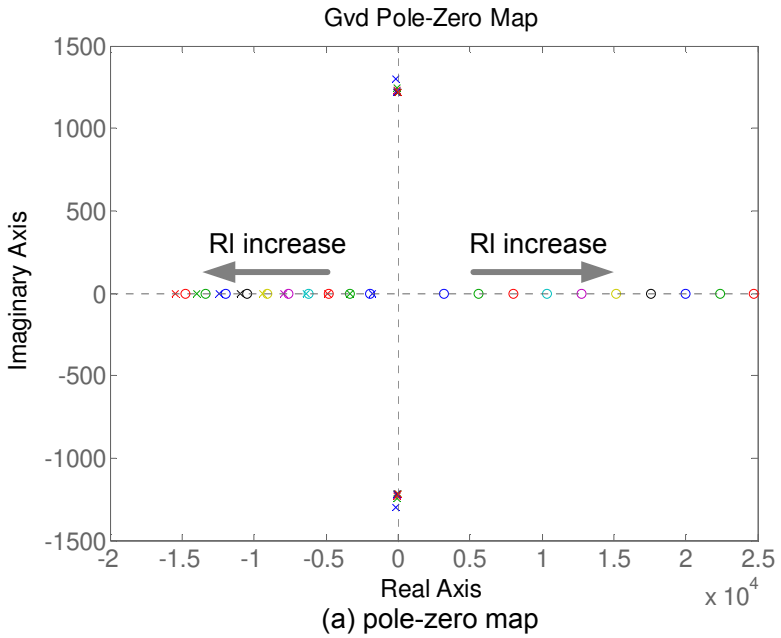
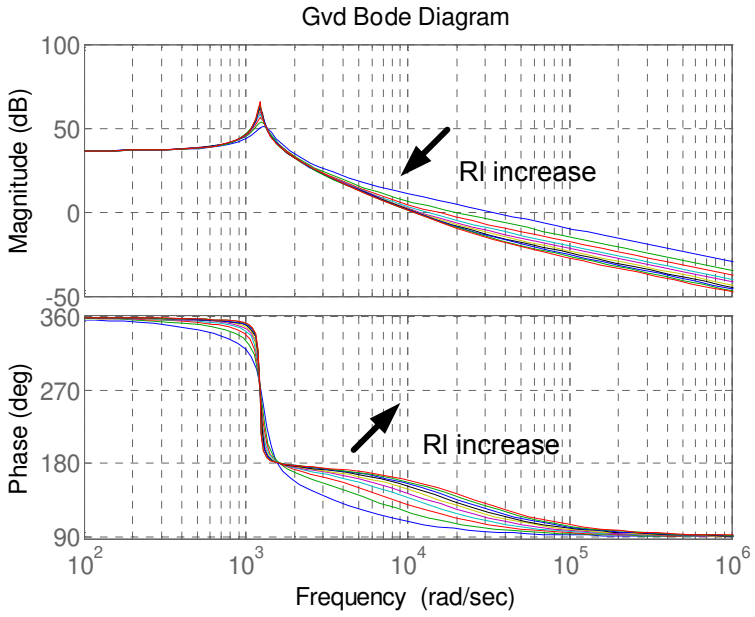


Figure A.3 Effect of shoot-through duty cycle variation on ZSC dynamics (10% – 40%)

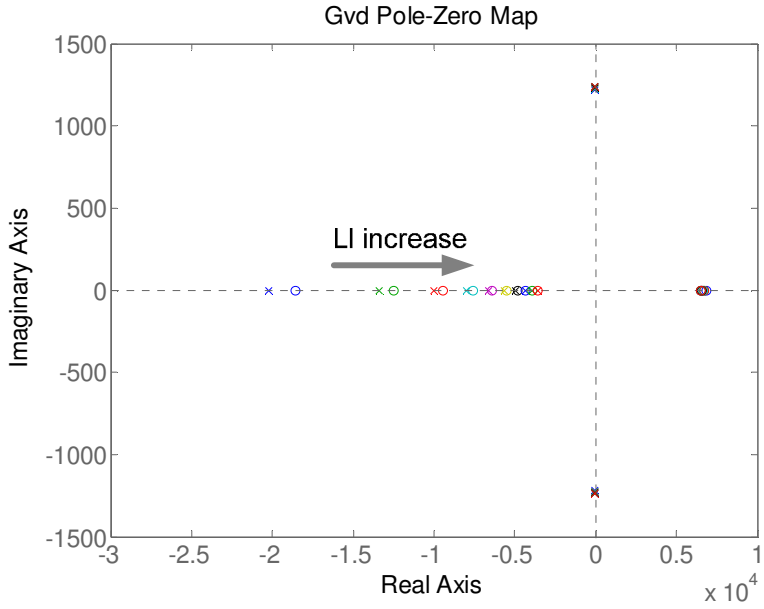


(a) pole-zero map

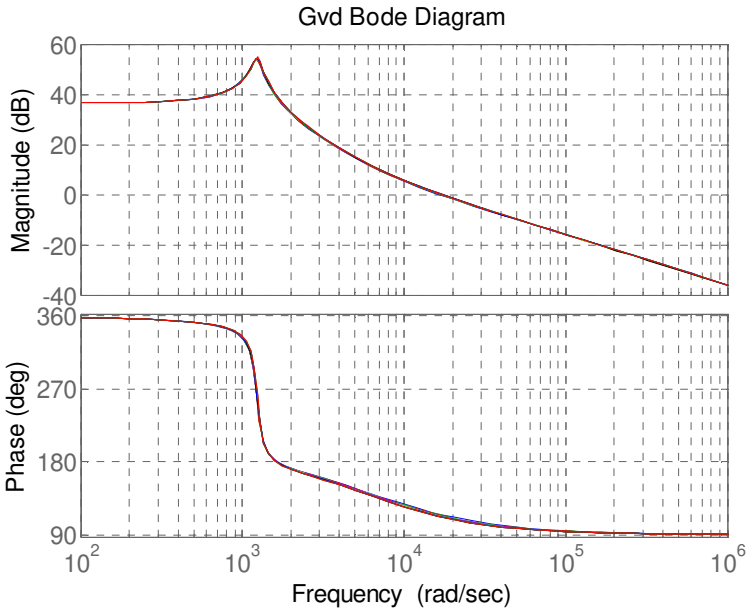


(b) Bode plot

Figure A.4 Effect of load resistance variation on ZSC dynamics ($4\Omega - 30\Omega$)



(a) pole-zero map



(b) Bode plots

Figure A.5 Effect of load inductance variation on ZSC dynamics ($200\mu H - 2000\mu H$)

APPENDIX B

LOW Q APPROXIMATION

The analysis in Appendix A showed that the dynamics associated with ZSC is affected by the circuit parameters. However the poles and zeros of the transfer function given in (4.19) are not separated, i.e. it is hard to distinguish which circuit parameter affects which pole or zero location. This section gives an approximate expression for control-to-capacitor voltage transfer function ($G_{vd}(s)$) of the ZSC to provide a clear picture of the effects of circuit parameters to the pole and zero locations.

It is explained in [2] that the low Q approximation can be used to factor a second order expression into its roots provided that the roots are real. For instance, Eq. (B.1) shows the standard normalized form of a second order system, where Q is the quality factor and ω_o is the natural frequency of the second order system.

$$G(s) = \frac{1}{1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2} \tag{B.1}$$

The roots of the denominator polynomial can be expressed as in Eq. (B.2),

$$\omega_1 = \left(\frac{\omega_0}{Q}\right)\frac{1-\sqrt{1-4Q^2}}{2} \qquad \text{or} \qquad \omega_1 = \frac{\omega_0 Q}{F(Q)}$$
$$\omega_2 = \left(\frac{\omega_0}{Q}\right)\frac{1+\sqrt{1-4Q^2}}{2} \qquad\qquad \omega_2 = \frac{\omega_0}{Q}F(Q) \tag{B.2}$$

where $F(Q) = \frac{1+\sqrt{1-4Q^2}}{2}$. Note that, if $Q << 0.5$, then $4Q^2 << 1$ resulting in two separate real roots as in Eq. (B.3) [2],

$$\omega_2 = \frac{\omega_0}{Q} \quad and \quad \omega_1 = Q\omega_0 \tag{B.3}$$

The low Q approximation can be generalized to obtain approximate roots of an arbitrary degree polynomial. For instance, we need to factor out Eq. (B.4) into Eq. (B.5),

$$P(s) = 1 + a_1 s + a_2 s^2 + ... + a_n s^n \tag{B.4}$$

$$P(s) = (1+\tau_1 s)(1+\tau_2 s)...(1+\tau_n s) \tag{B.5}$$

In physical systems, the coefficients $a_1,...,a_n$ are real, but the time constants $\tau_1,...,\tau_n$ may be real or complex. If the time constants are well separated in value then approximate analytical expressions can be driven as,

$$\begin{aligned}
a_1 &= \tau_1 + \tau_2 + ... + \tau_n \\
a_2 &= \tau_1(\tau_2 + ... + \tau_n) + \tau_2(\tau_3 + ... + \tau_n) + ... \\
a_3 &= \tau_1\tau_2(\tau_3 + ... + \tau_n) + \tau_2\tau_3(\tau_4 + ... + \tau_n) + ... \\
&\vdots \\
a_n &= \tau_1\tau_2\tau_3...\tau_n
\end{aligned} \tag{B.6}$$

An approximate solution to Eq. (B.6) can be proposed provided that, $\tau_1,...,\tau_n$ are real and well separated in value. If the time constants arranged in decreasing order of magnitude,

$$|\tau_1| >> |\tau_2| >> ... >> |\tau_n| \tag{B.7}$$

then the expressions in Eq. (B.6) are dominated by the first terms [2],

$$\begin{aligned} a_1 &\approx \tau_1 \\ a_2 &\approx \tau_1\tau_2 \\ a_3 &\approx \tau_1\tau_2\tau_3 \\ &\vdots \\ a_n &\approx \tau_1\tau_2\tau_3...\tau_n \end{aligned} \tag{B.8}$$

and expressions for each time constant can be driven as in Eq. (B.9), which gives approximate expressions for each root of Eq. (B.5). So Eq. (B.5) can be rewritten as in Eq. (B.10).

$$\begin{aligned} \tau_1 &\approx a_1 \\ \tau_2 &\approx \frac{a_2}{a_1} \\ \tau_3 &\approx \frac{a_3}{a_2} \\ &\vdots \\ \tau_n &\approx \frac{a_n}{a_{n-1}} \end{aligned} \tag{B.9}$$

$$P(s) \approx (1+a_1 s)\left(1+\frac{a_2}{a_1}s\right)\left(1+\frac{a_3}{a_2}s\right)...\left(1+\frac{a_n}{a_{n-1}}s\right) \tag{B.10}$$

In the case where two of the roots are not well separated, the corresponding terms are left in quadratic form. For instance, when the first inequality in Eq. (B.7) does not hold for the first two terms, then the approximate expression for the polynomial can be found as,

$$P(s) \approx \left(1 + a_1 s + a_2 s^2\right)\left(1 + \frac{a_3}{a_2} s\right)...\left(1 + \frac{a_n}{a_{n-1}} s\right) \tag{B.11}$$

provided that Eq. (B.12) holds.

$$\left|\frac{a_2^{\,2}}{a_3}\right| >> \left|a_1\right| >> \left|\frac{a_3}{a_2}\right| >> ... >> \left|\frac{a_n}{a_{n-1}}\right| \tag{B.12}$$

Generalized low Q approximation can be applied to ZSC transfer functions to get the approximate locations of the poles and zeros provided that Eq. (B.12) holds. Eq. (4.19) shows the control-to-capacitor voltage transfer function which has a second order numerator and third order denominator. First this expression will be simplified using the steady state relations shown in Eqs. (4.13) - (4.15). Expressions in Eq. (B.13) are produced using Eqs. (4.13) - (4.15) for simplification of Eq. (4.19),

$$\begin{aligned} 2V_c - V_g &= \frac{1}{D' - D} V_g \\ -2I_L + I_l = -\frac{1}{D' - D} I_l &= -\frac{1}{D' - D}\frac{V_c}{R_l} = -\frac{D'}{(D' - D)^2}\frac{V_g}{R_l} \end{aligned} \tag{B.13}$$

The normalized expressions for the numerator and denominator of the control-to-capacitor voltage of the ZSC in Eq. (4.19) can be obtained as,

$$Num(s) = 1 + \left(-\frac{2L}{R_l}\frac{DD'}{(D'-D)^2} + \frac{L_l}{R_l} \right) s + \left(-\frac{D'}{(D'-D)^2}\frac{LL_l}{R_l^2} \right) s^2$$

$$Den(s) = 1 + \left(\frac{2D'L}{R_l} + \frac{L_l}{R_l} \right) s + \left(\frac{LC}{(D'-D)^2} \right) s^2 + \left(\frac{LL_lC}{R_l(D'-D)^2} \right) s^3 \tag{B.14}$$

For the numerator polynomial $Num(s)$ in Eq. (B.14), we can find an approximate expression using Eq. (B.4) and Eq. (B.5) for a second order expression. This requires Eq. (B.7) to hold which means $|a_1| >> \left|\frac{a_2}{a_1}\right|$ to be true. In order this to be true, Eq. (B.15) should hold,

$$\left| -\frac{2L}{R_l}\frac{DD'}{(D'-D)^2} + \frac{L_l}{R_l} \right| >> \frac{\left| -\frac{D'}{(D'-D)^2}\frac{LL_l}{R_l^2} \right|}{\left| -\frac{2L}{R_l}\frac{DD'}{(D'-D)^2} + \frac{L_l}{R_l} \right|} \tag{B.15}$$

Eq. (B.15) becomes true if $L >> L_l$ *and* $D' \not>> D$. This means the value of the inductor L in Z-network is much greater than the load inductance L_l and the active state duty ratio $D'(=1-D)$ is not much greater than the shoot-through duty ratio D. Considering those assumptions Eq. (B.15) reduces to,

$$\left| -\frac{2DD'}{(D'-D)^2}\frac{L}{R_l} \right| >> \left| \frac{1}{2D}\frac{L_l}{R_l} \right| \tag{B.16}$$

Obviously Eq. (B.16) is in compatible with the assumptions. So $Num(s)$ reduces to,

$$Num(s) = (1 + a_1 s)(1 + a_2 s) \tag{B.17}$$

where $a_1 = -\frac{2DD'}{(D'-D)^2}\frac{L}{R_l}$ and $a_2 = \frac{1}{2D}\frac{L_l}{R_l}$. Similarly the expression for $Den(s)$ can be approximated using Eq. (B.11) provided that Eq. (B.12) holds. This requires for a third order expression to satisfy,

$$\left|\frac{a_2^{\,2}}{a_3}\right| >> |a_1| >> \left|\frac{a_3}{a_2}\right| \tag{B.18}$$

where for this case,

$$\begin{aligned} a_1 &= \left(\frac{2D'^2 L}{R_l(D'-D)^2} + \frac{L_l}{R_l}\right) \\ a_2 &= \left(\frac{LC}{(D'-D)^2}\right) \\ a_3 &= \left(\frac{LL_lC}{R_l(D'-D)^2}\right) \end{aligned} \tag{B.19}$$

Inserting Eq. (B.19) in Eq. (B.18),

$$\frac{L}{L_l}R_lC\frac{1}{(D'-D)} >> 2D'\frac{L}{R_l} + \frac{L_l}{R_l} >> \frac{L_l}{R_l} \tag{B.20}$$

implies $L >> L_l$. So a_1 becomes,

$$a_1 = \left(\frac{2D'^2 L}{R_l(D'-D)^2}\right) \tag{B.21}$$

In this case the factorized expression for $Den(s)$ can be written as,

$$Den(s) = \left(1 + 2\frac{D'^2}{(D'-D)^2}\frac{L}{R_l}s + \frac{LC}{(D'-D)^2}s^2\right)\left(1 + \frac{L_l}{R_l}s\right) \tag{B.22}$$

Here we have a low-frequency quadratic pole pair that is well separated from a high frequency real pole. So approximate control-to-capacitor voltage transfer function (G_{vd}) becomes,

$$G_{vd} = \frac{V_c}{D'(D'-D)} \frac{\left(1-\frac{2DD'}{(D'-D)^2}\frac{L}{R_l}s\right)\left(1+\frac{1}{2D}\frac{L_l}{R_l}s\right)}{\left(1+2\frac{D'^2}{(D'-D)^2}\frac{L}{R_l}s+\frac{LC}{(D'-D)^2}s^2\right)\left(1+\frac{L_l}{R_l}s\right)} \tag{B.23}$$

If the assumption of $D' \not>> D$, which was made before, holds; then the LHP zero and high frequency pole suppress each others' effect, leaving a structure similar to a boost or buck-boost converter Eq. (B.24), where critical frequency response parameters are as in Eq. (B.25).

$$G_{vd}(s) = G_{do} \frac{1-\frac{s}{\omega_z}}{1+\frac{s}{Q\omega_o}+(\frac{s}{\omega_o})^2} \tag{B.24}$$

$$\begin{aligned} \omega_z &= \frac{R_l}{L}\frac{(D'-D)^2}{2DD'} \\ \omega_0 &= \frac{(D'-D)}{\sqrt{LC}} \\ Q &= \frac{(D'-D)}{2D'^2}R_l\sqrt{\frac{C}{L}} \end{aligned} \tag{B.25}$$

APPENDIX C

SIMULINK MODEL OF THE SMALL SIGNAL AND SWITCHING CIRCUITS