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Voltage Balancing Control of Hybrid Stacked Multicell Converters Based on Modified Phase-Shifted PWM

JIANZHONG ZHANG[1], (Senior Member, IEEE), SHUAI XU[2], (Member, IEEE), XING HU[1], (Student Member, IEEE), AND YAODONG ZHU[3]

[1]School of Electrical Engineering, Southeast University, Nanjing 210096, China
[2]School of Electrical Engineering and Electronic Information, Xihua University, Chengdu 610039, China
[3]School of Mechanical and Electrical Engineering, Jiaxing University, Jiaxing 314001, China

Corresponding author: Jianzhong Zhang (jiz@seu.edu.cn)

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ABSTRACT The hybrid stacked multicell converter (HSMC) is a competitive converter in the low-voltage high-efficiency applications. Proper modulation and voltage balancing control are important for the operation of the HSMC, which may ensure the HSMC to obtain high-quality output and low power losses. A hybrid phase-shifted PWM (PS-PWM) with the modified reference signal is developed for nine-level HSMC (9L-HSMC), and the neutral point voltage can be naturally balanced in a fundamental cycle. Based on the hybrid PS-PWM, an active voltage balancing control is put forward for the flying capacitor (FC). The voltage balancing of FC is implemented by slightly modifying the reference signals to adjust the duty cycles of the high-frequency switches symmetrically. This method does not need complex calculations, and it can be easily extended to higher level HSMC and other FC-based configurations. The simulations are carried out to validate the merits of low power losses and superior power quality. A downscale experimental platform of a 9L-HSMC is a setup to verify the effectiveness of the proposed control strategy under both the steady state and the transient states.

INDEX TERMS Multilevel converter, neutral point (NP) voltage, phase-shifted PWM (PS-PWM), stacked multicell converter (SMC), voltage balancing control.

I. INTRODUCTION

In recent years, three-level neutral-point-clamped (NPC) converter has been widely used in high-power motor drives and renewable energy conversions [1], [2]. However, as the number of voltage level increases, the clamping diodes and unbalance loss distribution will be fast increased. Due to the merits of absence of diodes and balanced loss distribution, the flying capacitor multilevel (FCM) converters are ideal alternatives for higher-level applications [3]. Nevertheless, a large number of flying capacitors (FCs) may reduce system reliability. In recent years, hybrid multilevel converters have been proposed and compared to popular multilevel topologies, they require less switches and FCs [4]–[17].

Active neutral-point-clamped (ANPC) converter is a newly introduced hybrid multilevel converter (HMC), which combines the advantages of the NPC and FC converters [4]. Three-level ANPC and several five-level ANPC topologies have been put forward in [5]–[9]. The stacked multicell converter (SMC) is another HMC [10], and it draws much attentions due to the overwhelming merits, such as modularity, and inherent natural balancing of FCs. Three-level T-type converter (T^2C) can be recognized as the SMC with one cell [11]–[13]. In low-voltage applications, three-level T^2C is a better choice than three-level NPC converter due to low conduction losses. Several HMC topologies have been proposed based on the T^2C cell [14]–[17].

To further increase the voltage levels with reduced devices (including dc voltage source, switches and FCs), several new hybrid stacked multicell converters (HSMCs) have been proposed based on the SMC [18]–[20]. These topologies are mainly obtained by adding low frequency (LF) switches to the original SMC. In [18], the number of dc voltage sources was reduced to half. In [19], a mixed stacked multicell converter

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was proposed, by adding four LF switches to the SMC. To reduce the LF switches, a HSMC was introduced in [20], which was derived by adding only two LF switches into the SMC. The number of high-frequency (HF) switches has been reduced to half whereas the peak-to-peak value of output voltage has been doubled, so it is an attractive alternative for single-phase converter systems. When it is applied in three-phase systems, an isolated dc source is required for each phase. In this paper, the HSMC is configured as a full bridge, which is composed of SMC and 2L half-bridge (2L-HB).

Capacitor voltage balancing control is one of the most essential issues for the HSMCs. Carrier-based pulse width modulation (PWM) methods are widely used in FC-based multilevel converters and they can achieve natural voltage balancing [21], [22]. Several voltage balancing control methods have been proposed for HMCs [23]–[31]. Nature voltage balancing methods were put forward based on phase-shifted PWM (PS-PWM) in [23] and [24] and phase-disposition PWM (PD-PWM) in [25] and [26]. However, the control performance depends on the load power factor and switching frequency. In [24], a *RLC* balancing booster circuit was proposed to achieve fast natural balancing which increased power losses. Several active voltage balancing control methods were proposed in [27]–[31]. In [27], a space vector PWM (SVPWM) based voltage balancing control was proposed, but it is only applicable to three-phase systems, besides, a large number of voltage vectors make it complex. In [28], an active voltage balancing method was proposed based on the implementation of cost function to minimize the FC voltage deviations, which requires complex calculations. In [29], a voltage balancing control based on PS-PWM was proposed for SMC, which balances the FC voltages with a proportional controller. However, the voltage balancing control for the SMC in [28] and [29] did not discuss the balancing of neutral point (NP) voltage. In [30], a multicarrier-based PWM method was proposed for balancing NP voltage by using zero-sequence injection method. In [31], the theoretical analysis of the NP voltage balancing was put forward for the 5L ANPC. In [32], an active voltage balancing control was proposed, which is implemented by using dynamic models. But the switching frequency and power losses were not discussed. Other voltage balancing control methods are also applied in different multilevel converters [33]–[35].

Due to different topologies and PWM algorithms, those aforementioned voltage balancing control methods cannot be directly applied to the HSMC. The previous voltage balancing control of the HSMC is commonly based on the selection of redundant switching states [20]. However, the switching frequency of the switches is varied significantly. There is also rare report on the voltage balancing control method for both the NP and FCs of the HSMC. For this reason, this paper proposes a new active voltage balancing control (AVBC) strategy for the HSMC to achieve constant average switching frequency and united voltage balancing control of the NP and FCs. A hybrid PS-PWM with modified reference signal is developed for the HSMC, where switches of the SMC operate in high frequency and the switches of 2L-HB operate in fundamental frequency. With this hybrid PS-PWM the merits of low power losses and superior output power quality can be obtained. Moreover, the hybrid PS-PWM achieves natural balancing of the NP voltage in a fundamental cycle. The AVBC strategy is implemented by modifying the reference signals of the HF switches slightly, which adjusts duty cycles of HF switches symmetrically. Therefore, the AVBC neither need additional balancing circuits nor complex calculations, and it can be easily extended to higher level and multi-phase configurations.

This paper is organized as follows. In Section II, operating principle of the HSMC and comparisons are described. In Section III, the modified hybrid PS-PWM and AVBC strategy are put forward. In Section IV, the FFT spectrum, current THD and power losses are studied by simulations. In Section V, a small-scale experimental platform of the HSMC is built, and experiment results under steady state and transient states are presented. Finally, the conclusions are drawn in Section VI.

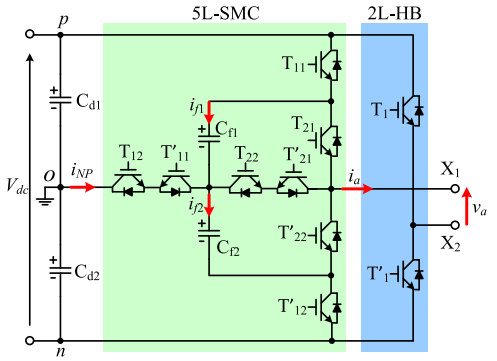

FIGURE 1. Circuit schematic of single-phase 9L-HSMC.

II. HYBRID STACKED MULTICELL CONVERTERS

A. NINE-LEVEL HSMC

Fig. 1 shows the circuit diagram of single-phase 9L-HSMC. It is composed of a 5L-SMC and a 2L-HB, and the midpoints of the 5L-SMC and 2L-HB are two AC output terminals X_1 and X_2. where v_a and i_a are output voltage and phase current, respectively; i_{f1}, i_{f2} are FC currents that flow through C_{f1} and C_{f2}; I_{NP} is the instantaneous *NP* current.

To make full use of the merits of the 9L-HSMC, the switches $T_{11}, T_{12}, T_{21}, T_{22}$ and their complementary switches of the 5L-SMC operate in high frequency (depends on the utilized carrier frequency) and the switches T_1 and T_1' of the 2L-HB operate in fundamental frequency (equals to 50Hz). Then the high quality output and low power losses will be obtained. Assuming the dc-bus voltage is V_{dc}, the capacitor voltages v_{c1} and v_{c2} should be maintained at $V_{dc}/2$ and the reference voltage of C_{f1} and C_{f2} is $V_{dc}/4$.

B. SWITHING STATES AND CURRENT PATHS

Table 1 shows switching states, output voltage and effects on the FCs. There are eighteen switching states that are used to

TABLE 1. Switching states, output voltage and effects on FCs.

States	LF cell	HF cell	Output voltage	NP current	FC current		FC voltage	
	T_1	$T_{11}T_{12}T_{21}T_{22}$	v_a	i_{NP}	i_{f1}	i_{f2}	v_{f1}	v_{f2}
V_1	0	1 1 1 1	V_{dc}	0	0	0	n	n
V_2	0	1 1 0 1	$3V_{dc}/4$	0	i_a	0	↑	n
V_3	0	0 1 1 1	$3V_{dc}/4$	i_a	$-i_a$	0	↓	n
V_4	0	0 1 0 1	$V_{dc}/2$	i_a	0	0	n	n
V_5	0	0 0 1 1	$V_{dc}/2$	0	$-i_a$	$-i_a$	↓	↓
V_6	0	1 1 0 0	$V_{dc}/2$	0	i_a	i_a	↑	↑
V_7	0	0 1 0 0	$V_{dc}/4$	i_a	0	i_a	n	↑
V_8	0	0 0 0 1	$V_{dc}/4$	0	0	$-i_a$	n	↓
V_9	0	0 0 0 0	0	0	0	0	n	n
V_{10}	1	1 1 1 1	0	0	0	0	n	n
V_{11}	1	0 1 1 1	$-V_{dc}/4$	i_a	$-i_a$	0	↓	n
V_{12}	1	1 1 0 1	$-V_{dc}/4$	0	i_a	0	↑	n
V_{13}	1	0 1 0 1	$-V_{dc}/2$	i_a	0	0	n	n
V_{14}	1	1 1 0 0	$-V_{dc}/2$	0	i_a	i_a	↑	↑
V_{15}	1	0 0 1 1	$-V_{dc}/2$	0	$-i_a$	$-i_a$	↓	↓
V_{16}	1	0 0 0 1	$-3V_{dc}/4$	0	0	$-i_a$	n	↓
V_{17}	1	0 1 0 0	$-3V_{dc}/4$	i_a	0	i_a	n	↑
V_{18}	1	0 0 0 0	$-V_{dc}$	0	0	0	n	n

The current and voltage are given assuming i_a>0 with the notations: "↓" represents capacitor discharging, "↑" represents capacitor charging, "n" represents no influence on the flying capacitors.

output nine levels ($\pm V_{dc}$, $\pm 3V_{dc}/4$, $\pm V_{dc}/2$, $\pm V_{dc}/4$, 0), and state redundancies are available for each voltage level except for states V_{dc} and $-V_{dc}$. According to Table 1, the output voltage v_a can be expressed as

$$v_a = -V_{dc}S_1 + \frac{1}{4}V_{dc}\left(S_{11} + S_{12} + S_{21} + S_{22}\right), \quad (1)$$

where S_1, S_{11}, S_{12}, S_{21} and S_{22} are switching functions of switches T_1, T_{11}, T_{12}, T_{21} and T_{22}, respectively.

To make it more comprehensive, the current paths and switching state combinations are shown in Fig. 2 under the positive current ($i_a > 0$) for voltage levels $\pm V_{dc}$ and $\pm V_{dc}/4$, where on-state and off-state devices are marked in black and gray colors, respectively. As can be seen in Fig. 2(a) and 2(b), the states V_1 and V_{18} are used to output voltage V_{dc} and $-V_{dc}$, and no current flows through the FCs. As shown in Fig. 2(c) and 2(d), states V_7 and V_8 can be selected to output $V_{dc}/4$, and they have opposite effects on the C_{f2}. States V_{11} and V_{12} are used to output $-V_{dc}/4$, resulting in discharging and charging C_{f1}, as shown in Fig. 2(e) and 2(f). Note that the effects on the FC voltage will be opposite with the reversal of phase current.

C. GENERIC TOPOLOGY OF HSMC

The HSMC can be extended to generate more voltage levels for obtaining higher quality output waveforms, and then the cost and volume of the output filter would be decreased. Fig. 3 shows the generic circuit configuration of the (4n + 1)-level HSMC, which is obtained by combing an n-cell (2n + 1)-level SMC with a 2L-HB.

If the dc-bus voltage is V_{dc}, the voltages of C_{fn1} and C_{fn2} should be controlled at their reference value $V_{dc}/(2\times n)$. The reference value of FCs in the k_{th} cell can be expressed as

$$v_{fk1} = v_{fk2} = \frac{V_{dc}}{2 \times n}(n - k + 1), \quad (k = 2,\ 3, \ldots,\ n). \quad (2)$$

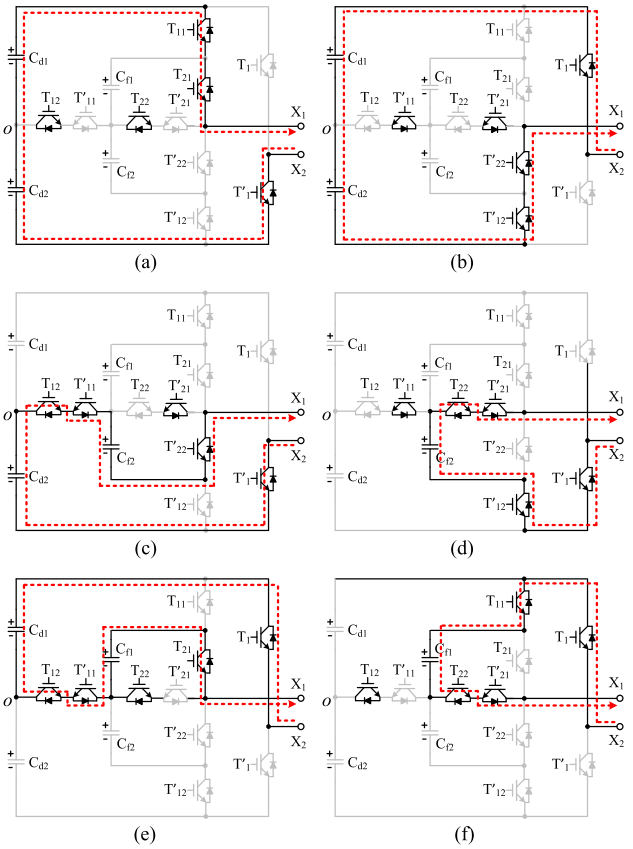

FIGURE 2. Current paths and switching state combinations under the positive phase current. (a) V_{dc} (V_1), (b) $-V_{dc}$ (V_{18}), (c) $V_{dc}/4$ (V_7), (d) $V_{dc}/4$ (V_8), (e) $-V_{dc}/4$ (V_{11}), (f) $-V_{dc}/4$ (V_{12}).

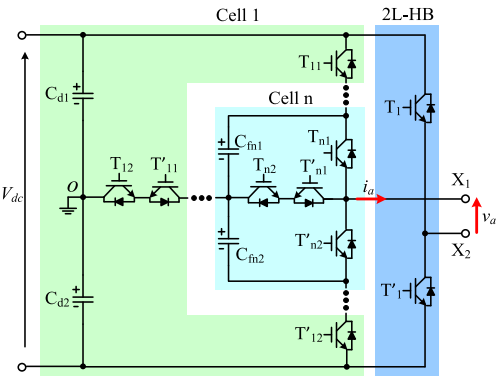

FIGURE 3. Circuit configuration of (4n + 1)-level HSMC with n-cell (2n + 1)-level SMC.

The comparisons of n-level FC-based multilevel converters are shown in Table 2. It is shown that the HSMC has fewer switches and FCs than the other compared converters for generating a higher level voltage.

III. PROPOSED VOLTAGE BALANCING CONTROL

A modified hybrid PS-PWM approach is developed for the HSMC by combining the PS-PWM with the PD-PWM algorithms. The natural balancing of NP voltage is theoretically analyzed. A new AVBC strategy based on the modified hybrid PS-PWM is proposed to balance the FC voltages.

TABLE 2. Comparisons of FC-based multilevel converters.

Topologies	Number of devices			
	FC cell	LF switch	HF switch	FC
FCM [2]	n-1	0	2(n-1)	n-2
SMC [10]	n-1	0	2(n-1)	n-3
Ref. [15]	(n-1)/2	6	n-1	(n-1)/2
Ref. [16]	$2[\log_2(n\text{-}1)/3]+2$	6	$4[\log_2(n\text{-}1)/3]+4$	$2[\log_2(n\text{-}1)/3]$
HSMC [20]	(n-1)/2	2	n-1	(n-5)/2

Note: $N_{level}=n$ and n is odd; dc source voltage is V_{dc}.

A. MODIFIED HYBRID PHASE-SHIFTED PWM

In the HSMC, there are LF switches which have to endure high voltage and should be switched in low frequency to reduce the switching losses. The switches in the SMC should be operated in high frequency to obtain high-quality output waveforms. To meet this requirement, a hybrid PS-PWM is developed, and the modified reference signal v_{ref} is obtained from the original modulation signal v_{am}. They are

$$v_{am} = 2m\sin(\omega t + \phi), \tag{3}$$

$$v_{ref} = v_{am} - sign\ (v_{am}), \tag{4}$$

$$sign(v_{am}) = \begin{cases} 1, & v_{am} \geq 0 \\ -1, & v_{am} < 0, \end{cases} \tag{5}$$

where $sign(\ )$ is sign function,m is modulation index ($0 \leq m \leq 1$), ω and φ are angular frequency and power factor angular, respectively.

Fig. 4 shows the principle of modified hybrid PS-PWM for the 9L-HSMC. Four triangular carriers in frequency $f_c =$ 500 Hz are distributed on both sides of zero axis. Carrier 1 and carrier 2 are used to generate gating signals for switches T_{11} and T_{21}, while carrier 3 and carrier 4 are for T_{12} and T_{22}, respectively. If the value of v_{ref} is higher than that of carrier 1, T_{11} will be on (T'_{11} is off) and similar rules can be applied to other three carriers. The gating signals for T_1 are generated by comparing v_{ref} with zero. During the positive half cycle of v_{ref}, T_1 is switched off, and then switched on during the negative half cycle. As shown in Fig. 4(b), 5L and 9L voltages v_{ao}, v_a are generated.

B. THEORETICAL ANALYSIS OF NP VOLTAGE NATURAL BALANCING

It can be seen from Fig. 1 and Tab. 1 that the phase current flows through NP when T_{11}' and T_{12} are switched on, and the instantaneous NP current i_{NP} can be expressed as

$$i_{NP} = (S_{12} - S_{11}) \cdot i_a. \tag{6}$$

Table 1 shows that the states V_3, V_4, V_7, V_{11}, V_{13} and V_{17} have contributions to the NP current. Since the reference modulation voltage v_{am} is selected as base value ($v_{am} \in [-2, 2]$), the reference voltage v_{ref} for the HF switches can be rewritten as

$$v_{ref} = \begin{cases} v_{am} + 1, & (-2 \leq v_{am} \leq 0) \\ v_{am} - 1, & (0 \leq v_{am} \leq 2). \end{cases} \tag{7}$$

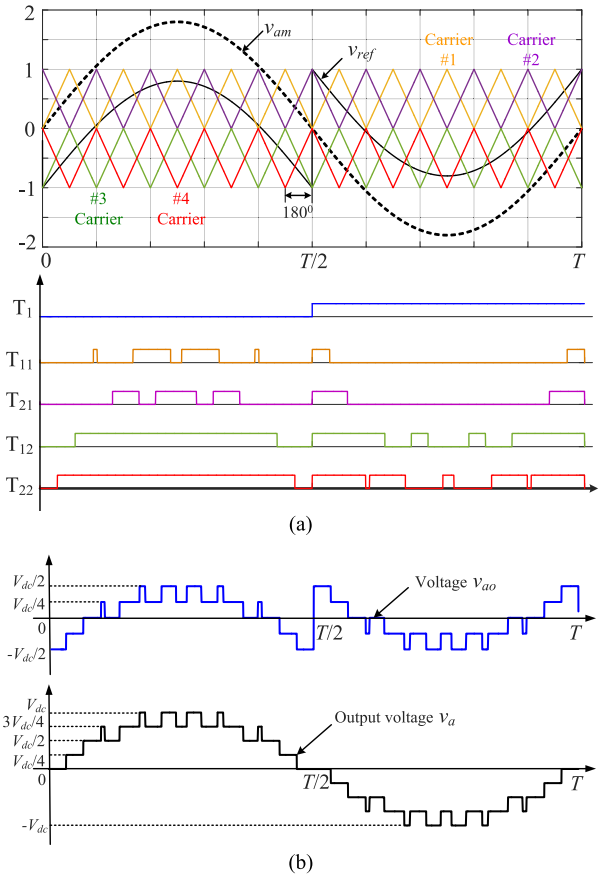

FIGURE 4. Modified hybrid PS-PWM for the 9L-HSMC. (a) Gating signal generation, (b) output voltage.

If the carrier frequency f_c is higher enough than the fundamental frequency, v_{ref} can be assumed constant in one carrier cycle. Then the duty cycle of the HF switches can be defined as

$$\begin{cases} d_{11} = d_{21} = v_{ref} \\ d_{12} = d_{22} = 1, \end{cases} \quad (0 \leq v_{ref} \leq 1). \tag{8}$$

$$\begin{cases} d_{12} = d_{22} = 1 + v_{ref} \\ d_{11} = d_{21} = 0, \end{cases} \quad (-1 \leq v_{ref} \leq 0). \tag{9}$$

where d_{ij} (i, j=1, 2) represent duty cycles of HF switches T_{ij}.

In order to obtain the duty cycle of the states, v_{ref} is divided into four regions $[-1, -0.5)$, $[-0.5, 0)$, $[0, 0.5)$, $[0.5, 1]$, as shown in Fig. 4.

When $0 \leq v_{am} \leq 2$ and v_{ref} locate at $[-1, -0.5)$ and $[-0.5, 0)$, T_1, T_{11} and T_{21} are switched off while T_{12} and T_{22} operate in high frequency. The state sequences in a carrier cycle are V_7-V_9-V_8-V_9-V_7 and V_7-V_4-V_8-V_4-V_7, and the duty cycles of the states can be calculated as

$$\begin{cases} dV_7 = d_{12} \\ dV_8 = d_{22} \\ dV_9 = 1 - d_{12} - d_{22}, \end{cases} \quad (1 \leq v_{ref} < -0.5). \tag{10}$$

$$\begin{cases} dV_7 = 1 - d_{22} \\ dV_8 = 1 - d_{12} \\ dV_4 = d_{12} + d_{22} - 1, \end{cases} \quad (-0.5 \le v_{ref} < 0). \tag{11}$$

When $0 \le v_{am} \le 2$ and v_{ref} locate at [0, 0.5) and [0.5, 1], T_{12} and T_{22} are switched on while T_1 is switched off, and the T_{11} and T_{21} operate in high frequency. The state sequences in a carrier cycle are V_2-V_4-V_3-V_4-V_2 and V_2-V_1-V_3-V_1-V_2, and the duty cycles of the states are

$$\begin{cases} dV_2 = d_{11} \\ dV_3 = d_{21} \\ dV_4 = 1 - d_{11} - d_{21}, \end{cases} \quad (0 \le v_{ref} < 0.5). \tag{12}$$

$$\begin{cases} dV_2 = 1 - d_{21} \\ dV_3 = 1 - d_{11} \\ dV_1 = d_{11} + d_{21} - 1, \end{cases} \quad (0.5 \le v_{ref} \le 1). \tag{13}$$

When $-2 \le v_{am} \le 0$ and v_{ref} locate at $[-1, -0.5)$ and $[-0.5, 0)$, T_1 is switched on while T_{11} and T_{21} are switched off. The state sequences in a carrier cycle are V_{17}-V_{18}-V_{16}-V_{18}-V_{17} and V_{17}-V_{13}-V_{16}-V_{13}-V_{17}, and the duty cycles of the states are

$$\begin{cases} dV_{17} = d_{12} \\ dV_{16} = d_{22} \\ dV_{18} = 1 - d_{12} - d_{22}, \end{cases} \quad (-1 \le v_{ref} < -0.5). \tag{14}$$

$$\begin{cases} dV_{17} = 1 - d_{22} \\ dV_{16} = 1 - d_{12} \\ dV_{13} = d_{12} + d_{22} - 1, \end{cases} \quad (-0.5 \le v_{ref} < 0). \tag{15}$$

When $-2 \le v_{am} \le 0$ and v_{ref} locate at [0, 0.5) and [0.5, 1], T_1 is switched on while the T_{12} and T_{22} are switched on. The state sequences in a carrier cycle are V_{12}-V_{13}-V_{11}-V_{13}-V_{12} and V_{12}-V_{10}-V_{11}-V_{10}-V_{12}, and the duty cycles of the states are

$$\begin{cases} dV_{12} = d_{11} \\ dV_{11} = d_{21} \\ dV_{13} = 1 - d_{11} - d_{21}, \end{cases} \quad (0 \le v_{ref} < 0.5). \tag{16}$$

$$\begin{cases} dV_{12} = 1 - d_{21} \\ dV_{11} = 1 - d_{11} \\ dV_{10} = d_{11} + d_{21} - 1, \end{cases} \quad (0.5 \le v_{ref} \le 1). \tag{17}$$

According to Eq. (8) to Eq. (17), the average NP current $\bar{i}_{NP}$ can be obtained by combining the contributions of V_3, V_4, V_7, V_{11}, V_{13} and V_{17} in a carrier cycle, and yielding

$$\bar{i}_{NP} = \begin{cases} (1 + v_{ref}) \cdot i_a, & (v_{ref} \in [-1, 0) \& v_{am} \in [0, 2]) \\ (1 - v_{ref}) \cdot i_a, & (v_{ref} \in (0, 1] \& v_{am} \in [0, 2]) \\ (1 + v_{ref}) \cdot i_a, & (v_{ref} \in [-1, 0) \& v_{am} \in [-2, 0]) \\ (1 - v_{ref}) \cdot i_a, & (v_{ref} \in (0, 1] \& v_{am} \in [-2, 0]). \end{cases} \tag{18}$$

According to Eqs. (3), (7) and (18), the average NP current in a fundamental cycle T can be calculated by

$$\bar{I}_{NP} = \frac{1}{T} \int_0^T \bar{i}_{NP}(t) dt = 0. \tag{19}$$

From (19), the average NP current in a fundamental cycle T for a single phase is equal to zero. It means that the NP voltage of the 9L-HSMC is naturally balanced by using the modified hybrid PS-PWM method under ideal and steady-state condition. For three-phase applications, there are two circuit configurations which are supplied by three isolated dc sources and one single dc source, as shown in Fig. 5.

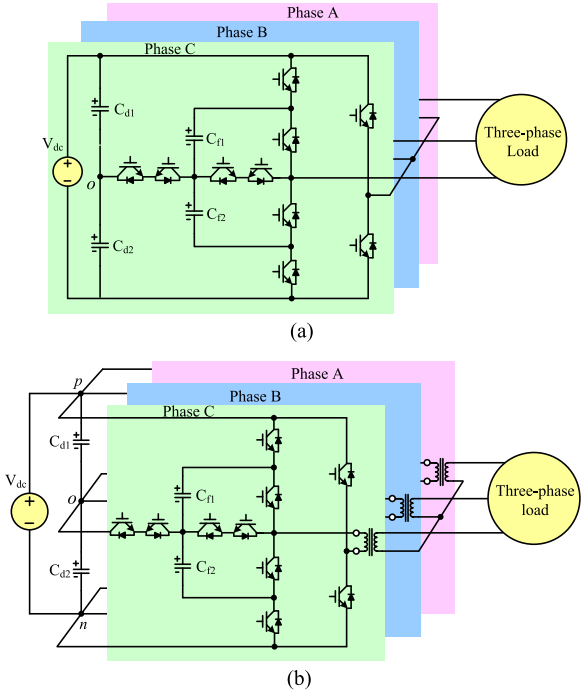

FIGURE 5. Circuits of three-phase 9L HSMC with (a) three isolated dc sources, (b) single dc source and three output coupling transformers.

As can be seen in Fig. 5(a), the NP voltage of each phase can be naturally balanced by using the modified hybrid PS-PWM, which named "single-phase method". The balance of the NP voltage in Fig. 5(b) can be achieved by "three-phase method" such as zero-sequence injection in carrier-based PWM methods and optimum redundant vector selection in SVM-based methods. The relationship between the average NP current and zero-sequence voltage is similar as the NPC and ANPC converters [30], [31].

C. ACTIVE VOLTAGE BALANCING CONTROL

As shown in Table 1, the redundant sates are available for each level except for $-V_{dc}$ and V_{dc}, which provides a freedom degree for balancing FC voltages. For example, V_7 and V_8 are the redundant states for generating voltage level $V_{dc}/4$ which have opposite effects on the C_{f2}. Similarly, V_{11} and V_{12} for voltage level $-V_{dc}/4$ have opposite effects on C_{f1}.

The phase current flows into or out the C_{f1} when T_{11} and T_{21}' are switched on or off. Similarly, phase current flow into

or out C_{f2} when T_{12} and T_{22}' are switched on or off. The instant FC currents i_{f1} and i_{f2} can be expressed as

$$\begin{cases} i_{f1} = (S_{11} - S_{21}) \cdot i_a \\ i_{f2} = (S_{12} - S_{22}) \cdot i_a. \end{cases} \tag{20}$$

The average FC currents in a carrier cycle can be rewritten as

$$\begin{cases} \bar{i}_{f1} = (d_{11} - d_{21}) \cdot \bar{i}_a \\ \bar{i}_{f2} = (d_{12} - d_{22}) \cdot \bar{i}_a, \end{cases} \tag{21}$$

where d_{ij}(i=1, 2; j=1, 2) is duty cycle of the switch S_{ij}, and $\bar{i}_a$ is average phase current over a carrier cycle.

It can be seen from (21) that the average FC current is determined by the phase current and duty cycle of the adjacent HF switches. The voltage deviations of the FC voltage can be calculated by the average FC current. It yields

$$\begin{cases} C_{f1}\Delta v_{f1}/T_s = (d_{11} - d_{21}) \cdot \bar{i}_a \\ C_{f2}\Delta v_{f2}/T_s = (d_{12} - d_{22}) \cdot \bar{i}_a, \end{cases} \tag{22}$$

where Δv_{f1} and Δv_{f2} are FC voltage deviations, and they are defined as $\Delta v_{f1} = V_{dc}/4 - v_{f1}$, $\Delta v_{f2} = V_{dc}/4 - v_{f2}$ in the 9L-HSMC.

Since the phase current in one carrier cycle is assured constant, the duty cycle can be adjusted to balance the FC voltage according to (21) and (22). When using the PS-PWM to the original SMC, it meets $d_{11} = d_{21}$ and $d_{12} = d_{22}$ in one carrier cycle. So the average FC current is zero and FC voltage is naturally balanced under steady state. As the modified hybrid PS-PWM is applied to the HSMC, the duty cycle should be adjusted properly to balance the FC voltage. So an AVBC strategy is proposed for the HSMC to enhance voltage balancing performance of FCs under dynamic conditions. The reference modulation signal v_{ref} can be modified to adjust the duty cycles of the HF switches and the operating time of the redundant states might be modified. As each half cycle of v_{ref} has been divided into four regions in Fig. 4(a) as [0, 0.5], [0.5, 1], [−0.5, 0] and [−1, −0.5]. For $0 \le v_{ref} \le 2$, the modified states by adjusting the duty cycles under four different conditions can be shown in Fig. 6.

1) When $v_{ref} \in [0,\ 0.5)$, T_1 is switched off and T_{12}, T_{22} are switched on continually. If C_{f1} needs to be discharged, a negative average FC current $\bar{i}_{f1}$ should be generated. As d_{11} and d_{21} decrease and increase symmetrically, the output voltage will not be changed but a negative current $\bar{i}_{f1}$ is provided. Fig. 6(a) shows the modified states by adjusting the duty cycle. The new duty cycles d_{11}' and d_{21}' are obtained by

$$\begin{cases} d_{11}' = v_{ref} - \Delta d_{11} \\ d_{21}' = v_{ref} + \Delta d_{21}, \end{cases} \tag{23}$$

where Δd_{11} and Δd_{21} are compensated duty cycle and $\Delta d_{11} = \Delta d_{21} = \Delta d_1$. Note that the value of d_{11}' and d_{21}' should be located at the same range of v_{ref} to ensure the output voltage level unchangeable in one carrier cycle. The negative $\bar{i}_{f1}$ is obtained by

$$\bar{i}_{f1} = -(\Delta d_{11} + \Delta d_{21}) \cdot \bar{i}_a = -2\Delta d_1 \cdot \bar{i}_a. \tag{24}$$

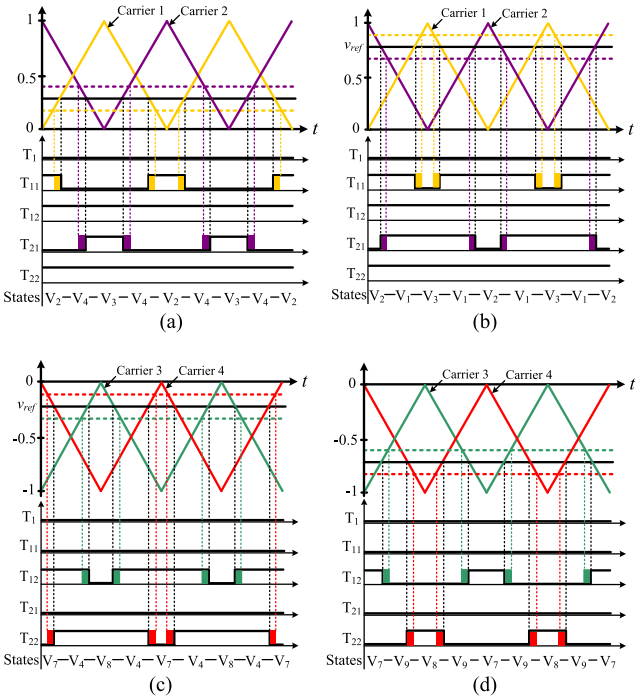

FIGURE 6. Modified switching states by adjusting the duty cycle for positive output voltage ($0 \le v_{am} \le 2$): (a) $0 \le v_{ref\_} < 0.5$, C_{f1} needs to be discharged; (b) $0.5 \le v_{ref\_} \le 1$, C_{f1} needs to be charged; (c) $-0.5 \le v_{ref\_} < 0$, C_{f2} needs to be discharged; (d) $-1 \le v_{ref\_} < -0.5$, C_{f2} needs to be charged.

2) When $v_{ref} \in (0.5,\ 1]$, T_1 is switched off and T_{12}, T_{22} are switched on continually. If C_{f1} needs to be charged, a positive $\bar{i}_{f1}$ should be generated. And then d_{11} and d_{21} will increase and decrease symmetrically. Fig. 6(b) shows the modified states by adjusting the duty cycle. The new duty cycles d_{11}',d_{21}' and the positive $\bar{i}_{f1}$ are obtained by

$$\begin{cases} d_{11}' = v_{ref} + \Delta d_{11} \\ d_{21}' = v_{ref} - \Delta d_{21}, \end{cases} \tag{25}$$

$$\bar{i}_{f1} = (\Delta d_{11} + \Delta d_{21}) \cdot \bar{i}_a = 2\Delta d_1 \cdot \bar{i}_a. \tag{26}$$

3) When $v_{ref} \in [-0.5,\ 0)$, T_1 is switched on and T_{11}, T_{21} are switched off continually. If C_{f2} needs to be discharged, a negative $\bar{i}_{f2}$ should be generated. And then d_{12} and d_{22} will decrease and increase symmetrically. Fig. 6(c) shows the modified states by adjusting the duty cycle. The new duty cycles d_{12}',d_{22}' and the negative $\bar{i}_{f2}$ are obtained by

$$\begin{cases} d_{12}' = v_{ref} - \Delta d_{12} \\ d_{22}' = v_{ref} + \Delta d_{22}, \end{cases} \tag{27}$$

$$\bar{i}_{f2} = -(\Delta d_{12} + \Delta d_{22}) \cdot \bar{i}_a = -2\Delta d_2 \cdot \bar{i}_a, \tag{28}$$

where Δd_{12} and Δd_{22} are compensated duty cycle and $\Delta d_{12} = \Delta d_{22} = \Delta d_2$.

4) When $v_{ref} \in [-1,\ -0.5]$, T_1 is switched on and T_{11}, T_{21} are switched off continually. If C_{f2} needs to be charged, a positive $\bar{i}_{f2}$ should be generated. And then d_{12} and d_{22} will increase and decrease symmetrically. Fig. 6(d) shows the

modified states by adjusting the duty cycle. The new duty cycles d'_{12},d'_{22} and the positive $\bar{i}_{f2}$ are obtained by

$$\begin{cases} d'_{12} = v_{ref} + \Delta d_{12} \\ d'_{22} = v_{ref} - \Delta d_{22}, \end{cases} \tag{29}$$

$$\bar{i}_{f2} = (\Delta d_{12} + \Delta d_{22}) \cdot \bar{i}_a = 2\Delta d_2 \cdot \bar{i}_a. \tag{30}$$

Since the compensated duty cycle $\Delta d_{ij}(i, j = 1, 2)$ is a quite small adjusted value, it can be obtained by using a proportional integrator (PI) or a hysteresis controller. Here a proportional controller is used to simplify the controller. The compensated duty cycle Δd_1 and Δd_2 can be calculated by

$$\begin{cases} \Delta d_1 = K\left(v_{f\_ref} - v_{f1}\right) \cdot sign(i_a) \\ \Delta d_2 = K\left(v_{f\_ref} - v_{f2}\right) \cdot sign(i_a), \end{cases} \tag{31}$$

where $sign(i_a)$ is the sign function and it is 1 and -1 when $i_a > 0$ and $i_a < 0$, respectively. K is a proportional factor, and it can be tuned flexibly to minimize the FC voltage deviation.

In the AVBC, the voltage balancing is realized by adjusting duty cycles of the HF switches symmetrically, and it does not depend on the modulation index and carrier frequency.

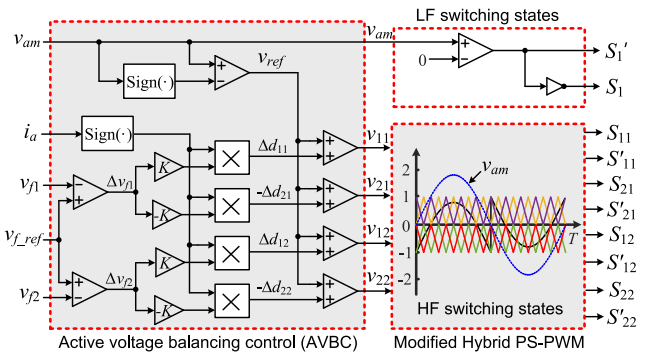

FIGURE 7. Principle of the proposed AVBC with modified hybrid PS-PWM algorithm for the 9L-HSMC.

D. IMPLEMENTATION OF PROPOSED ALGORITHM

Fig. 7 shows the principle of the proposed hybrid PS-PWM combined with AVBC algorithm. The gating signals of LF switches T_1 and T_1' are generated by comparing v_{am} with zero. The new duty cycle d'_{ij} of the HF switch T_{ij} is generated by tuning the factor K according to the FC voltage deviation and $sign(i_a)$. For example, assuming $sign(i_a) = 1$ and C_{f1} needs to be charged, a positive FC average current $\bar{i}_{f1}$ should be generated. The compensated duty cycle Δd_{11} and Δd_{21} are generated and used to form the new duty cycle (reference signal v_{11} and v_{21}). In this case, a positive $\bar{i}_{f1}$ will be generated to charge the C_{f1}.

Overall, the AVBC based on modified hybrid PS-PWM can be implemented by the following steps:

1) Obtain the reference modulation signals v_{am} and v_{ref} by using outer loops to meet specific control targets (active and reactive power control, common voltage suppression, etc.)

2) Detect the phase current direction $sign(i_a)$ and FC voltages v_{f1}, v_{f2}, and then calculate voltage deviations Δv_{f1}, Δv_{f2} and the average FC currents $\bar{i}_{f1}$, $\bar{i}_{f2}$.

3) Calculate the compensated duty cycles $\Delta d_{ij}(i = 1, 2; j = 1, 2)$ by selecting optimum value of the factor K, considering control the FC voltage deviation within the defined threshold value while reduce the average switching frequency.

4) Obtain the new duty cycle d'_{ij} of the HF switches T_{ij} by adding Δd_{ij} to the original v_{ref}, and then the resulted reference signals v_{ij} are compared with the triangular carriers.

5) Determine the optimum switching state for each voltage level and apply the gating signals (from Table 1) for the LF and HF switches T_1, T_{ij}, respectively.

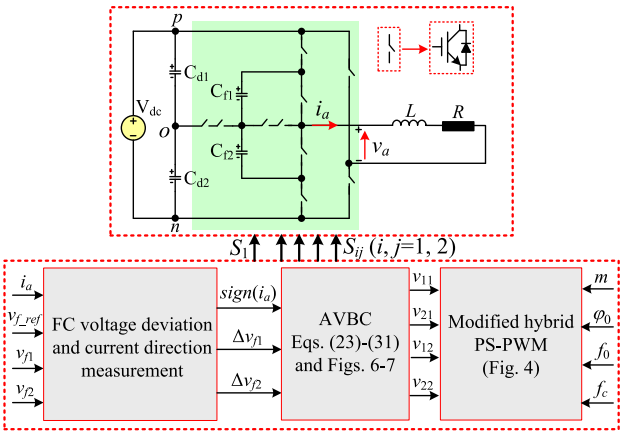

FIGURE 8. Overall diagram of the AVBC with modified hybrid PS-PWM for the single-phase 9L-HSMC.

Fig. 8 shows the overall block diagram of the AVBC with modified hybrid PS-PWM for the single-phase 9L-HSMC. The ac-side output of the 9L-HSMC is connected with a pure resistor through a filtering inductor. The reference voltage v_{am} of the hybrid PS-PWM can be synthesized by using Eq. (3). The proposed AVBC algorithm is implemented by using Eqs. (23)-(31) and Figs. (6)-(7).

E. GENERALIZED ALGORITHM

As shown in Fig. 3, a higher level HSMC is achieved by stacking more HF cells in the SMC, which may be suitable for low-voltage high-efficiency applications, such as the renewable energy conversion system, power quality compensator. The FC voltages in each HF cell should be balanced separately. Fortunately, the proposed AVBC can be easily extended due to the modularity of the HSMCs. Fig. 9 shows the generalized algorithm of the proposed AVBC with hybrid PS-PWM for a (4n + 1)-level HSMC with n HF cells. As shown in Fig. 9, the AVBC consists of n cells that are used to adjust the duty cycles for the HF switches of each HF cell. The reference value of the FC voltages v_{fk1} and v_{fk2} $(k = 2, 3, \ldots, n)$ for the k_{th} HF cell has been defined in Eq. (2). The required number of carriers is equal to $2n$ for a (4n + 1)-level HSMC, and they have a π/n phase-shift with each other.

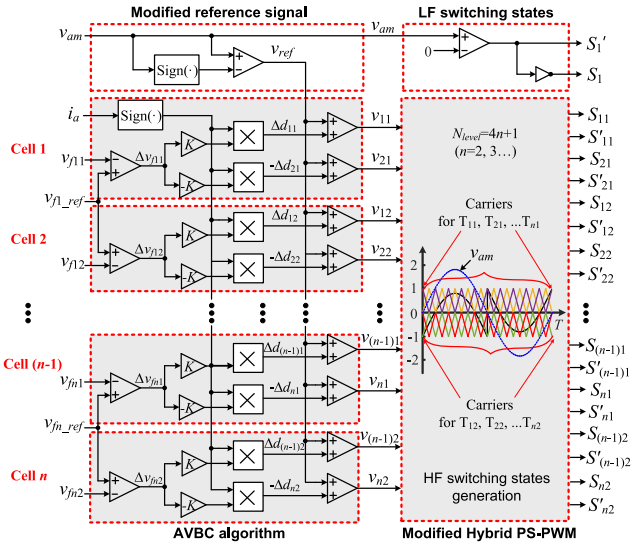

FIGURE 9. Generalized algorithm of the proposed AVBC with modified hybrid PS-PWM for the (4n + 1)-level HSMC.

TABLE 3. Comparisons of voltage balancing control for FC-based multilevel converters.

Methods (PWM technology)	Voltage balancing capability	
	Neutral point	Flying capacitor
Ref. [23-24] (PS-PWM)	**Not good**, not discussed.	**Good**, but the *RLC* circuit is required, and power losses are increased.
Ref. [25-26] (PD-PWM)	**Not good**, not discussed.	**Good**, but the performance depends on the load power factor and carrier frequency.
Ref. [27] (SVPWM)	**Good,** plentiful voltage vectors make it complex for high-level topology.	**Not good,** it is only applicable to the three-phase converter system.
Ref. [28-29] (PD-PWM, PS-PWM)	**Not good,** not discussed.	**Good**, based on a cost function, which requires complex calculations.
Ref. [30] (PD-PWM)	**Not good**, not discussed.	**Good**, based on zero-sequence injection.
AVBC (hybrid PS-PWM)	**Good**, NP voltage is naturally balanced.	**Good**, not depend on the modulation index and carrier frequency.

Table 3 shows the comparisons of voltage balancing control methods for FC-based multilevel converters. The proposed AVBC method requires neither additional hardware circuits nor complex calculations, and voltage balancing control for both NP and FC is achieved.

IV. PERFORMANCE EVALUATIONS

To evaluate the performance of 9L-HSMC with the proposed control strategy, a simulation model is built in the MATLAB/Simulink with system parameters are listed in Table 4. The dc bus is supplied by a dc power source $V_{dc} = 1$ kV while the ac-side output is series connected with a linear *RL*-load ($R = 10\ \Omega$, $L = 10$ mH). Infineon switches FZ400R17KE3 are used in the main circuit. The power losses are calculated by using the PLECS Toolbox within MATLAB/Simulink environment based on the constructed model.

TABLE 4. Simulation parameters.

Symbols	Parameters	Values
V_{dc}	Dc-bus voltage	1 kV
f_0	Output frequency	50 Hz
f_s	Sampling frequency	10 kHz
C_f	Flying capacitor	1 mF
C_{dc}	Dc-link capacitor	2200 μF
L	Filtering inductor	10 mH
R	Resistor load	10 Ω

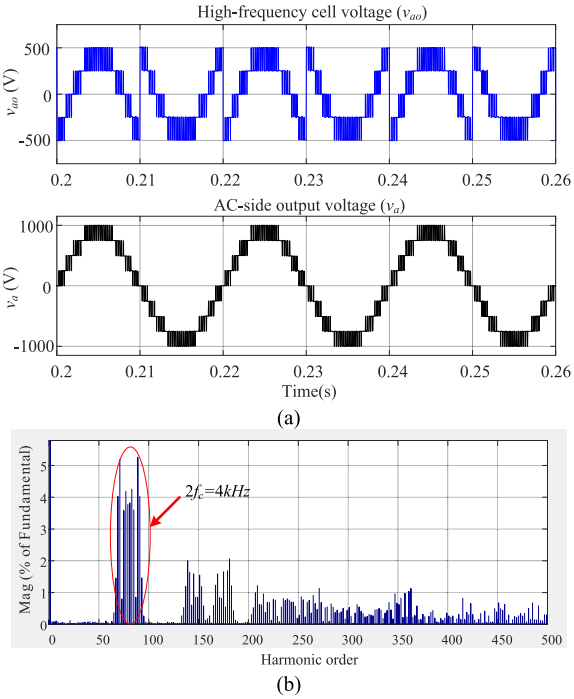

FIGURE 10. Simulation results of the 9L HSMC with *RL*-load ($m = 0.9$, $f_c = 2$ kHz). (a) Output voltage, (b) FFT spectrum of output voltage.

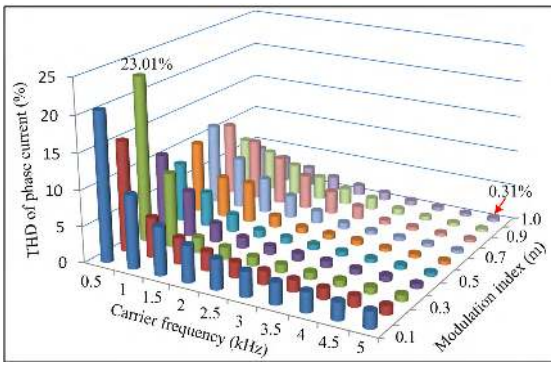

FIGURE 11. THD of phase current plot versus the modulation index m (from 0.1 to 1.0) and carrier frequency f_c (from 0.5 kHz to 5 kHz).

A. FFT SPECTRUM AND THD ANALYSIS

Fig. 10 shows the simulation results, where the carrier frequency f_c is 2 kHz and the modulation index m is 0.9. The high-frequency cell voltage v_{ao} and ac-side output voltage v_a have five levels and nine levels, respectively. Fig. 10 (b) shows the first sideband harmonics centered around 4 kHz, since the equivalent frequency is $2f_c$. Fig. 11 shows the THD

of phase current plot versus m (from 0.1 to 1.0) and f_c (from 0.5 to 5 kHz). It reveals that the THD is decreased by increasing the value of m and f_c to some extent.

B. AVERAGE SWITCHING FREQUENCY

The average switching frequency f_{sw_avg} of the 9L-HSMC over one fundamental cycle is defined as

$$f_{sw\_avg} = \frac{f_{s1} + f_{s11} + f_{s12} + f_{s21} + f_{s22}}{5}, \tag{32}$$

where f_{s1}, f_{s11}, f_{s12}, f_{s21} and f_{s22} are average switching frequencies of the switches T_1, T_{11}, T_{12}, T_{21} and T_{22}, respectively.

To evaluate the effect of proportional factor K in the AVBC strategy, the average switching frequency f_{sw_avg} and the peak-to-peak value of FC voltage deviation ΔV_{peak}, according to the factor K are given in Fig. 12. Here $m = 0.9$ and $f_c = 2$ kHz. As the K increases from 0 to 1, ΔV_{peak} and f_{sw_avg} vary in opposite trends. As can be seen in Fig. 12, the value of f_{sw_avg} is not varied significantly with the range of K from 0.3 to 1, and the value of ΔV_{peak} decrease continuously. It can be concluded that a relative constant switching frequency and good balancing capability are obtained by using the AVBC strategy. In order to obtain an optimum control performance, the value of K is selected as 0.6 by making a tradeoff between ΔV_{peak} and f_{sw_avg}.

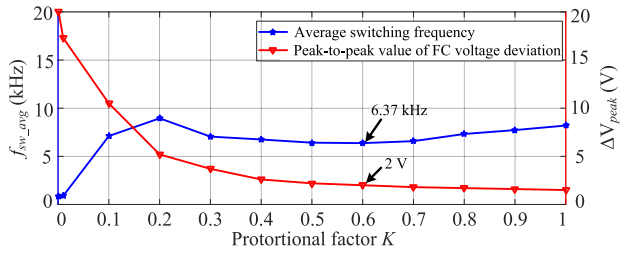

FIGURE 12. Average switching frequency f_{sw_avg} and peak-to-peak value of FC voltage deviation ΔV_{peak} versus factor K.

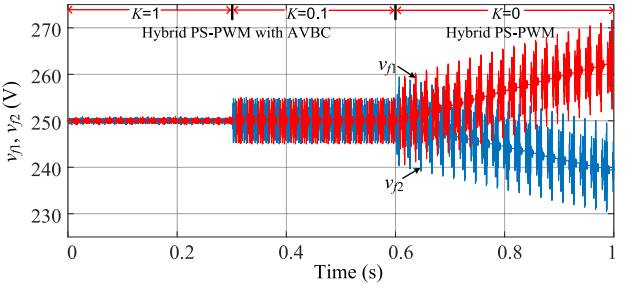

FIGURE 13. Waveforms of FC voltages with hybrid PS-PWM and AVBC strategy under different values of proportional factor K ($m = 0.9$, $f_c = 2$ kHz).

Fig. 13 shows the simulation results of FC voltage with proposed hybrid PS-PWM and AVBC strategy under three different values of K. Here $m = 0.9$ and $f_c = 2$ kHz. As shown in Fig. 13, the FC voltage ripples increase with the decrease of K, and the FC voltages v_{f1} and v_{f2} will deviate from each other if K is set to 0 at 0.6 s.

C. SENSITIVITY TO PARAMETER VARIATIONS

As illustrated in Section III, the proposed AVBC algorithm is realized by adjusting duty cycles of the HF switches, which may change the modulation signal slightly. In order to validate the sensitivity to parameter variations, two transient cases regard to variations of modulation index m and carrier frequency f_c are conducted.

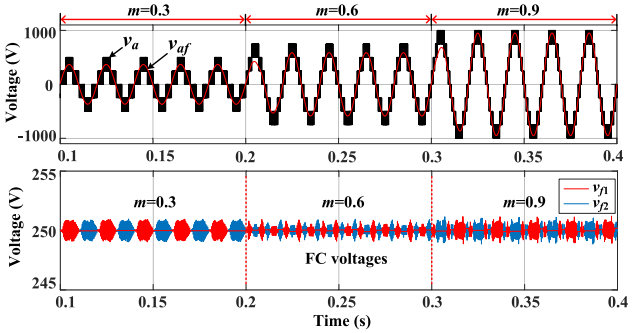

FIGURE 14. Transient results of 9L-HSMC with the hybrid PS-PWM and AVBC under different values of modulation index m ($K = 0.6$, $f_c = 2$ kHz).

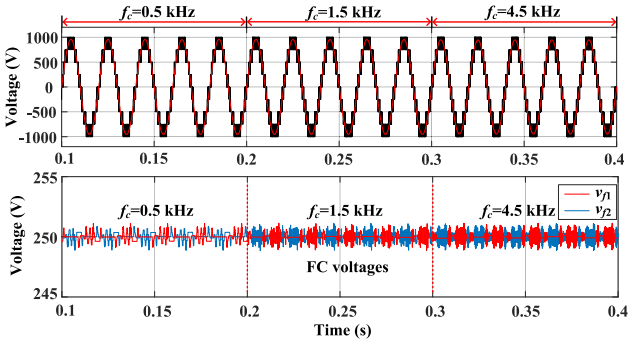

FIGURE 15. Transient results of 9L-HSMC with the hybrid PS-PWM and AVBC under different values of carrier frequency f_c ($K = 0.6$, $m = 0.9$).

Figs.14 and 15 show the transient results of 9L-HSMC with the hybrid PS-PWM and AVBC under variations of m and f_c, respectively. The waveforms shown are output voltage (v_a), fundamental component (v_{af}), and FC voltages (v_{f1}, v_{f2}). For Fig. 14, three values of modulation index $m = 0.3$, 0.6, and 0.9 are tested with $K = 0.6$ and $f_c = 2$ kHz. As can be seen in Fig.14, the FC voltages v_{f1} and v_{f2} are maintained balance, and the voltage deviation is not changed under different values of m. Fig. 15 shows waveforms obtained by using three values of carrier frequency $f_c = 0.5$ kHz, 1.5 kHz, and 4.5 kHz. Here, $K = 0.6$ and $m = 0.9$. It can be observed that the frequency of the FC voltages increases with the increase of f_c.

In both cases, the FC voltage is balanced and remained unchanged significantly even during the transient produced by the variations of m and f_c. Hence, the proposed AVBC is very robust in balancing the FC voltages, and the deviation of FC voltage does not depend on the values of the modulation index and carrier frequency.

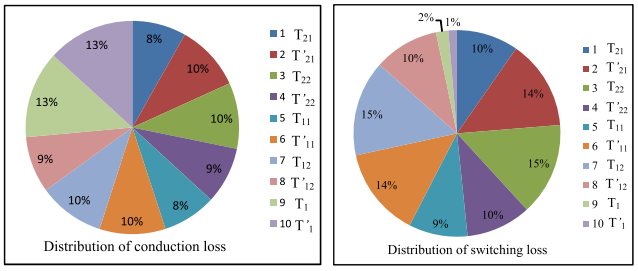

FIGURE 16. Distribution of power losses for 9L-HSMC. (a) Conduction losses, (b) switching losses ($m = 0.9$, $f_c = 2$ kHz).

D. POWER LOSSES ANALYSIS

This section investigates the power losses distribution of the 9L-HSMC with the proposed control strategy. Here, two main kinds of power losses are considered, namely conduction losses and switching losses [36], [37]. The conduction losses is related with ON-state equivalent resistance and forward voltage drop of switches and diodes, and they are expressed as

$$P_{con\_sw} = [V_T + R_T i(t)] \cdot i(t), \tag{33}$$

$$P_{con\_d} = [V_D + R_D i(t)] \cdot i(t), \tag{34}$$

where, V_T and V_D are the on-state voltage drops of the switch and diode, respectively, R_T and R_D are the on-state equivalent resistances,P_{con_sw} and P_{con_d} are conduction losses for a typical switch and diode. So total conduction losses P_{con} of the 9L-HSMC are obtained by

$$P_{con} = \frac{2}{T}\int_0^{T/2} \left[x(t)P_{con\_sw} + y(t)P_{con\_d}\right] d(t), \tag{35}$$

where $x(t)$ and $y(t)$ represent the number of switches and diodes in the current path. The switching losses can be calculated by using the linear approximation of voltage and current. The energy losses of switch k caused by turning-on and turning-off are calculated by

$$E_{on,k} = \int_0^{t_{on}} v(t)i(t)dt = \frac{1}{6}V_{sw,k}I't_{on}, \tag{36}$$

$$E_{off,k} = \int_0^{t_{off}} v(t)i(t)dt = \frac{1}{6}V_{sw,k}It_{off}, \tag{37}$$

where t_{on} and t_{off} are the turn-on and turn-off time of the switch, respectively. $V_{sw,k}$ is the off-state voltage of the switch k. $N_{on,k}$ and $N_{off,k}$ are the number of turn-on and turn-off switches during a fundamental cycle T. The total switching losses of the 9L-HSMC can be calculated by

$$P_{sw} = \frac{1}{T}\left[\sum_{k=1}^{N_{sw}}\left(\sum_{i=1}^{N_{on,k}} E_{on,k,i} + \sum_{i=1}^{N_{off,k}} E_{off,k,i}\right)\right]. \tag{38}$$

Fig. 16 shows the percentage of distributed power losses (conduction losses and switching losses) among ten switches for the 9L-HSMC. As shown in Fig. 16(a), the conduction loss percentage of LF switches in the 2L-HB is higher than that of HF switches in the 5L-SMC. Since the LF switches T_1 and T_1' of the 2L-HB are controlled to switch in fundamental frequency, the percentages of switching losses of T_1 and T_1' are less than 2%, as shown in Fig. 16(b).

Fig. 17 shows power loss distributions of IGBTs and diodes. It can be seen from Fig. 17 that the amount of switching losses is bigger than conduction losses for the HF switches, because they are switched in high frequency to balance the FC voltages. It is worth noted that the switching losses of the LF switches are negligible, which reduces the total power losses. The information of loss distributions is useful for the design of heat sinks. Moreover, it is possible to equip the HSMC by using power switches with different voltage ratings to exploit their advantages.

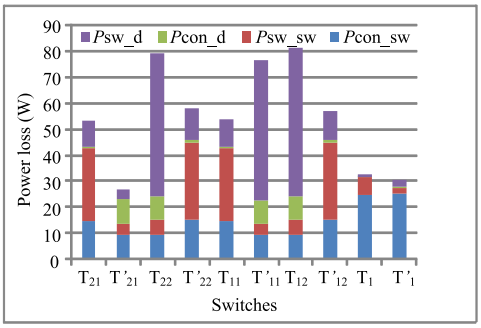

FIGURE 17. Power losses distribution of the 9L-HSMC. (*Psw_d*: diode switching loss, *Pcon_d*: diode conduction loss, *Psw_sw*: IGBT switching loss, *Pcon_sw*: IGBT conduction loss).

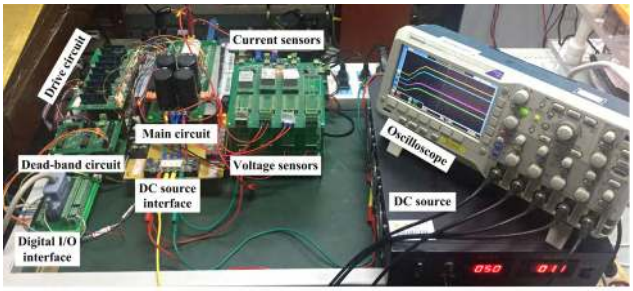

FIGURE 18. Experimental platform of the 9L-HSMC connected with linear *RL*-load.

V. EXPERIMENTAL VALIDATIONS

To validate the 9L-HSMC with the proposed control strategies, a small-scale experimental platform is built, as shown in Fig. 18. The experimental system is composed of main converter circuit, voltage and current sensing circuits, controller and PWM driving circuit. A real-time board/module MicroLAB is used to implement the ADC and control strategies. The converter dc bus is supplied with a constant dc source, and the ac-side terminals are connected to a linear resistor load through a filtering inductor ($L = 4.3$ mH, $R = 15\ \Omega$). The modified hybrid PS-PWM with carrier frequency $f_c = 2$ kHz and modulation index $m = 0.9$ is used by combing with the proposed AVBC strategy. The PWM gating signals of power switches are generated by the driving circuits and the dead-time circuit with an accurate dead time

between the gating signals of the complementary switches. The experiment parameters are listed in Table 5.

TABLE 5. Experiment parameters.

Symbols	Parameters	Values
V_{dc}	Dc-bus voltage	50 V
f_0	Output frequency	50 Hz
f_s	Sampling frequency	10 kHz
f_c	Carrier frequency	2 kHz
C_f	Flying capacitor	1 mF
C_{dc}	Dc-link capacitor	2200 μF
L	Filtering inductor	4.3 mH
R	Resistor load	15 Ω
t_d	Dead-band time	2.5 μs
K	Proportional factor	0.6

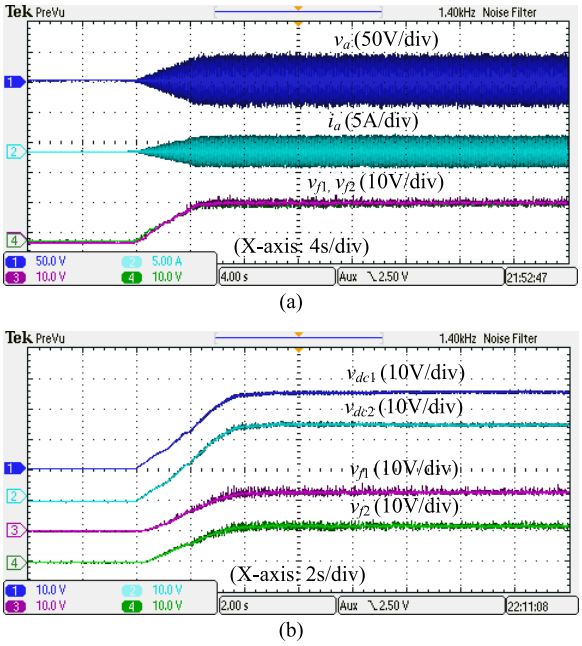

FIGURE 19. Experiment results during start-up process. (a) Output voltage, load current and FC voltage, (b) capacitor voltage.

A. RESPONSE TO START UP

Fig. 19 shows the response of the start-up process. Initially, the dc-bus voltage V_{dc} is zero, and then it has a slope increase to the nominal value 50 V after 4 s. The voltage of dc-link capacitor and FC increases to the reference values 25 V and 12.5 V after 4 s. The FC voltage is balanced with the proposed hybrid PS-PWM combined with AVBC strategy, even during the start-up transient process.

B. STEADY STATE PERFORMANCE

Fig. 20 shows the experiment results that are obtained under steady state, where $m = 0.9$ and $f_c = 2$ kHz. It can be seen from Fig. 20(a) that the output voltage v_a with nine levels and sinusoidal current i_a are obtained. As shown in Fig. 20(b), both the voltage of dc-link capacitor and the FC are balanced.

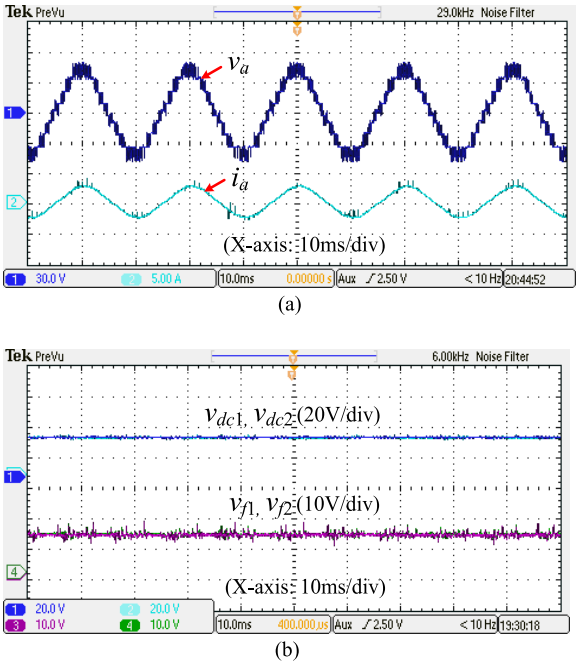

FIGURE 20. Steady-state experiment results. (a) Output voltage and load current, (b) dc-link capacitor voltage and FC voltage.

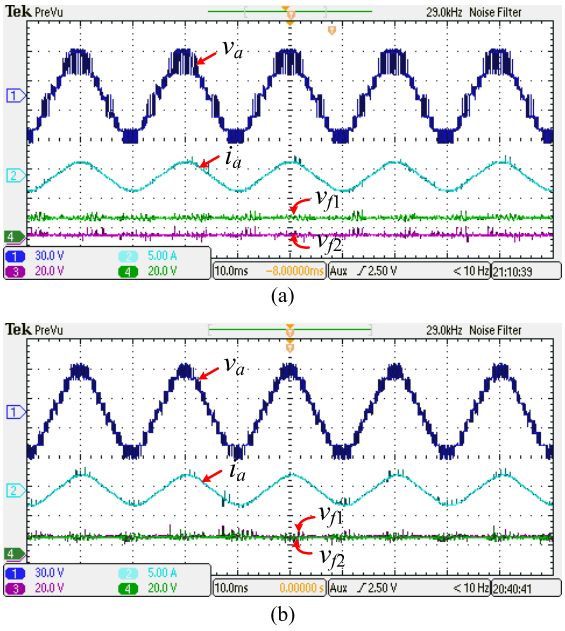

FIGURE 21. Experiment results under different control strategies: (a) hybrid PS-PWM without FC voltage balancing control, (b) hybrid PS-PWM combined with AVBC strategy.

Although some high-frequency switching components exist in the FC voltages, no voltage spikes and low-frequency voltage ripples are observed in the capacitor voltages.

Fig. 21 shows experiment results of the hybrid PS-PWM and the proposed control strategy, respectively. As shown in Fig. 21(a), the output voltage is distorted seriously due to the unbalanced FC voltages. Under the modified hybrid

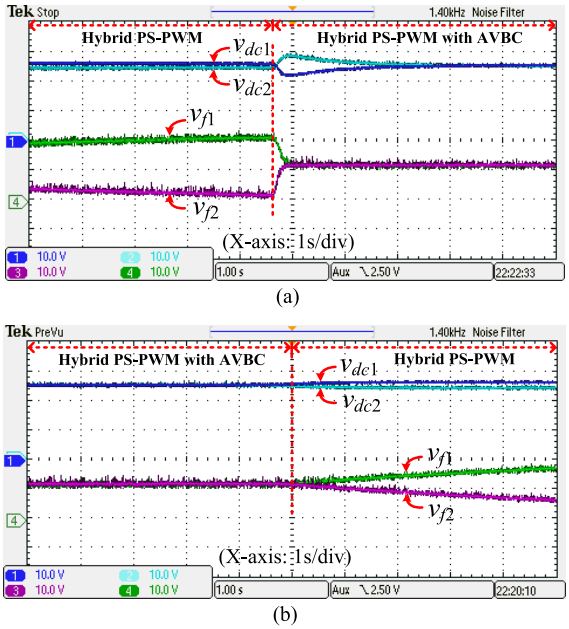

FIGURE 22. Dynamic response of capacitor voltage with step changes: (a) from hybrid PS-PWM to the proposed control strategy, (b) from proposed control strategy to hybrid PS-PWM.

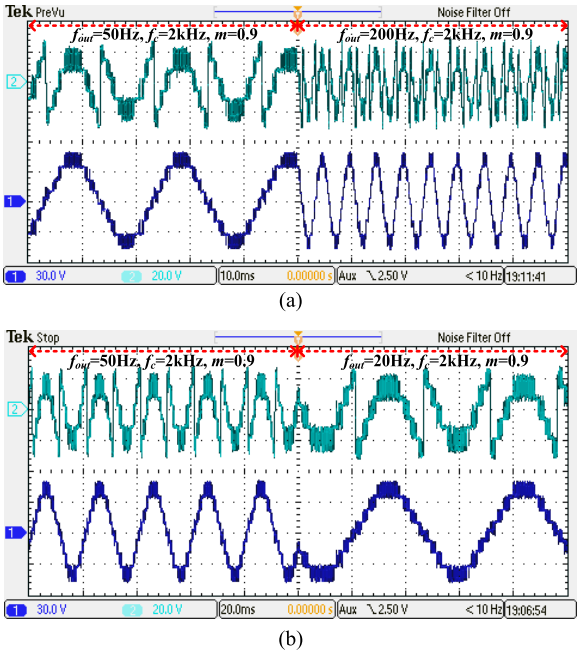

FIGURE 23. Experimental results with step changes of output frequency f_{out} from (a) 50 Hz to 200 Hz, (b) 50 Hz to 20 Hz.

PS-PWM combined with the AVBC strategy, the FC voltage is balanced, as shown in Fig. 21(b). Fig. 22 shows the FC voltage with step changing between two different conditions. As can be seen in Fig. 22, both the voltage of FC and dc-link capacitor recover balance rapidly under the proposed control strategy.

C. DYNAMIC PERFORMANCE

To further demonstrate the dynamic performance of the proposed control strategy, several transient cases are investigated. The responses of converter output to the transient cases are shown in Figs. 23 to 25.

Fig. 23 shows transient experiment results with step changes of output frequency f_{out}. Here, the f_c is 2 kHz and m is 0.9. For the purpose of comparison, the value of m changes from its nominal value 50 Hz to different frequencies 20 Hz and 200 Hz. It can be seen from Fig. 23 that the output is controlled in desired frequency, and no voltage spike is observed during the transient process.

Fig. 24 shows experiment results with step changes of m and f_c. The output voltage level will be adjusted according to the variation of m. When the value of m changes from 0.9 to 0.5, the $v_{ref\_}$ interacts with only two carriers during each half cycle. Then the voltage levels of v_{ao} and v_a degrade to five and seven, respectively. The experiment results with a step change at f_c from 500 Hz to 5 kHz are shown in Fig. 24(b). To make a tradeoff between the output quality and switching losses, the f_c is set as 2 kHz in this paper. Fig. 25 shows transient results with multiple changes of parameters f_{out}, f_c and m.

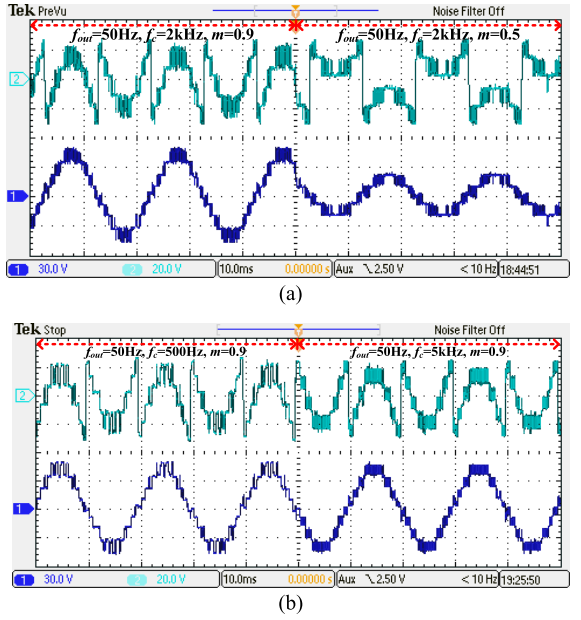

FIGURE 24. Experimental results with step changes of: (a) modulation index m from 0.9 to 0.5, (b) carrier frequency f_c from 500 Hz to 5 kHz.

As can be seen from Figs. 23 to 25, during step changes of multiple variables f_{out}, f_c and m, the desired output voltages v_{ao} and v_a are obtained quite well under the hybrid PS-PWM combined with AVBC strategy. The transient time is less than one half cycle, and no significant voltage spike is observed during the transient process. Hence, the proposed AVBC strategy is robust and the deviation of FC voltages is not influenced significantly with changes of system parameters, such as modulation index and carrier frequency.

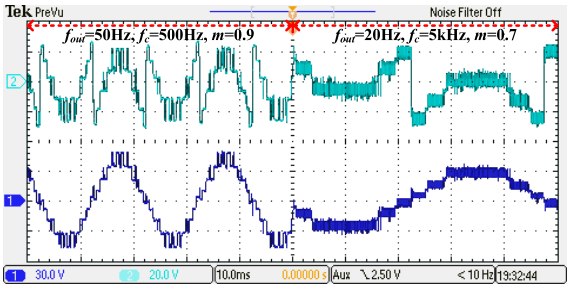

FIGURE 25. Experimental results of output voltage v_{ao} and v_a with changes of multiple parameters from $f_{out} = 50$ Hz, $f_c = 500$ Hz, $m = 0.9$ to $f_{out} = 20$ Hz, $f_c = 5$ kHz, $m = 0.7$.

VI. CONLUSIONS

In this paper, a hybrid PS-PWM with modified reference signal is developed and a new AVBC strategy is put forward to balance the capacitor voltage. With this control strategy voltage balancing of the NP is achieved naturally in a fundamental cycle and the FC voltage is balanced precisely. The switching frequency can be regulated flexibly by using the AVBC, and a relative constant switching frequency is obtained. The distribution of power losses for the HSMC are studied by using the PLECS toolbox. The switching losses of the LF switches occupy small proportion to the total losses and the percentage is less than 2% for each LF switch. The HSMC with hybrid PS-PWM and AVBC strategy has merits of superior output power qualities and low power losses. Due to the modularity, the proposed AVBC algorithm is easy to be extended to higher level HSMCs. Experiments under steady state and several transient states are conducted and verify the effectiveness of the proposed control strategies.

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JIANZHONG ZHANG (M'08–SM'16) received the M.Sc. and Ph.D. degrees in electrical engineering from the Department of Electrical Engineering, Southeast University, Nanjing, China, in 2005 and 2008, respectively.

From 2006 to 2007, he was a Visiting Scholar with the Department of Energy Technology, Aalborg University, Aalborg, Denmark. Since 2008, he has been with Southeast University, where he is currently a Research Professor with the School of Electrical Engineering. He was a Visiting Professor with the Worcester Polytechnic Institute, Worcester, MA, USA, in 2012. His research interests include electric machines, power electronics, and wind power generation.

Dr. Zhang was a recipient of the Institution Premium Award from the Institution of Engineering and Technology, U.K.

SHUAI XU (S'14–M'19) received the B.Sc. and M.Sc. degrees in electrical engineering from Henan Polytechnic University, Jiaozuo, China, in 2011 and 2013, respectively, and the Ph.D. degree in electrical engineering from the Department of Electrical Engineering, Southeast University, Nanjing, China, in 2018.

From 2016 to 2017, he was a joint Ph.D. Student with the Department of Electrical and Computer Engineering, The University of British Columbia, Vancouver, BC, Canada. He is currently with the School of Electrical Engineering and Electronic Information, Xihua University, Chengdu, China. His research interests include multilevel converters, advanced modeling, fault diagnosis, and fault-tolerant control.

XING HU (S'15) received the B.Eng. degree in electrical engineering from Anhui University, Hefei, China, in 2013. He is currently pursuing the Ph.D. degree with the Department of Electrical Engineering, Southeast University, Nanjing, China.

Since 2018, he has been a Guest Ph.D. Student with the Department of Energy Technology, Aalborg University, Aalborg, Denmark. His research interests include modular multilevel converters, VSC-HVDC, fault diagnosis, and fault-tolerant control.

YAODONG ZHU received the M.Sc. and Ph.D. degrees in test measurement technology and instrument from the Department of Automation, Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2000 and 2003, respectively. Since 2005, he has been with Jiaxing University, where he is currently an Associate Professor with the School of Mechanical and Electrical Engineering. His research interests include smart robot, embedded computing, and computer vision.