Research Article

Voltage Mode Pulse Width Modulator Using Single Operational Transresistance Amplifier

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This paper presents a voltage mode pulse width modulator (PWM) using single operational transresistance amplifier (OTRA). The proposed PWM consists of a relaxation oscillator output which is modulated using modulating signal. PSPICE simulation results and experimental results have been included to verify the theoretical analysis.

1. Introduction

Pulse width modulation (PWM) scheme is widely used in communication systems, DC motor speed controller, power conversion control circuits [1–3], and instrumentation. In PWM, the width of pulses of a pulse train is changed in accordance to voltage level of modulating signal. The PWM generators are available in Integrated Circuits (ICs) form; however, the internal circuitry is somewhat complex and typically consists of current sources, flip-flop, comparators, and analog switches [4]. Apart from these readily available ICs, the PWM signal can most commonly be generated by comparing a modulating signal with a sawtooth or triangular waveform. Alternatively, information signal can first be combined with a sawtooth or triangular waveform and thereafter comparing the combined signal with a reference level to generate PWM signal. This can be implemented using a Schmitt trigger with an RC circuit in feedback loop [5]. Extensive literature review reveals that PWMs based on this concept are available using different active analog building blocks such as op-amps [6], current conveyor II (CCII) [4], and operational transconductance amplifier (OTA) [7, 8]. High-frequency performance of PWMs employing op-amps is limited due to lower slew rate and constant gain-bandwidth product of the op-amps. The CCII-based PWM has the advantage of generating accurate PWM signal with

high operating frequencies [4], and the output amplitude and frequency of the PWMs based on OTAs can be independently/electronically tuned [7]. Despite these advantages, the circuits proposed in [4, 7] suffer a drawback of using excessive number of active elements. Reference [8] presents another OTA-based PWM which uses derivative method. In derivative method, the duty cycle of PWM signal depends on a differentiated result of the modulating signal. This method is not suitable for applications where the changes in modulating signal are rare, such as in power converters [7]. The open literature suggests that a PWM pulse train can also be produced with the use of voltage-controlled delay lines [9], current-controlled delay cells [10], and voltage-controlled phase shifter [11] wherein the underlying concept is not the same as used in [4–8]; that is, the comparison of modulating signal with reference triangular/sawtooth waveform [9] uses two voltage-controlled delay lines, a fixed delay element, two rising edge detectors, along with an RS latch to generate a 0%–50% duty cycle at the output of the latch. Two 0%–50% modulators are connected in parallel to extend the duty cycle to 100%. Current-controlled delay cell-based duty oscillator and pseudohyperbola charge current generator are used in [10] for generating PWM. Yet, another PWM is proposed in [11] which employs a voltage-controlled phase shifter, a two-input logic AND gate, a network of logic inverters, and FET

switches. This circuit generates a 0% to 50% pulse width using the phase shifter and an AND gate and then extends the range to 0%–100% using the inverters.

This paper aims at presenting an operational transresistance amplifier (OTRA) based PWM, using a relatively simpler scheme, wherein the modulating signal is combined with an exponential carrier waveform and compared with a reference. This paper is organized as follows. In Section 2, the function of an OTRA is briefly described, followed by the operation principle of the proposed PWM circuit. The feasibility of the presented circuits is verified through circuit simulations and experimental results in Section 3. It is observed that the simulation and experimental results are in close agreements with theoretical propositions. The comparison of the proposed circuit with earlier reported structures is presented in Section 4. Section 5 concludes the paper.

2. Circuit Descriptions

OTRA is a high gain current input voltage output device. The input terminals of OTRA are internally grounded, thereby eliminating response limitations due to parasitic capacitances and resistances and, hence, are appropriate for high-frequency operation. The circuit symbol of OTRA is shown in Figure 1, and the port characteristics are given by (1), where R_m is transresistance gain of OTRA. For ideal operations, the R_m of OTRA approaches infinity and forces the input currents to be equal. Thus, OTRA must be used in a negative feedback configuration. Consider

$$\begin{bmatrix} V_p \\ V_n \\ V_o \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ R_m & -R_m & 0 \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ I_o \end{bmatrix}. \tag{1}$$

The general scheme of PWM is depicted in Figure 2. The modulating signal and carrier signal are first summed up, and then PWM output signal is generated by comparing the summation signal and reference level.

The proposed PWM circuit is shown in Figure 3. The circuit consisting of OTRA, resistors R_F and R_L, and capacitor C serves as square wave generator. Exponential voltage waveform across capacitor C serves as carrier waveform. The modulating signal v_i and the carrier wave are summed up at node p through resistor R_s. Thus, the voltage across the capacitor will be summation of carrier and modulating signal, and the PWM output is available at v_o.

The resistor R_F and capacitor C form a positive feedback loop. V_{sat}^+ and V_{sat}^- are the two possible saturation levels of output v_0. Assume initially that v_0 switches to saturation level V_{sat}^+ at $t = 0$, as shown in Figure 4. This results in charging of the capacitor present in the feedback loop, and the voltage across the capacitor reaches V_{TH}, a value at which I_p, the current through p terminal, becomes slightly less than the current through n terminal, I_n. As a result, the output voltage switches to V_{sat}^-, and the capacitor starts charging in the opposite direction. Now, as capacitor voltage approaches V_{TL}, the output once again switches back to V_{sat}^+.
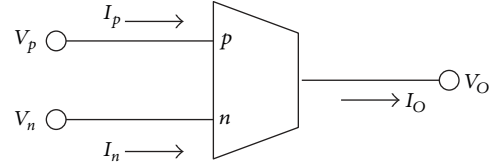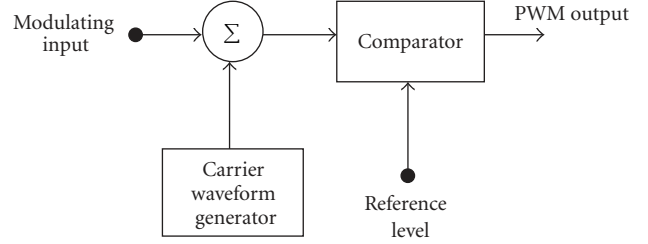

Figure 1: OTRA circuit symbol.

Figure 2: The scheme of PWM [4].

The V_{TH} and V_{TL} values can be obtained from the routine analysis of this PWM circuit and are expressed by (2) and (3), respectively. Consider

$$V_{TH} = V_{sat}^+ \left(1 - \frac{R_F}{R_L} \right) + v_i(t) \frac{R_F}{R_S}, \tag{2}$$

$$V_{TL} = V_{sat}^- \left(1 - \frac{R_F}{R_L} \right) + v_i(t) \frac{R_F}{R_S}. \tag{3}$$

These values of V_{TH} and V_{TL} result in T_{on} and T_{off} as follows:

$$T_{on} = R_F C \ln \frac{[2R_L/R_F - 1] - v_i(t) R_L/V_{sat}^+ R_S}{[1 - v_i(t) R_L/V_{sat}^+ R_S]}, \\ T_{off} = R_F C \ln \frac{[2R_L/R_F - 1] - v_i(t) R_L/V_{sat}^- R_S}{[1 - v_i(t) R_L/V_{sat}^- R_S]}. \tag{4}$$

The overall period of the modulated output is given by

$$T = T_{on} + T_{off}, \tag{5}$$

and the duty factor (D) can be computed as

$$D = \frac{T_{on}}{T} \times 100\%. \tag{6}$$

Equation (4) shows that the duty cycle of the output can be controlled with the help of modulating signal $v_i(t)$.

3. Realizing an OTRA and Nonideality Analysis

For the proposed PWM circuit, the OTRA was realized using AD844 CFOA IC as shown in Figure 5 [12]. The equivalent circuit of Figure 5 for nonideal analysis [13] is presented in Figure 6. The CFOAs have been replaced with current conveyors having finite input resistances (R_X) and finite
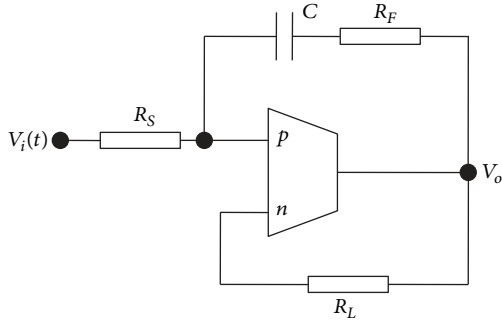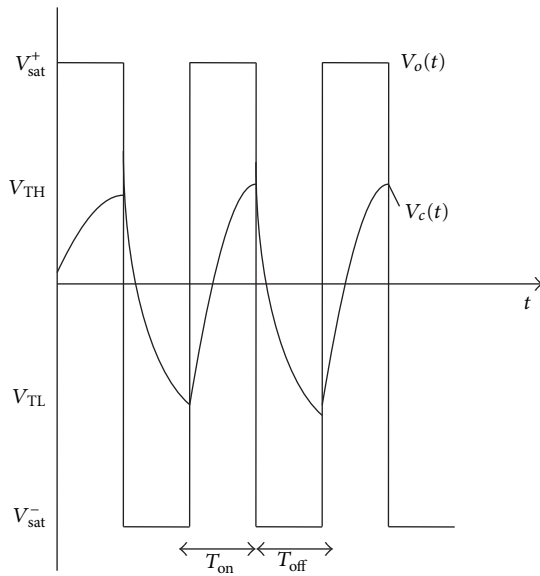
Figure 3: The OTRA PWM circuit.

Figure 5: OTRA constructed with AD844.

Figure 4: Output of the square wave generator of Figure 3.

Figure 6: Equivalent circuit of OTRA constructed with AD844.

resistance at its Z terminal (R_Z). Ideally, the input resistance at the X terminal is zero and is infinite at the Z terminal. For the AD844 CFOA, the input resistance R_X is around $50\,\Omega$, and R_Z is around $3\,M\Omega$ [14].

From Figure 6, various currents can be calculated as follows:

$$I_{Z1} = I_+,$$

$$I_D = I_{Z1}\left(\frac{R_Z}{R_X + R_Z}\right),$$

$$I_{X2} = I_- - I_D,$$

$$I_{Z2} = I_{X2}.$$

(7)

Ideally, I_D should be equal to I_{Z1}, which can be approximated only if $R_Z \gg R_X$, which is true for AD844. Also,

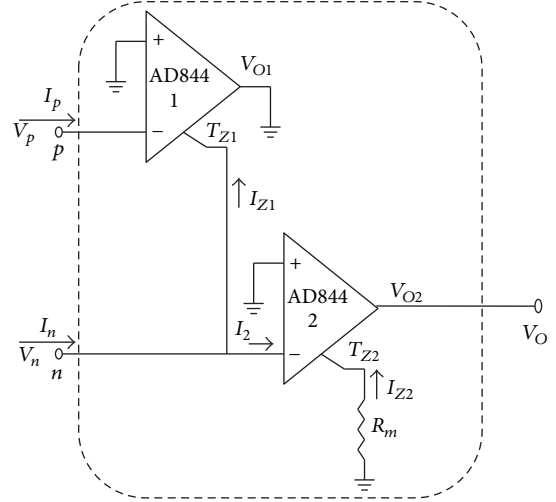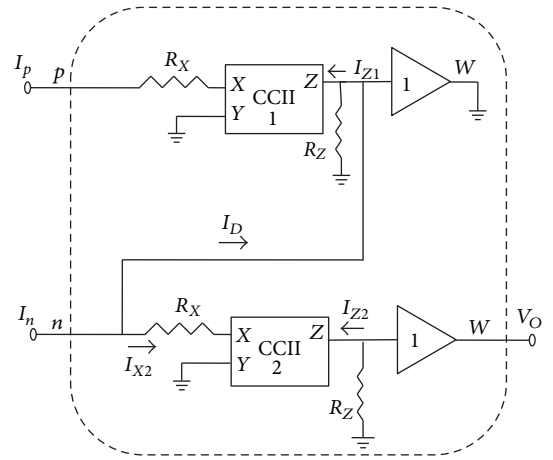the approximation that the input terminals are virtually grounded will be true only if the external resistance at the input terminal of the OTRA is much larger than R_X. If these two conditions are satisfied, the OTRA constructed with AD844 closely approximates an ideal OTRA.

From (7), the output voltage V_O, taking into account the previously mentioned approximations, can be calculated as

$$V_O = (I_+ - I_-)R_Z,$$

(8)

where R_Z is the transimpedance gain of the OTRA.

If in PWM circuit shown in Figure 3 the equivalent circuit of OTRA constructed with AD844 is used, then the threshold limits of the output get modified to

$$V_{TH} = V_{sat}^+\left(1 - \frac{R_F + R_x}{R_L + R_X//R_Z}\right) + v_i(t)\,\frac{R_F + R_x}{R_S + R_x},$$

(9)

$$V_{TL} = V_{sat}^-\left(1 - \frac{R_F + R_x}{R_L + R_X//R_Z}\right) + v_i(t)\,\frac{R_F + R_x}{R_S + R_x}.$$

(10)

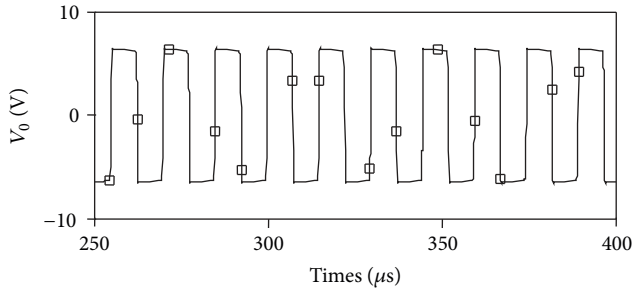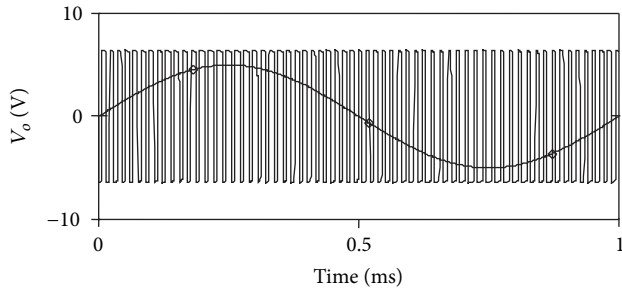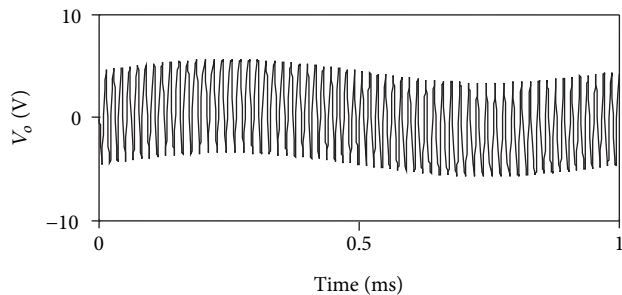Figure 7: PWM output without modulating signal.

(a) Modulating signal and PWM output signal

(a) Modulating signal and PWM output signal

(b) Summed up modulating and carrier signals

(b) Summed up modulating and carrier signals

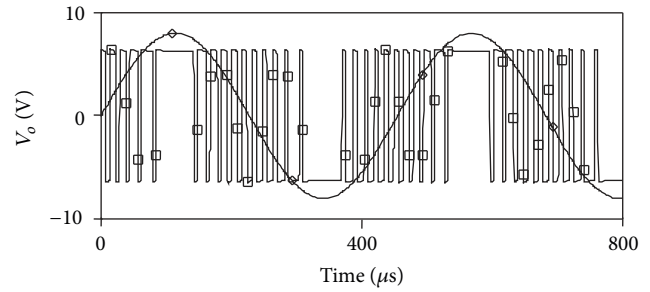Figure 9: PWM output of for 8 V, 2.2 KHz modulating signal.

Figure 8: PWM output for 5 V, 1 KHz sinusoidal modulating signal.

The external resistance at the input of the OTRA should be much larger than R_X so that the feedback current can be absorbed into the input terminals. Since R_L, R_F, R_S, and $R_Z \gg R_X$, Equations (9) and (10) reduce to (2) and (3), respectively.
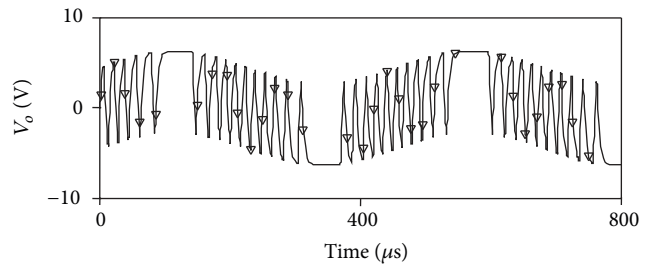
4. Simulation and Experimental Results

The proposed circuit is simulated using PSPICE. OTRA is realized using current feedback operational amplifiers (CFOAs) IC AD844 as shown in Figure 5. Macro model of AD844 is used for simulations. Figure 7 shows the output voltage of the PWM when modulating signal is not applied, for $R_F = 20\,\text{K}\Omega$, $R_L = 70\,\text{K}\Omega$, $R_S = 80\,\text{K}\Omega$, and $C = 200\,\text{pF}$, and corresponds to a 50% duty cycle. The observed output frequency is 66.7 KHz as against the calculated value of 69.7 KHz.

Simulated output of pulse width modulator, with same component values as used in Figure 7, is shown in Figure

8 for a 5 V, 1 KHz sinusoidal modulating signal. Figure 8(a) shows the modulating signal and the PWM output, and summation of modulating and carrier wave is depicted in Figure 8(b). Figures 9 and 10 show the output of pulse width modulator for an 8 V, 2.2 KHz modulating signal and 5 V, 40 KHz modulating signal, respectively, for same set of component values. Frequency spectrum of the pulse width modulator for 8 V, 2.2 KHz modulating signal is shown in Figure 11 which consists of modulating component and carrier signal. Thus, the modulating signal can be recovered with the help of appropriate low pass filter.

Figure 12 shows the variation of theoretically computed and simulated % duty factor of the modulator with the applied input signals. This shows that the two results closely match with each other.

The functionality of the proposed pulse width modulator circuits is verified through hardware as well.

The commercial IC AD844AN is used to implement an OTRA. Supply voltages used are ±5 V. Figure 13 shows typical experimental results of the circuit for two different modulating signals. Figure 13(a) depicts output for component values $R_F = 20\,\text{K}\Omega$, $R_L = 70\,\text{K}\Omega$, $R_S = 80\,\text{K}\Omega$ and $C = 200\,\text{pF}$ and for an 8 V, 2.2 KHz modulating signal. Another screen shot of oscilloscope is shown in Figure 13(b) for a high-frequency modulating signal of 40 KHz with 5 V amplitude. These experimental results are in close agreement to simulated results.

TABLE 1: Comparison between the proposed and the previously reported works.

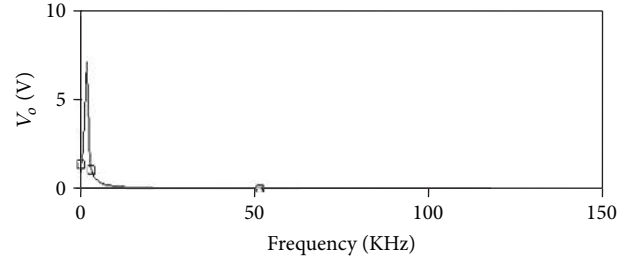| References	no. of active components	No. of passive components	Carrier signal type	Electronic tunability
[4]	Single CC-II, two op-amps	Single capacitor, three resistors	Triangular	No
[6]	Single op-amp	Single capacitor, three resistors	Exponential	No
[7]	(i) Two OTAs, an inverter, and a MOS switch	(i) Single capacitor, single resistor	(i) Sawtooth	Yes
	(ii) Four OTAs and an inverter	(ii) Single capacitor, single resistor	(ii) Triangular	Yes
[8]	Three OTAs	Single capacitor, two resistors	Triangular	Yes
Proposed	Single OTRA	Single capacitor, three resistors	Exponential	No
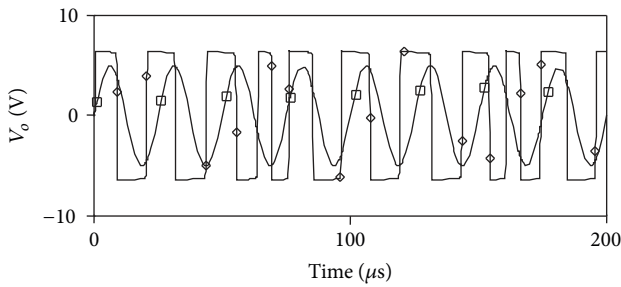
(a) Modulating signal and PWM output signal
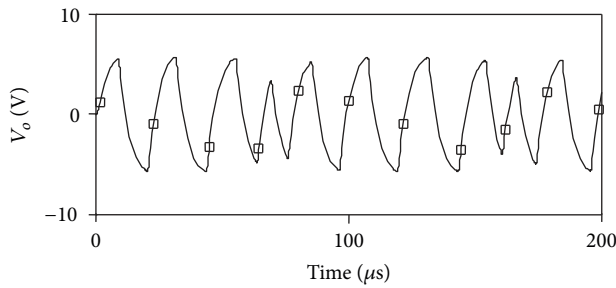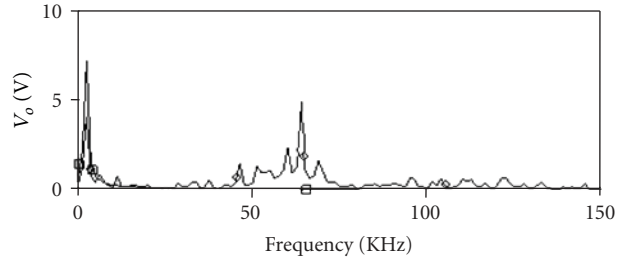

(b) Summed up modulating and carrier signals

FIGURE 10: PWM output for 5 V, 40 KHz modulating signal.

(a) Frequency spectrum of modulating signal

(b) Frequency spectrum of modulated signal

FIGURE 11: Frequency spectrum of the PWM.

5. Comparison

In this section, a comparison of the proposed work with the previously reported analog PWM circuits [4, 6–8] is presented, which are all based on the concept of comparing a modulating signal with a reference sawtooth or triangular waveform to generate PWM signal. Table 1 shows the detailed comparison. The study of Table 1 reveals that topologies presented in [4, 7, 8] use more number of active components as compared to the proposed work. The proposed circuit is simpler as compared to the topologies of [4, 7, 8], since it uses the exponential voltage waveform across the capacitor of the square wave generator as carrier wave and, hence, does not require additional circuitry needed for triangular/sawtooth waves. Though exponential carrier wave being a nonlinear signal yields

relatively inaccurate PWM signal at lower carrier frequencies as compared to the triangular/sawtooth wave, yet one can trade off accuracy for simplicity depending upon the application.

The PWM topology of [6], which is a classical opamp-based design, uses same number of active and passive components as in proposed circuit. However, the opamp-based circuits show limited high-frequency performance due to lower slew rate and constant gain-bandwidth product of the op-amps. Additionally, the input terminals of OTRA being virtually grounded, the proposed circuit is free from parasitic effects.

6. Conclusion

In this paper, single OTRA-based PWM generator, a nonlinear application of OTRA, is proposed. This circuit can be used for speed control of DC motors and for DC-DC converters.
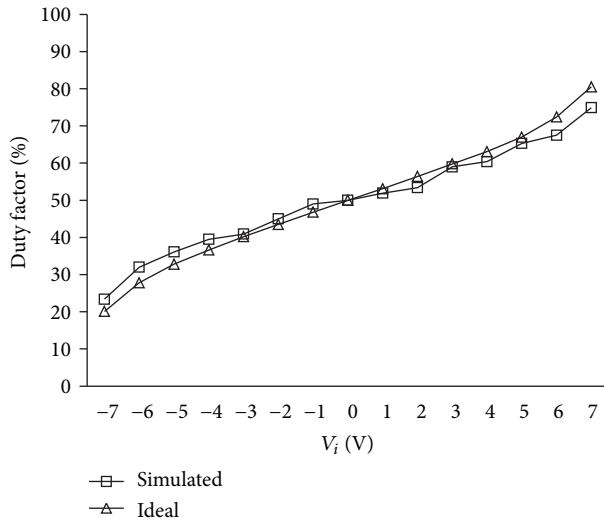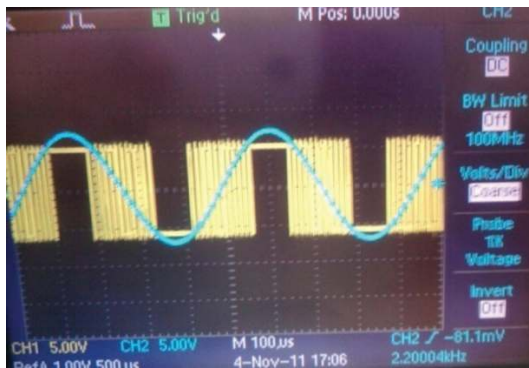
Figure 12: Variation of duty factor with applied input signal.

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(a) PWM output for an 8 V, 2.2 KHz modulating signal

(b) PWM output for a 5 V, 40 KHz modulating signal

Figure 13: Experimental results of the proposed PWM.

PSPICE simulation results using AD844 macromodel and experimental results have been included for verification of the theoretical propositions which are found in close agreement.

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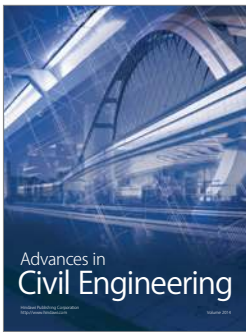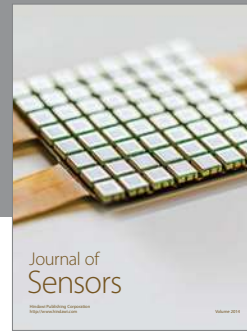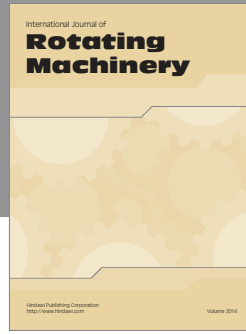
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