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# Voltage Sag Detection based on Rectified Voltage Processing

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**Abstract** – An algorithm for voltage sag detection based on rectified voltage processing is presented and its performances are evaluated by means of simulated and real voltage waveforms (recorded at some Low Voltage busbars and measured on a scaled prototype of a voltage support system). The algorithm is intended to detect voltage sag occurrence and to trigger the disconnection of the faulty supply network and subsequently the connection of a voltage support system. The algorithm is very convenient in terms of memory storage and computational requirements and may be implemented on low cost platforms. The results show that the time for detection is very short and always less than a quarter of the supply voltage period.

**Index Terms** – Industrial power system transients, Power conditioning, Signal detection

## I. INTRODUCTION

A voltage sag is a reduction of the voltage at a customer position with a duration of between one cycle and a few seconds [1]. Voltage sags are caused by motor starting, short circuits and fast reclosing of circuit breakers. Voltage sags normally do not cause equipment damage, but can easily disrupt the operation of sensitive loads such as adjustable-speed drives, static converters supplied loads, etc. [2,3,4].

Voltage sags are much more common than voltage interruptions, since they can be associated with faults remote from the customer. Even voltage sags lasting only 4 - 5 cycles can cause sensitive equipment to malfunction [5,6,7]. A great effort has been devoted to define voltage sag characteristics and statistical properties together with the assessment of the sensitivity of important loads [8,9,10]. Several power quality surveys may be found in the literature [10-13].

As stated in [10], voltage sags which may impact equipment are usually caused by faults on the power system. Motor starting also results in voltage sags, but the magnitudes are usually not severe enough to cause equipment misoperation.

Several solutions have been conceived for sensitive loads, depending on several factors [4,8,9,10]. For the solutions which imply one or more static converters, switched onto the supply network to feed the load in case of voltage sag or voltage interruption, a key role is played by the time for the detection of the voltage sag and the duration of the switching operation. Depending on the characteristics of the sensitive load, the requirements on the intervention time may be very severe. Moreover, the choice of algorithm/techniques for

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voltage sag detection is highly dependent on the real-time requirements, on the available computational hardware and on the amount of computational effort. Several approaches have been proposed in the literature for voltage sag analysis and detection [14-18]. The algorithms appearing in the literature are based on 1) Short Time Fourier Transform, 2) analog or digital filters banks, 3) wavelet transform using different wavelet kernels, 4) neural network classifiers and 5) fractal base methods. The critics which are moved to the first two more “classical” approaches are typically that first, the Fourier transform is less efficient in tracking the signal dynamics and that it relies on a uniform window, whichever the frequency components distribution, and second, linear filters generate signal phase delay and slow time response of the detection algorithm. On the contrary, the critics which may be moved to the other three approaches are that first, they require a considerable computational effort (in terms of computational time and memory storage), in particular neural network classifiers, second, their response has not been tested in the presence of a disturbed signal (i.e. the supply voltage waveform under the assumption of a fairly high value of the Total Harmonic Distortion index, like for weak rural distribution feeders or dedicated industrial feeders) and third, these approaches are typically adopted for classification tasks (as clearly stated in [18]), which are performed by means of off-line computational procedures without severe real-time requirements.

## II. RECTIFIED VOLTAGE ALGORITHM

The Rectified Voltage (RV) algorithm is based on the comparison of the instantaneous rectified voltage  $r(n)$  (which may be obtained with a low power diode bridge or with maximum operation performed at software level) with a reference rectified voltage  $rr(n)$ , obtained using a moving average FIR (Finite Impulse Response) filter. The comparison is performed using an adjustable threshold  $\alpha$ . The algorithm operates on the rectified voltage only, instead of all the three-phase input voltages, to save computational time and memory storage. The structure of the algorithm is shown in Fig. 1.

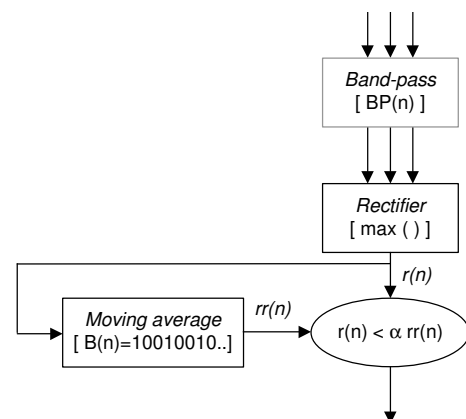


Fig. 1. Block diagram of the RV algorithm

The algorithm may be simplified if the reference signal  $rr(n)$  is assigned the rated no-load rectified voltage given by

$$rr(n) = 1.35 V_{ll,rms} \quad (1)$$

The “moving average”  $B(n)$  filter is used to obtain a reference signal  $rr(n)$ , which is updated online by the real average rectified voltage. The filter structure is conceived as a repetitive sequence ( $M$  times) of a nonzero coefficient followed by  $P-1$  zeros (the zero coefficients are inserted to save computational time); in this case the depth of the filter is  $M(P-1)$  samples, but the operations necessary to perform filtering are only those corresponding to the nonzero coefficients. The  $B(n)$  filter is a FIR filter with the following general structure

$$B(n) = \begin{cases} 0 & n \neq Pk, \quad k \text{ integer} \\ 1 & n = Pk, \quad k \text{ integer} \end{cases} \quad (2)$$

where

$P$  is the length of a single averaging cell in number of samples;

$M$  is the length of the filter impulse response in number of samples.

An ageing factor  $1/\beta$  is also included in the more general version of the filter. In the present implementation of the RV algorithm the sampling frequency is 5 kHz.

$$B(n) = \begin{cases} 0 & n \neq Pk, \quad k \text{ integer} \\ 1/\beta & n = Pk, \quad k \text{ integer} \end{cases} \quad (3)$$

The algorithm was implemented in C language as a routine on a Texas Instruments TMS 320C40 DSP board. The routine length is 150 code lines and the execution time is around 10  $\mu$ s, with a total cycle time of 500  $\mu$ s. The same board performs other tasks like the control of the inverter modulator and the switching in and out of the Compensation Electronic System.

### III. PRELIMINARY PERFORMANCE EVALUATION

Preliminary tests were performed at the design stage to set the optimal values of the algorithm parameters, taking into account the size of the FIR filter (for memory storage and computational effort), the immunity to unwanted network disturbances (controlled by keeping the sampling frequency as low as possible), the detection performances in terms of first, number of “successful detections” and second, number of detections” with respect to the total number of tests.

The parameter  $M$  was set preliminarily to 5 times  $P$ , which leads to  $B(n)$  size of 15, 50 and 150 samples (if the values reported in Table I are considered), that is 3 ms, 10 ms and 30 ms, for a sampling time of 200  $\mu$ s (which is implemented later in the prototype).

TABLE I  
PARAMETERS USED IN THE TESTS

Parameter	Value
Moving average filter length ( $M$ )	5P
Moving average filter step ( $P$ )	3, 10, 30

A voltage sag of 90% depth is applied in Fig. 2, where three configurations of the RV algorithm are tested to determine the optimal choice of the algorithm parameters.

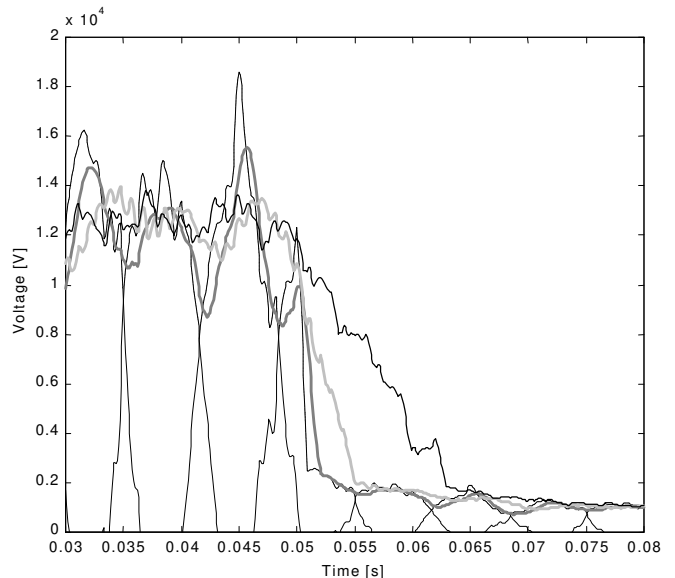


Fig. 2 Response to the reference voltage sag (no ageing factor):  
 $M=5P$ ,  $P=3$  (dark grey),  $P=10$  (light grey),  $P=30$  (black)

The black dotted curves indicate the three line-to-line voltages and the rectified voltage  $r(n)$ ; it is evident the effect of the very high THD adopted for the simulation (8%).

The instantaneous value of  $r(n)/rr(n)$  (by which the threshold  $\alpha$  may be determined) is computed in Fig. 3 for the test case of Fig. 2.

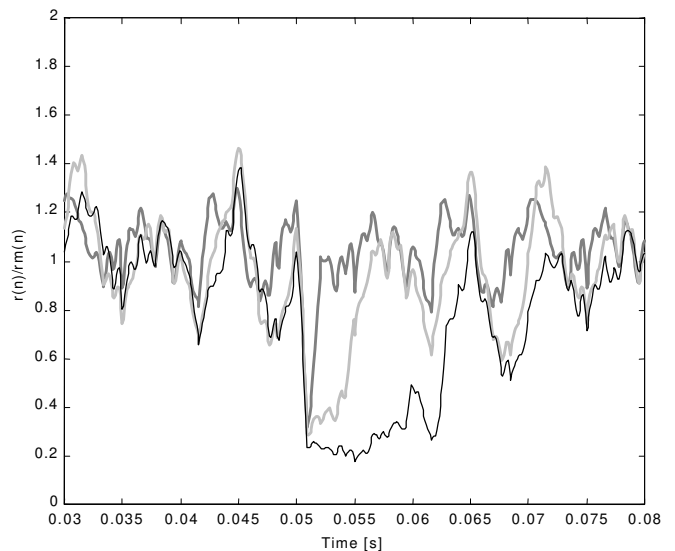


Fig. 3 Instantaneous value of the ratio  $\alpha(n) = r(n) / rr(n)$  (no ageing factor):  
 $M=5P$ ,  $P=3$  (dark grey),  $P=10$  (light grey),  $P=30$  (black)

Several tests were performed with the  $P$  values reported in Table I, with random phase of supply harmonics and different THD values. It was evident that a low  $P$  value gives a very fast tracking algorithm, but the number of “false increases and the algorithm performance is affected heavily by network THD. Yet, a larger  $P$  value increases the robustness of the algorithm with respect to impulsive disturbances. A trade-

off is the choice  $P=10$ , which corresponds in the actual implementation to half of a supply voltage period.

The parameters are then set to  $P=10$  and  $M=5P, 10P$  and  $20P$  and then a test is repeated with the introduction of the ageing coefficient  $1/\beta$  set to 0.33.

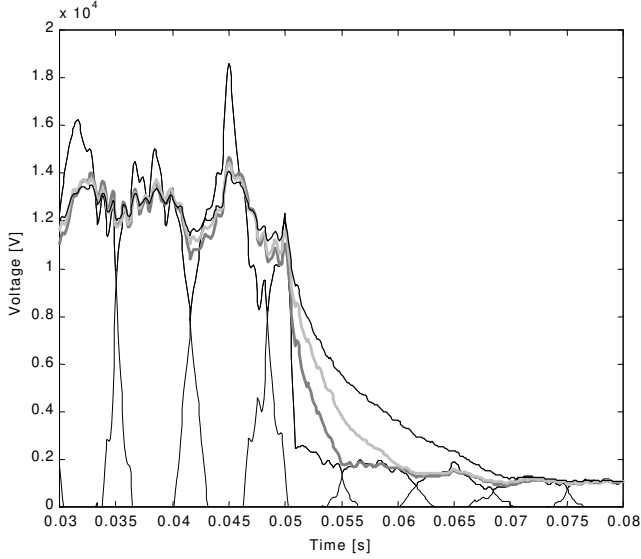


Fig. 4 Response to the reference voltage sag (ageing factor  $1/\beta=0.33$ ):  $P=10$ ,  $M=5P$  (dark grey),  $M=10P$  (light grey),  $M=20P$  (black)

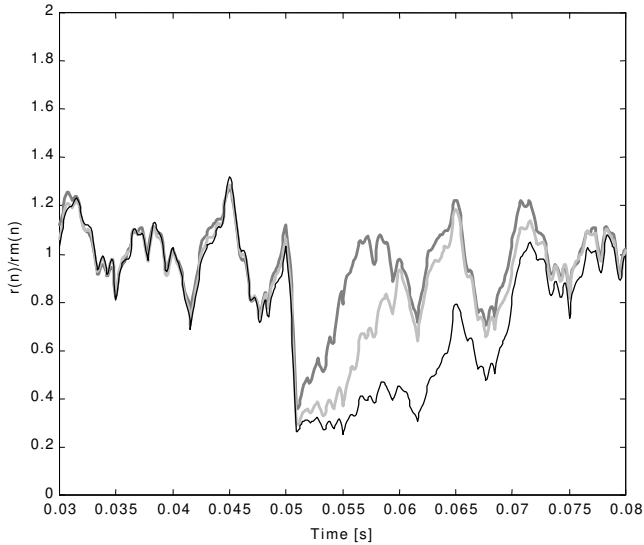


Fig. 5 Instantaneous value of the ratio  $\alpha(n) = r(n) / rm(n)$  (ageing factor  $1/\beta=0.33$ ):  $M=5P$ ,  $P=3$  (dark grey),  $P=10$  (light grey),  $P=30$  (black)

The introduction of the ageing coefficients improves the shape of the algorithm response, as it is evident in Fig. 4. Yet, it increases the computational effort and it doesn't improve the algorithm performances if the threshold  $\alpha$  is chosen wisely.

The examination of the results shown in Fig. 3 and 5 leads to set  $\alpha$  value around 0.5-0.6. Larger values of  $\alpha$  are not advisable, since the benefit from the point of view of the response delay is negligible, while the risk of false sag detection increases dramatically.

#### IV. TEST RESULTS

Tests on the algorithm response to simulated and real voltage sags are then performed using:

1. artificial three-phase test signal generated at a specified THD (ranging from 2% up to 8%), with the amplitude of harmonic components proportional to the limits indicated in the standard EN 50160 [23] and random phase with uniform distribution; the voltage sag is of variable amplitude between 10% and 100% (voltage interruption), occurring always at  $t=50$  ms;
2. three-phase voltages recorded at voltage sags occurrence;
3. three phase voltages with fault induced on a prototype system in the laboratory;

##### A. Test with artificial voltage sag waveforms

The results of the test performed on artificial sag waveforms is shown in Fig. 6 (the residual voltage is 10% and the sag transient duration is 1 ms), where the normalised rms value of the line voltage is shown together with the output of the RV algorithm.

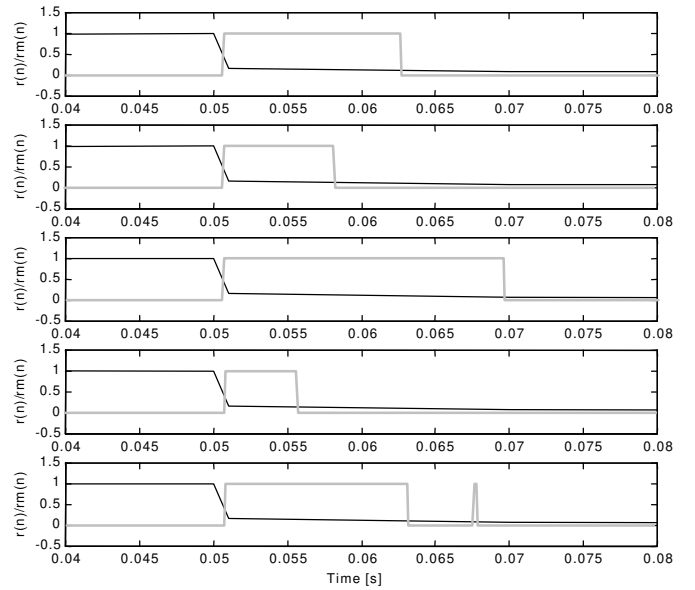


Fig. 6 Normalised rms value of the line-line voltage (THD=8%) and RV algorithm output: (top to bottom)  $P=30$  and  $M=5P$ ,  $P=10$  and  $M=10P$ ,  $P=10$  and  $M=20P$ ,  $P=10$  and  $M=10$  ( $1/\beta=0.33$ ),  $P=10$  and  $M=20P$  ( $1/\beta=0.33$ )

For the considered voltage waveform the RV algorithm detects the artificial voltage sag after less than 1 ms for all the choices of the algorithm parameters.

Several tests were performed for variable sag depth (80%, 70%, 50%, 30% and 10%), random phase distribution of supply voltage harmonics and different instants of voltage sag occurrence. The threshold  $\alpha$  is set to 0.54. The results of the statistical evaluation are shown in Table II.

TABLE II  
RESULTS OF THE STATISTICAL EVALUATION

Parameter	Residual voltage				
	10%	30%	50%	70%	80%
False detections	1/500	4/500	6/500	3/500	4/500
Missed detections	6/500	0/500	0/500	0/500	17/500
Detection time: mean [ms]	1.5	1.1	2.3	3.3	4.0
Detection time: std. dev. [ms]	1.2	0.84	2.0	1.6	1.5

##### B. Test with recorded waveforms

The results of two tests performed with voltage sag waveforms recorded at the secondary winding of a Medium

Voltage/Low Voltage transformer are shown in Fig. 7 and Fig. 8. These waveforms were recorded at low sampling rate (500 Hz), so that an extensive analysis of the benefits obtained by increasing the RV algorithm sampling rate is not possible.

For these tests the reference signal  $rr(n)$  was held constant as indicated by (1) without any “moving average” filter.

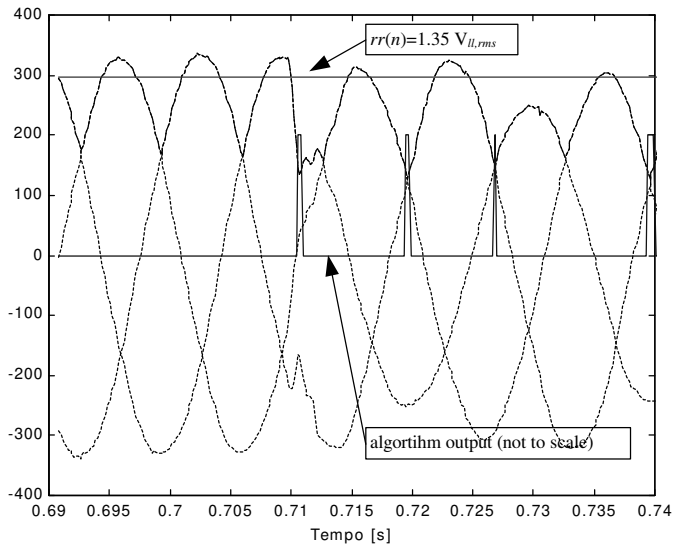


Fig. 7 RV algorithm response for real cases: repetitive sags of short duration

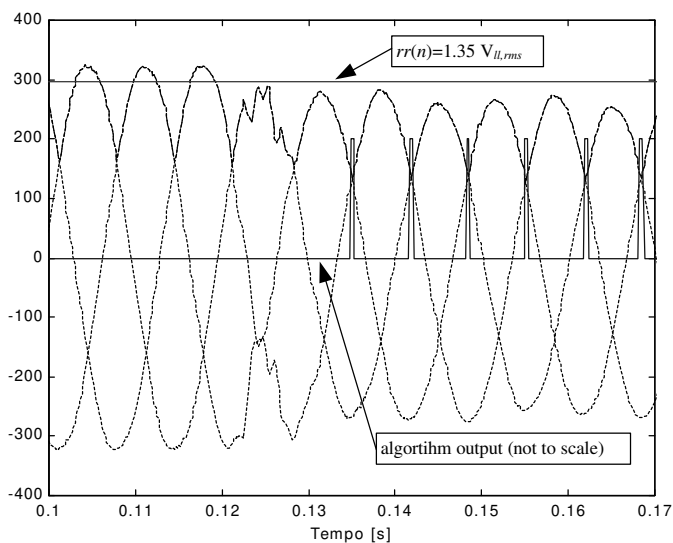


Fig. 8 RV algorithm response for real cases: 85% sag of long duration

The RV algorithm detects the multiple voltage sags after less than 550  $\mu$ s.

### C. Test with real waveforms

The RV algorithm was implemented on a DSP board and tested in the laboratory on the prototype of the Compensation Electronic System (composed of a Voltage Source Inverter and all other apparatus for voltage regulation, system protection and control) of a Superconductive Magnetic Energy Storage system.

Again, for these tests the reference signal  $rr(n)$  was held constant as indicated by (1).

The voltage sags were caused either by switching on and off low value resistors on the supply network (test 1), causing a

network overload, or opening the main circuit breaker (test 2). The performed tests cover voltage sags produced by both single phase and three phase faults. Investigated faults are obtained only with resistive ballast, without considering inductance and capacitance on the network, other than parasitic elements. No voltage swell and its influence on algorithm performance was investigated.

The results are shown in Fig. 9 and Fig. 10. Two line-to-line voltages are shown and the third (lower) trace is the algorithm response.

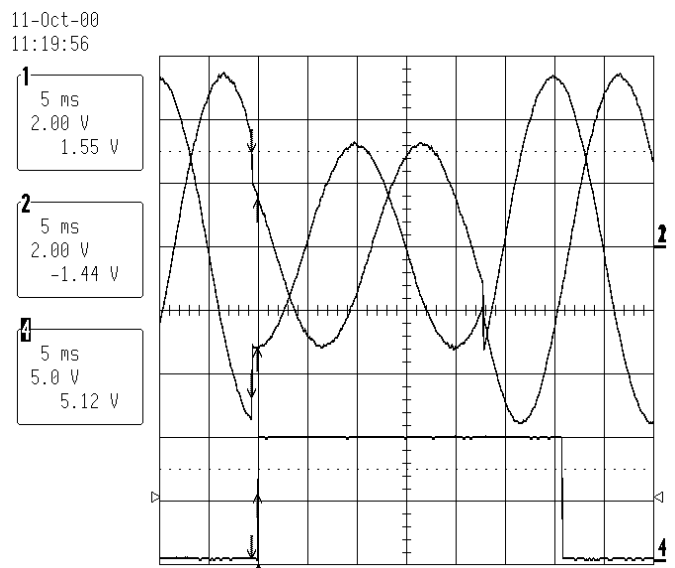


Fig. 9 Response of the RV algorithm for lab test 1

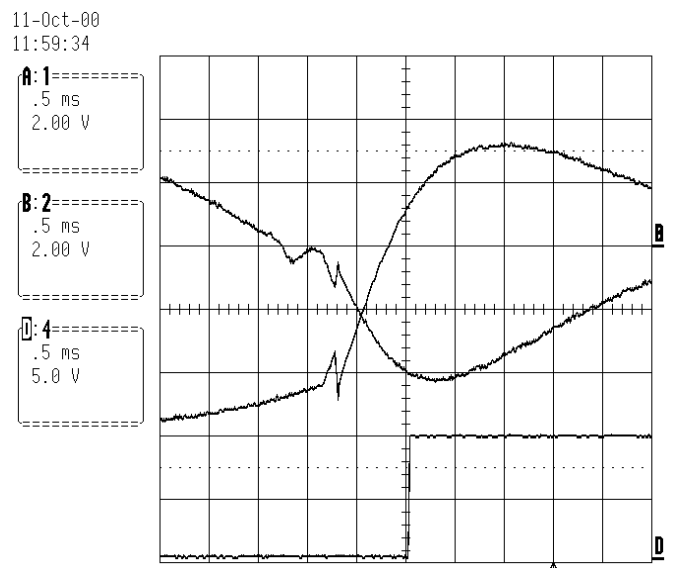


Fig. 10 Response of the RV algorithm for lab test 2

The delay values for sag detection may be estimated equal to 0.6 ms and 0.8 ms for Fig. 9 and Fig. 10 respectively.

Tests like those shown in Fig. 9 and Fig. 10 have been repeated for days, switching the Compensation Electronic System on and off from the protected load, with detection times generally less than 1 ms and only in a few cases (about 5% of tests) between 1 ms and 1.5 ms.

## V. CONCLUSIONS

The proposed algorithm has shown to be efficient in voltage sag detection (the time to sag detection is below 1 ms for most of the tests) and the computational effort (that is the algorithm complexity in terms of number of operations and memory storage requirements) is reduced to a minimum.

This algorithm is presently implemented on a Texas Instruments TMS320C40 board, where the inverter modulator code, the control and automation software and the monitoring program are running in parallel. The power system is the prototype of the Compensation Electronic System, supplied by a Superconductive Magnetic Energy Storage (SMES) device. The complete system will undertake extensive field tests starting on autumn 2003.

## VI. ACKNOWLEDGEMENTS

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## VII. REFERENCES

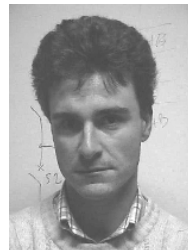
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## BIOGRAPHIES



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**Andrea Mariscotti** was born in Genova, Italy in 1968, he received the degree in Electronics Engineering in 1991 (cum laude) and the Ph.D. in Electrical Engineering in 1997; he was involved in post-Ph.D. activities at the University of Genova on 1998/2000 and he is now a Research Fellow, working in national and international research programs. His main research interests are (internal and external) electromagnetic compatibility, applied to electric drives and transport systems, and modeling and measurement of the electromagnetic interference in power systems. He is Member of the IEEE Instrumentation and Measurement Society. He is a registered professional engineer in the province of Genova.



**Maurizio Mazzucchelli** graduated cum laude in Electrical Engineering from the University of Genova. Since July 1987 he has been Associated Professor of Electrical Machinery at the University of Genova, teaching Electrical Drives for Traction Systems in undergraduate courses in Mechanical Engineering and Electronic Power Systems in undergraduate courses in Electrical Engineering. Prof. Mazzucchelli's technical and scientific activities are mainly concerned with Electronic Power Systems and Drives, with an emphasis on Traction Drives. He is the author of about 70 papers presented at international conferences or published in international journals. Since January '96 until '02 he has been the director of the Transport Research Center of the University of Genova. At present, he is director of the Electrical Engineering Dept. of the Genova University.