Voltage to Frequency Converter for DAC Test

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ABSTRACT

In this paper a modified relaxation oscillator is proposed as the core of an analog to digital modulator for on chip signal extraction for test. The architecture uses digital current source generation and digital switching in place of active circuitry. The resulting design allows for high input sensitivity, robustness to component variation while occupying little silicon area. This paper provides solutions on the main challenges in implementing this modulator and how it may be integrated with a digital based tester.

Keywords: Mixed signal testing, data converters, oscillators.

1. INTRODUCTION

The development of CMOS and BiCMOS technologies has made it possible to combine digital and analog circuits on the one chip increasing system functionality and integration. While the test challenges relating to digital circuits has been addressed through the availability of CAD tools and structured test strategies, the mixed signal test is still function based and therefore complex. The challenges and limitations facing mixed signal analog function based test are, increased resolution, increased bandwidth, higher direct conversion rates and lower permitted noise floor (Figure 1) [1]. It is obvious that present ATE will not be able to accurately measure these devices and that new more expensive ATE will have to be developed, see shaded areas of Figure 1 for more information. This is driving up the cost of analog and mixed signal test.

Verifying the performance of critical analog or mixed signal components on a larger, primarily digital, device is very challenging. While the majority of the device can be tested on a standard digital tester, the analog or mixed signal component will require special analog I/O with large dynamic range and low noise tolerance. While many testers have some analog I/O included, their presence generally has a large cost implication in the overall system. From another perspective, the same problem restricts the use of built in self test(BIST) techniques. In cases where the BIST technique is larger in area or more complex in design than the analog circuitry being tested. This commonly makes BIST economically non-viable.

This paper proposes to insert into a DAC, a modified modulator that will convert the high-resolution analog output signal to a stream of digital pulses, the frequency of which is inversely proportional to the voltage being measured. This digital output will be robust to noise and interference and easy to receive by a digital tester with a high frequency timing reference. For the on-board modulator, a simplified relaxation oscillator will be used to perform the analog voltage to frequency conversion. This overcomes the issue of size in most BIST and embedded ADC applications. The architecture of the modified modulator and the results to date will be presented in the coming sections.

Year of First Product Shipment Technology Generation	2006 100nm	2009 70nm	2012 50nm
Low Frequency Source & Digitiser			
BW (MHz) *	4	4	4
Fs (MS/s) **	10	10	10
Bits	20-23	20-23	20-23
Noise Floor (dB/RT Hz)	-160	-160	-160
High Frequency Waveform Digitizer			
Level V (pk-pk)	4	4	4
BW (MHz) (undersampled)	2000	3000	3000
Fs (MS/s)	1/40/320	1/40/640	1/40/1280
Bits (AWG/Sine)	18/14/12	18/14/12	20/16/12
Noise Floor (dB/RT Hz)	-120	-120	-120

Figure 1: Future test
measurement requirements

2. RELAXATION OSCILLATORS

Relaxation oscillators have been used for many years in applications such as, clock or timing recovery circuits and as part of phase locked loop(PLL) circuits. Relaxation oscillators are astable vibrators, switching between states. Early bipolar transistor implementations utilized the familiar multivibrator architecture [1]. More recent implementations using MOSFET devices typically utilize a Schmitt-trigger based architecture with a grounded timing capacitor. Prominent papers on these oscillators have been written by Gilbert [2], Banu [3] and Abidi and Meyer [4].

The remainder of this section will discuss the operation and performance of the constant current relaxation oscillator using two comparators [5]. The circuit is shown below in Figure 2.

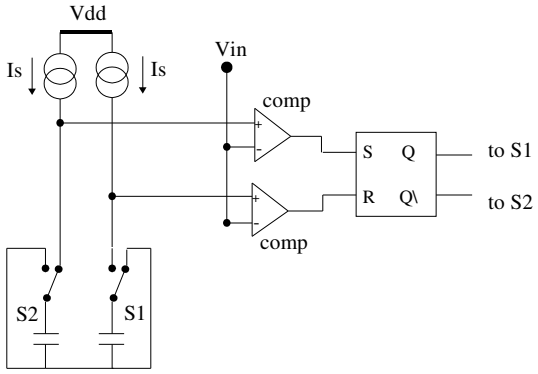

Figure 2: Constant current relaxation oscillator(voltage controlled)

As can be seen the capacitors are either connected to the charging constant current, or are shorted to ground. The capacitor is charged linearly by the constant current sources, the output of the capacitor is connected to a comparator where this voltage is compared with Vin. When the capacitor voltage exceeds Vin, the SR flipflop is triggered which results in the output and the switches, S1 and S2, changing state. This alternates the charging and discharging of the capacitors, Figure 3 shows some ideal waveforms.
Typically these oscillators use varying currents with a fixed voltage reference(as Vin). This results in a frequency to current relationship which is ideally linear, these are called current controlled oscillators. In voltage controlled oscillators, the current source is constant and the input voltage is varied. This results in a time(output period) to voltage relationship that is ideally linear.

The voltage on a capacitor is given by,

$$V = \frac{1}{C} \cdot \int_0^t i_s \cdot dt \tag{1}$$

integrating the right hand side and since i_s is constant,

$$V = \frac{I_s \cdot T}{C} \tag{2}$$

The output time period T is given by

$$T = \frac{2 \cdot V \cdot C}{I_s} \tag{3}$$

where V is V_{in}.

And the corresponding frequency as

$$f_{osc} = \frac{1}{T} = \frac{I_s}{2 \cdot Vin \cdot C} \tag{4}$$

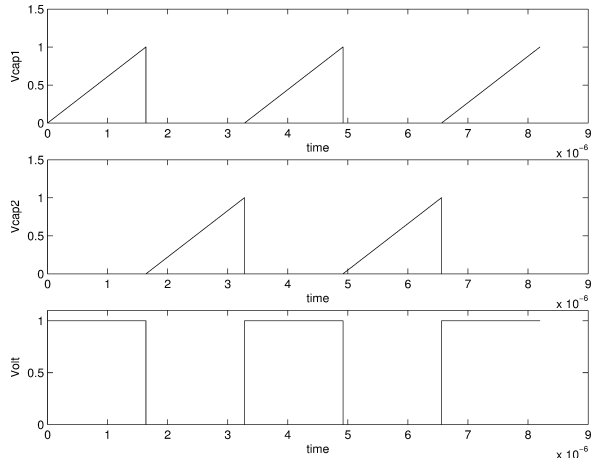

Figure 3: Capacitor voltage waveforms and flipflop output.

The most significant deviation from this linear relationship is the time it takes the comparator to make a decision, the flipflop and the switches to change state. This delay period T_D, sets a minimum value on the oscillation period, resulting in a maximum frequency limit ($1/2T_D$). For the current controlled oscillator, the deviation from the ideal is indicated in Figure 4. For the voltage controlled oscillator, the deviation from the ideal is indicated in Figure 5.

In the voltage controlled case, the relationship remains linear apart from an offset which can be calibrated out. Fortunately the development of faster processes has enabled T_D to be reduced to parts of a nanosecond. The next section discusses the modified oscillator, which is a voltage controlled oscillator.

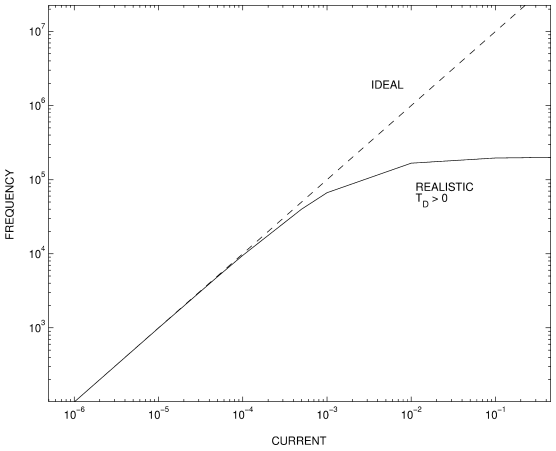

Figure 4: Current controlled Osc.

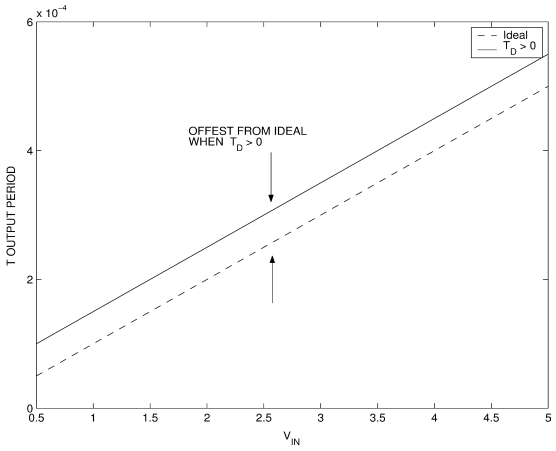

Figure 5: Voltage controlled Osc.

3. MODIFIED OSCILLATOR

For test purposes, it is important that the size of the embedded modulator be kept to a minimum. Most relaxation oscillators have been designed to produce a predictable frequency output with minimal jitter. Size is not a typical constraint. For test purposes the design constraints on the embedded oscillator are to minimize area, achieve a linear relationship between output time period and input voltage, while also minimizing jitter. To achieve this, we propose some modifications to the standard architecture. First the use of a single comparator and the retention of two grounded capacitors, and second the removal of the current source biasing structure.

A circuit diagram of the proposed system is shown below in Figure 6.

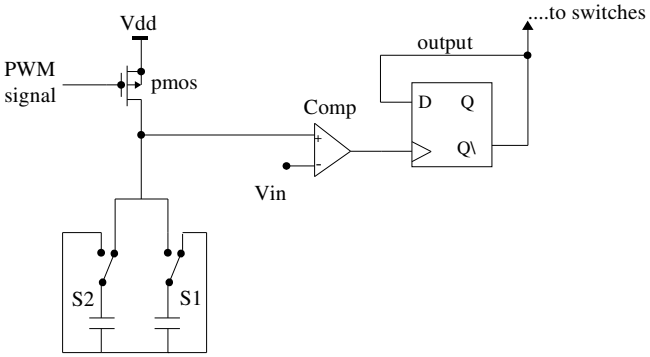

Figure 6: Circuit diagram for proposed minimal sized oscillator.

3.1 Two Capacitors and a Single Comparator

The standard relaxation oscillator CMOS designs utilized a single capacitor with two current sources in series. Depending on the state of the switches, the current sources would act as a source or sink for the charge on the capacitor. Two comparators are then used to set the upper and lower threshold levels. The approach requires two non zero voltage references and is prone to overshoot on the charge or discharge cycle, due to the time delay from crossing the comparator thresholds to changing the state of the switches.

Flynn [5] used two comparators to check the voltage on each capacitor using a single reference. A single voltage input is available in our application. With appropriate switching a single comparator can be used to check the voltage on each capacitor on alternative cycles. Instead of using an SR latch a D-Type flipflop will be used. Each comparator decision

will clock the flipflop whose output will then alternate the switch states. This avoids the need for a second comparator and additional voltage references.

The resolution and precision of the system, is controlled by the deadband or decision sensitivity of the comparator. Thus the design of the comparator must be equal to or greater than the desired conversion resolution. For a 16bit system, this corresponds to tens of microvolts resolution. This is achievable with existing designs [6]. The design of the comparator is simplified as it operates at the oscillation frequency, which can be low, with a high slew rate to minimize T_D.

3.2 Digital Current Source Control

In most relaxation oscillators the current source is provided through a current mirror driven from either a bandgap reference or from some form of input driven g_m cell. For an embedded modulator for test purposes, including a bandgap reference would increase the area overhead substantially. We purpose to use a single PMOS transistor driven via a pulse-width modulated(PWM) voltage signal, as a current source.

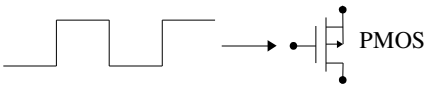

Figure 7: PWM driven PMOS

When the gate voltage is high no current flows through the PMOS, and when its low, the drain current can be approximated by the saturated MOSFET equation,

$$I_D = \frac{\beta'}{2} \cdot \frac{W}{L} (V_{GS} - V_T)^2 \qquad (5)$$

assuming no channel length modulation.

If the PWM switching frequency is high, and the drain current is appropriately low pass filtered, the effective output time period or frequency of the modulator will correspond to the mean of the current from the PMOS. The first point of filtering is through the PMOS itself through the parasitic capacitances at the gate. In saturation, and with low g_m, c_{gs} will dominate, and act as a low pass filter on the input to the PMOS. This is unlikely to be a strong filtering effect as this capacitance is quite small. Much stronger filtering occurs in the charging capacitors. These are in effect integrators with time constants approximate to their oscillation frequency. Finally to calculate the output time period, the tester will take multiple samples over a period of time and then calculate the average time period, effectively integrating the output and providing the final point of filtering.

There are two main areas of difficulty in implementing this approach. First the single PMOS current source needs to have a very large small signal output impedance in order to act as a linear current source with varying drain voltage. With modern devices and increased short-channel effects, this will be very difficult to achieve using a single PMOS. A cascoded current source could be used. Secondly a digitally driven gate input would be prone to power supply noise which would modulate the current supplied to the capacitor. This noise will also be filtered but may be troublesome in sensitive applications where the current source and capacitor values are sufficiently small.

3.3 Jitter Analysis

Jitter is defined as random fluctuations in the output period of the waveform, caused by noise produced by the active and passive components of the oscillator circuit. Abidi and Meyer [4] described jitter by the expression,

$$\text{jitter} = \frac{\sigma_T}{\mu_T} \qquad (6)$$

where σ_T and μ_T are the standard deviation and mean respectively, of the oscillation pulsewidth. To calculate the jitter, the total circuit noise is referred to a single equivalent voltage noise source V_n, in series with the capacitor voltage and at the input to the comparator. Abidi and Meyer showed that the variation in period σ_T (jitter), can be calculated as

$$\sigma_t = \frac{\alpha \cdot \sqrt{6} \cdot V_n(\text{rms})}{S} \tag{7}$$

where S is the slope of the capacitor voltage waveform, α is a constant valued between 0.5 and 1, depending on the bandwidth of the noise [4]. Thus to minimize jitter we can increase the slope of the capacitor voltage waveform, reduce the bandwidth of the noise by filtering or minimize the noise by design.

The total referred circuit noise at the input of the comparator, as stated above, excludes the noise due to current noise through the capacitor caused by the current source and also excludes capacitor noise (kT/C). These noise sources are much smaller than other noise contributers in the circuit [4]. Thus for the circuit in Figure 6 we need only examine the noise contributions of the devices in the comparator circuit.

4. MEASUREMENT AND CALIBRATION

Measurement of the period of the output waveform can be performed by two external edge counters driven by an external reference clock. This will enable accurate measurements of signal periods if taken over a sufficiently large period of time.

$$\frac{T_{\text{period}}(\text{ref clock})}{T_{\text{period}}(\text{signal})} = \frac{N_{\text{edges}}(\text{signal})}{N_{\text{edges}}(\text{ref clock})} \tag{8}$$

Since this process is an integration operation, increased measurement time will also reduce the effect of cycle to cycle jitter on the final accuracy.

The increase in oscillation period is monotonic with increases in input voltage, but the scalar relationship is unclear, due to process variations in capacitor and current source values. Thus it is important to calibrate the linear relationship of input voltage to oscillation period, through measurement of some known points. If a reference voltage can be applied that is available elsewhere on the chip or externally, it and fractions of it could be used. Also if a zero input is used, the system can be designed so that it will oscillate at the minimum period of the system, defined by T_D. Where the modulator is interfaced with a tester, a preliminary set of measurements would identify the scaling factors, which than can be used in later measurements.

5. RESULTS

To explore the performance of the system, a MATLAB simulation was created for a 16bit modulator. That assumed transistor level performance as described by (5) but with channel length modulation included giving,

$$I_D = \frac{\beta'}{2} \cdot \frac{W}{L} (V_{GS} - V_T)^2 \cdot (1 + \lambda (V_{DD} - V_{CAP})) \tag{9}$$

An ideal saturation current of 1.6uA was used with a capacitor value of 50pF. A switching time delay of 3nS was assumed, which is conservative given modern logic. Simulations have shown that large switching time delays(T_D) have little effect on performance, Figure 5. From (3) the output time period increases by approximatley 9.5nS for an input voltage increase of 1 LSB, based on a 50/50 mark-space ratio modulated current source and a 1mS measurement time. For a tester with a reference clock period of 1nS this gives a minimum difference resolution of 3bits.

From (3) the expected relationship between the input voltage and the output period is linear, as shown in Figure 8. the corresponding inversely proportional relationship with frequency is shown in Figure 9. The exact slope of the line, shown in Figure 8, is given by the ratio of charging current and capacitance. In a real application, calibration of this slope would be required to cater for the variability in capacitance and current values. This could then be used to control the mark space ratio of the digital signal to the current source, adjusting the slope of the line. Alternatively it could be used off chip for mathematical correction.

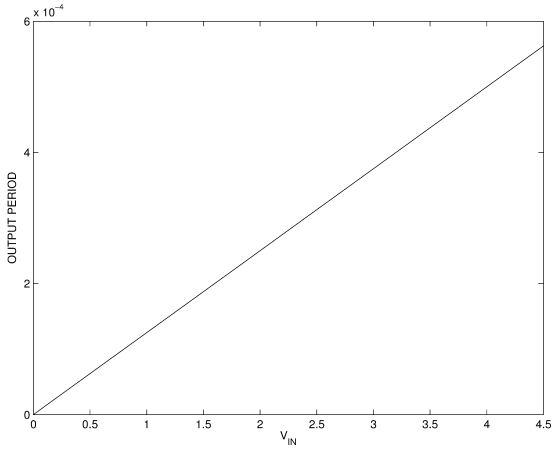

Figure 8: Output period vs input voltage

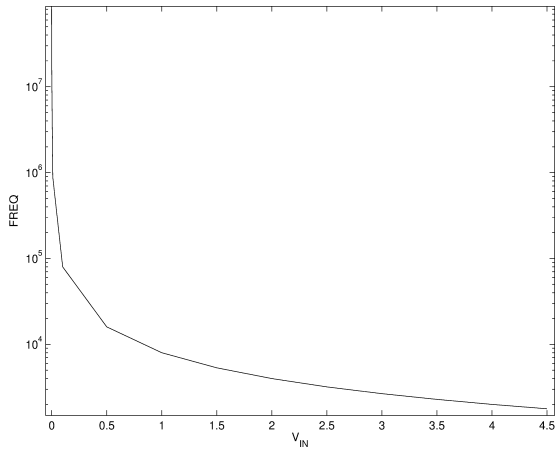

Figure 9: Output freq. vs input voltage

The use of a digitally modulated current source has significant advantages in terms of controllability and size. However through both gate drain capacitance and direct modulation of the current source, a route exists for signal feedthrough to the output. In the following Figure 10, the output noise from an oscillator with a digitally modulated current source was compared with that from a constant current source. Figure 10 shows that as the modulation frequency decreases the noise contribution increases, though it remains low. A method to further reduce the effect of clock feedthrough via gate drain capacitance is shown in Figure 11. An NMOS transistor is placed in parallel to the PMOS, and is driven by the inverted PWM signal. The NMOS is half the size of the PMOS, assuming that the mobility of the NMOS is twice that of the PMOS.

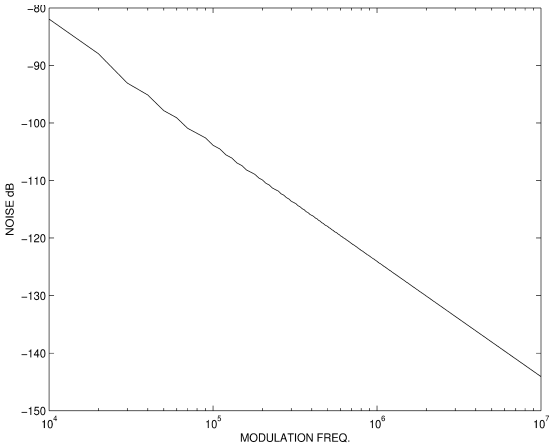

Figure 10: RMS difference in I_{mirror} & PWM current source

A more serious issue is that of channel length modulation, λ. The effect of λ is to change the current source from delivering a constant current, when ON, to one whose current changes value depending on the voltage on the capacitor

V_{CAP}. In Figure 12 below, the period to input voltage relationships are shown for a number of devices with varying channel length modulation. The design of the current sources will need to focus on reducing λ, or equivalently increase the small signal output resistance, r_{ds}, through cascading or longer devices.

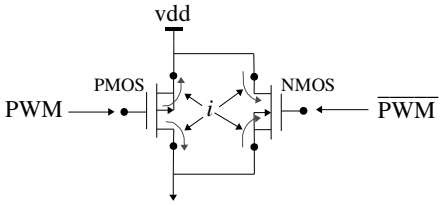

Figure 11: NMOS reduces signal feed-through significantly

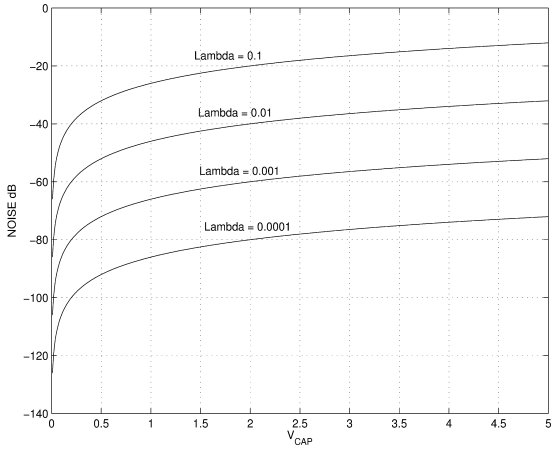

Figure 12: Effects of channel modulation on linearity

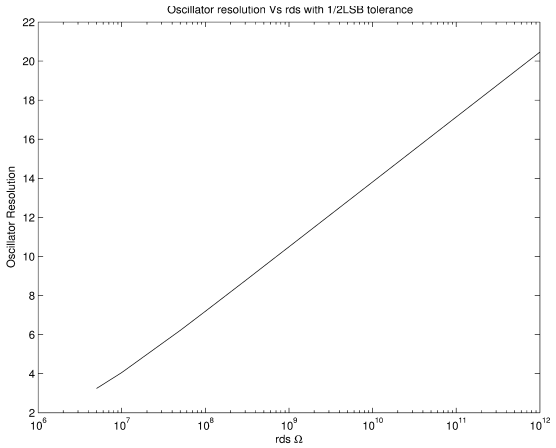

Figure 13: Modulator Resolution vs r_{ds} values

Figure 13 shows the relationship between modulator resolution and r_{ds}. As can be seen to achieve a resolution of 16bits with a non-linearity tolerance of 1/2LSB would require an r_{ds} value of approximately 40GΩ, which is unachievable. Figure 14 shows how the difference in output period from the ideal, for various values of r_{ds}. This means that the output period will be non-linear to the input voltage as described by (3) and therefore will need to be calibrated in order to correct the effects of channel length modulation.

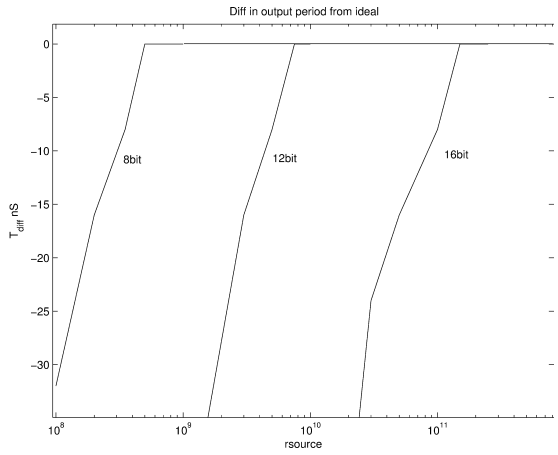

Figure 14: Difference in output period for various modulator resolutions

There is a way to eliminate the effect of channel length modulation, it is shown below in Figure 15. The drain of the PMOS is now held at virtual ground, thus the current source is linear. The disadvantage of this solution is the capacitor voltage now ramps negatively, therefore it needs to be inverted before being compared with V_{IN}. The operational amplifier and inverting amplifier will add a voltage offset to Vcap as well as voltage noise. The addition of these extra two circuit blocks also increases the silicon area.

A better solution is to use a switched capacitor integrator circuit as shown in Figure 16. It is a non-inverting and parasitic insensitive circuit. C_R is charged during ϕ_1 while the voltage across C is held, during ϕ_2 the charge in C_R is injected into C, the voltage across C is defined as

$$V_o(z) = V_i(z) \cdot \left(\frac{C_R}{C}\right) \cdot \frac{z^{-1}}{(1 - z^{-1})} \qquad (10)$$

while PWM is low, when PWM is high, V_o is held. And where,

$$V_i = \frac{I_D \cdot T_\Phi}{C_R} \qquad (11)$$

Therefore the output voltage will step up by $V_i(C_R/C)$ every ϕ_2 clock cycle.

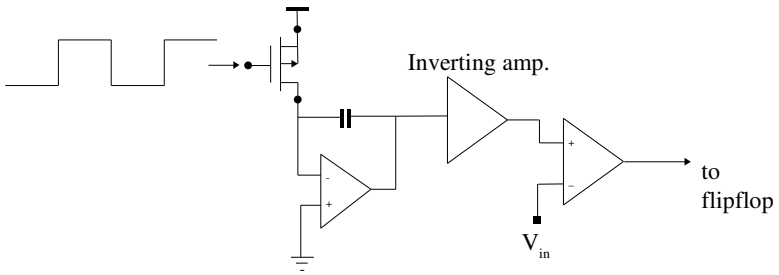

Figure 15: Method to overcome effect of channel length modulation

Although the drain voltage of the PMOS in Figure 16 still varies from 0 to V_{1LSB}, this is sufficiently small enough to ignore channel length modulation effects. The system requires two non-overlapping clocks, ϕ_1 and ϕ_2, these could be generated from a clock already on chip or externally from the tester. The operational amplifier will add a voltage offset to the output voltage and noise. The system also requires a monostable multi-vibrator instead of a flipflop to reset C once the comparator threshold has being crossed.

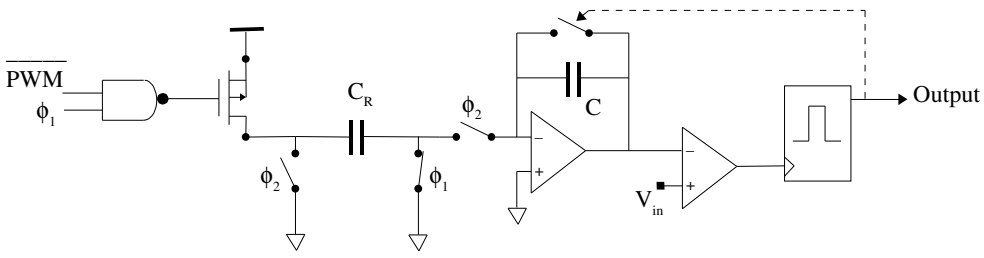

Figure 16: Switched capacitor ramp

The problem of a nonlinear voltage ramp has not gone away though, finite amplifier gain will cause the switched capacitor ramp to be nonlinear. Finite gain influences not only the value of the input, on $C_{R,}$ but also the value stored on the integrating capacitor C. V_{out} of the integrator is described as,

$$V_o = ((\frac{C_R}{C}) \cdot V_i + V_{stored}) \cdot \frac{A}{(A+1)} \quad (12)$$

where A is the open loop gain of the amplifier and V_{stored} is V_o of the previous step.

The effect of the finite gain is to continually reduce the contribution from the previous steps(N) as follows,

$$V_o(N) = \sum_{i=1}^{N} i \cdot V_i \cdot [\frac{A}{(1+A)}]^{N-i} \quad (13)$$

This will lead to a nonlinear voltage ramp as shown below.

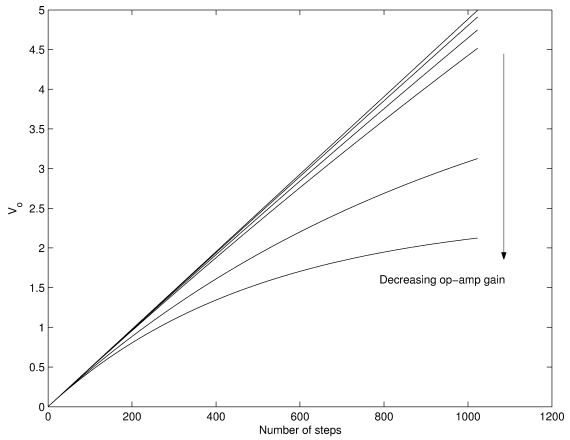

Figure 17: Nonlinearity due to finite op-amp gain.

The problem is related to the number of steps in the staircase not the size of the step itself. From simulations, to keep the overall INL error to be less than a quarter of an LSB, will require the following minimum gain for the integrator amplifier,

Resolution(bits)	Min Gain(dB)
8	102
12	150
16	198

Table 1: Min op-amp gain for 1/4LSB INL tolerance

Despite the low frequency of operation, for high performance exceptionally high gain values are needed, but which are typically unobtainable. This problem can be partially solved through the use of finite-gain insensitive integrators [7-9]. It is envisaged that these types of integrators will be used in the ramp generators as part of a pipeline architecture, where two relaxation oscillators will be connected in series, they will each have 8 bits of resolution. The architecture is shown in Figure 18.

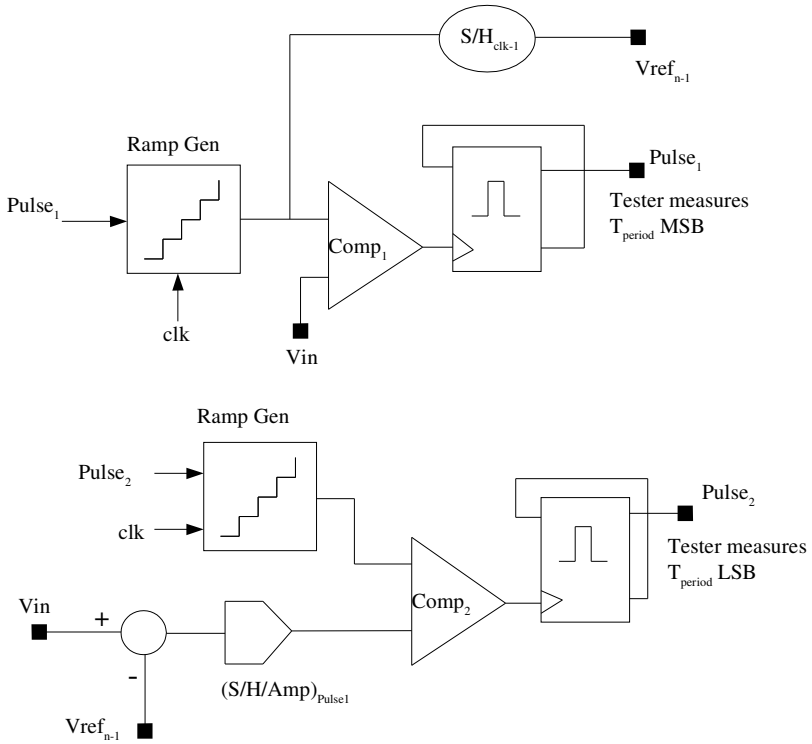

Figure 18: Pipeline relaxation oscillator ADC

6. CONCLUSIONS & FUTURE WORK

The purposed architecture meets the requirement of high sensitivity and performance with low die area. The architecture trades sampling speed for performance in a linear manner. Current trends in process technologies and device speeds will enhance its performance, allowing for either faster sampling or increased resolution. It is robust to process variations and has an inherent method for calibration and self test. Work is ongoing to develop a prototype of the modulator Figure 18, the purposed architecture has the potential for achieving high resolution with a very small die footprint.

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