VULNERABILITY ASSESSMENT OF LINE CURRENT DIFFERENTIAL PROTECTION IN CONVERTER-DOMINATED POWER SYSTEMS

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Abstract

Line current differential (LCD) protection is traditionally considered to be highly dependable and secure. However, the increasing penetration of converter interfaced sources (CIS) (e.g. wind, PV, HVDC systems, etc.) could significantly reduce the system fault level and change the fault characteristics, thus presenting challenges to the reliable operation of LCD protection. In this paper, the impact of the integration of CIS on LCD performance is investigated comprehensively. Analytical expressions representing LCD relay operation in the presence of converter-driven fault currents and weak infeed conditions have been developed. A test network, comprising of a CIS model equipped with a typical converter fault-ride through strategy that is compliant with the GB Grid Code, has been built in a Real-Time Digital Simulator (RTDS). Simulations of LCD performance for different fault and system conditions are performed and presented. It is demonstrated that the dependability of the LCD relay can be compromised during internal phase-to-phase faults. The results also show that with the synchronous generation being displaced by CIS, the increasing CIS penetration and fault contribution from the CIS can lead to an increased phase angle difference between the fault currents contributed from the two ends of the protected line, which will increase the risk of the compromised protection performance.

1 Introduction

Power system operators in many countries are striving to accelerate the decarbonisation agenda to achieve the net-zero emission target, while ensuring the secure and reliable delivery of electricity. As a result, increasing volumes of converter interfaced sources (CIS, e.g. wind, PV, HVDC systems, etc.) are being integrated to the power networks to displace fossil fuel-driven Synchronous Generators (SGs)[1], which leads to a massive decrease of system fault levels [2]. The fault characteristics of CIS are determined by the associated grid code requirements, proprietary converter controller strategies and converter ratings. The different and variable nature of the fault characteristics in power systems with a high penetration level of CIS can introduce significant challenges to the operation of traditional protection systems.

Line differential current protection has been widely used as an important primary protection method for transmission lines, which provides highly dependable and secure protection for different adverse situations in conventional systems dominated by SGs [3]. Various studies have found that the integration of CIS could severely compromise the performance of distance protection [4–6] and directional overcurrent schemes [7], highlighting the increasing importance and reliance on the LCD protection performance. However, the limited fault current contribution capability of CIS and the controller dependent fault characteristics have also led to an increasing concern of the risk of comprised performance of LCD protection in future power networks.

Investigations of LCD protection in the presence of CIS have been presented in [8–11]. In [8, 9], characteristics of the converter fault current using a dual sequence current controller with different control objectives are analysed, which demonstrate that fault conditions and control objectives could both influence the fault current angles. It was shown that, for a transmission line connecting a CIS with the grid, the angular difference between the CIS and the grid currents for the faulted phase can increase significantly for internal phase-to-phase faults, thus presenting risk of protection failure. However, the influence of various factors (e.g. CIS ratings, system fault levels) on the LCD performance have not been analysed. [10] and [11] present mathematical expressions for representing fault contributions from the CIS and the grid into an LCD operating characteristic, under the assumption of a relatively strong grid-side fault contribution. In [10], the mathematical expression for the CIS current references under different control strategies are derived, while in [11] the controlled nature of CIS fault waveforms are represented as a voltage dependent current source in parallel with a variable impedance. It was demonstrated that the line length, CIS capacity, fault location and fault severity could all influence the performance of the LCD protection. Available literature has highlighted that decreased sensitivity or possible protection failure of LCD in the presence of CIS is possible. However, determining which factors or combination of factors are more likely to impact LCD protection is difficult to achieve from a purely analytical approach. Existing simulation case studies have also only focused on investigating individual factors or have been limited to a few extreme conditions. An assessment of LCD performance, in the presence of fundamentally different CIS fault characteristics and low fault level conditions, is therefore urgently needed to ensure the comprehensive understanding of the risk of LCD protection failure, thus enabling continued deployment of CIS.

This paper investigates and demonstrates the impact of reduced system fault levels and CIS fault characteristics on the LCD performance. Analytical expressions representing the LCD operation in the presence of CIS conditions are developed to identify factors that may impact its performance. A test network, comprising of a CIS model with typically adopted converter control strategies, is established in a Real-Time Digital Simulation (RTDS) platform for simulating different fault scenarios that could potentially affect the LCD performance. The identified scenarios that negatively impact LCD performance combined with knowledge of present and predicted power system conditions will allow operators to determine the risk of compromised LCD performance as well as the timescale in which it may occur.

The rest of the paper is structured as follows: Section 2 presents the analysis of LCD protection in the presence of CIS; details of the simulation model used as well as case studies showing the influence of various factors on LCD performance are presented and discussed in Section 3; and finally, Section 4 presents the conclusions and possible future research activities based on the outcomes of this work.

2. Analysis of Line Current Differential Protection in the Presence of CIS

Fig. 1(a) shows a schematic representation of an LCD protection scheme in the presence of varying CIS penetration and system fault level. Considering a scenario where the fault contribution at Bus M is supplied completely by the CIS (i.e., CIS M) and the fault contribution at Bus N supplied by the grid is mainly from synchronous generation represented as a voltage source (i.e. SG N) with an equivalent internal impedance. The current measurements from the protected line used by the LCD to calculate the differential and restraining currents (I_d and I_r respectively) can be represented as in (1) and (2) [12]:

$$I_d = |I_M^f + I_N^f| \tag{1}$$

$$I_r = K|I_M^f - I_N^f| \tag{2}$$

The operating condition can therefore be described by:

$$I_d > KI_r \tag{3}$$

where K represents the slope of the restraining characteristic and can typically range from 0.3 to 1.2; I_N^f is the fault current contribution from the grid side (i.e. terminal N); and I_M^f is the fault current contribution from the CIS (i.e. terminal M). I_M^f varies depending on the rating of the converter plant, control scheme including fault ride through (FRT) requirements and fault conditions. This behaviour can be modelled as a voltage-dependent current source with a parallel variable impedance in series with the transformer impedance as illustrated in Fig. 1(b) [13]. Z_{CIS}^f represents the equivalent impedance of the variable converter impedance and the transformer impedance. The grid is modelled as a voltage source, E_G with equivalent impedance, Z_G. Z_L represents the impedance of the protected line MN and x is the distance to the fault location relative to bus M. Applying Kirchhoff's Current Law to the circuit of Fig. 1(b), the fault current can be expressed as:

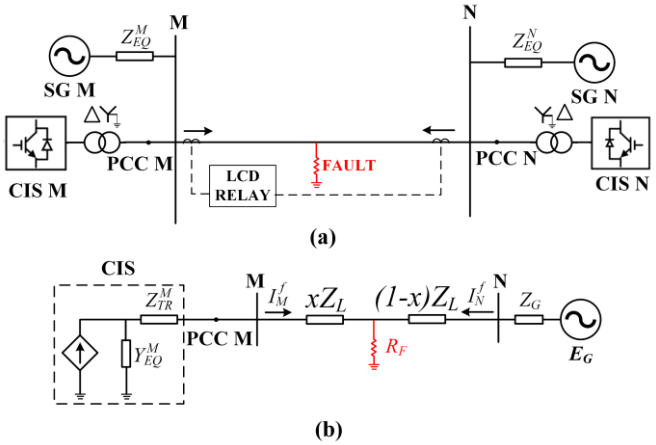

Fig. 1. (a) LCD protection scheme for a transmission line with variable penetration of CIS; (b) Equivalent model representation during faults with the CIS at Bus M connected to the grid at bus N

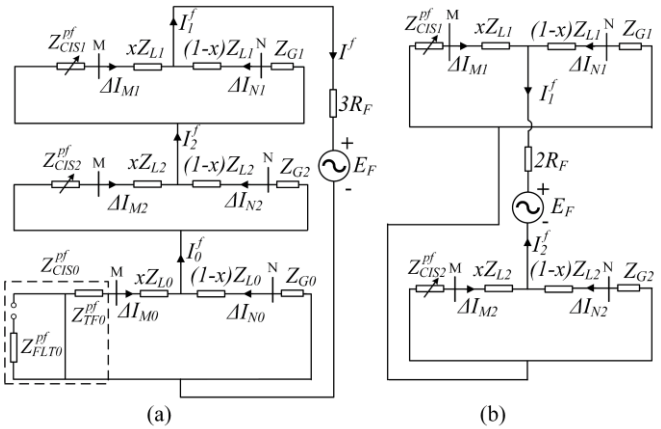

Fig. 2. Sequence networks: (a) AG fault, (b) BC fault.

$$I_f = I_M^f + I_N^f \tag{4}$$

When a fault occurs, the current is changed relative to the pre-fault conditions resulting in incremental current [14] , $\Delta I_{(M,N)}$, at the line terminals:

$$\Delta I_{(M,N)} = I_{(M,N)}^f - I_{(M,N)}^{pre} \tag{5}$$

where, $I_{(M,N)}^{pre}$ is the pre-fault current at bus M and N respectively. By substituting (5) into (4), the faulted loop current can be expressed in terms of incremental current as:

$$I_f = \Delta I_M + \Delta I_N \tag{6}$$

Based on (5) and (6), pure-fault sequence network representations for phase-to-ground (AG) and phase-to-phase (BC) faults are illustrated in Fig. 2(a) and Fig. 2(b) respectively. Z_{CIS}^{pf} represents the pure-fault equivalent impedance of the CIS and transformer; E_F represents the pre-fault voltage at the fault location and the subscripts 1, 2 and 0 represent the positive, negative and zero-sequence respectively. Note that due to the delta-wye-grounded connection of the transformer, there is no zero-sequence current contribution from the CIS. Consider an AG fault occurring at a distance x from bus M along the transmission

line MN. Applying sequence component representation, (1) becomes:

$$I_d^A = \left|(I_{M1}^f + I_{N1}^f) + (I_{M2}^f + I_{N2}^f) + (I_{M0}^f + I_{N0}^f)\right| \quad (7)$$

Using (4) and (6), I_d^A, can be expressed in terms of incremental currents:

$$I_d^A = |(\Delta I_{M1} + \Delta I_{N1}) + (\Delta I_{M2} + \Delta I_{N2}) + (\Delta I_{M0} + \Delta I_{N0})| \quad (8)$$

Incremental sequence currents at bus N can be described using current distribution factors as presented in (9):

$$\Delta I_{N(1,2,0)} = D_{(1,2,0)} \Delta I_{M(1,2,0)} \quad (9)$$

where:

$$D_{(1,2,0)} = \frac{Z_{CIS(1,2,0)}^{pf} + xZ_{L(1,2,0)}}{Z_{G(1,2,0)} + (1-x)Z_{L(1,2,0)}} \quad (10)$$

Applying the distribution factors to (8) and noting that for an AG fault that $I_1^f = I_2^f = I_0^f$, the differential current for an AG fault can be expressed as:

$$I_d^A = |3\Delta I_{MA1}(1 + D_1)| \quad (11)$$

Similarly, restraint current in (2) can be represented as

$$I_r^A = \left|(I_{M1}^f - I_{N1}^f) + (I_{M2}^f - I_{N2}^f) + (I_{M0}^f - I_{N0}^f)\right| \quad (12)$$

$(I_{M1}^f - I_{N1}^f)$ in (12) can be expressed in terms of incremental and pre-fault current as in (13):

$$(I_{M1}^f - I_{N1}^f) = \sqrt{(1+D_1)^2 \Delta I_{M1}^2 - (I_{M1}^{pre} + \Delta I_{M1})(-I_{M1}^{pre} + D_1 \Delta I_{M1})} \quad (13)$$

(13) is simplified in (14).

$$\left(I_{M1}^f - I_{N1}^f\right) = 2I_{M1}^{pre} - (D_1 - 1)\Delta I_{M1} \quad (14)$$

Similarly, the negative and zero-sequence terms of (12) can be expressed as:

$$\left(I_{M(2,0)}^f - I_{N(2,0)}^f\right) = \Delta I_{M(2,0)}(1 - D_{2,0}) \quad (15)$$

Substituting (14) and (15) into (12), the restraining current is expressed as:

$$I_r^A = \left|\left(2I_{M1}^{pre} - (D_1 - 1)\Delta I_{MA1}\right) + \Delta I_{MA2}(1 - D_2) + \Delta I_{MA0}(1 - D_0)\right| \quad (16)$$

Using current distribution factors in (10), the relation between faulted path currents for AG fault can be expressed as:

$$\Delta I_{M1}(1 + D_1) = \Delta I_{M2}(1 + D_2) = \Delta I_{M0}(1 + D_0) \quad (17)$$

Thus I_r^A can be expressed as:

$$I_r^A = \left| 2I_{M1}^{pre} + \Delta I_{M1}\left((1 + D_1) + \frac{(1 - D_0)(1 + D_1)}{(1 + D_0)} + \frac{(1 - D_2)(1 + D_1)}{(1 + D_2)} \right) \right| \quad (18)$$

With a similar approach for BC fault, the differential and restraining currents for B and C phase are derived in (19) – (22) using the pure-fault sequence network shown in Fig. 2(b).

$$I_d^B = \left|-j\sqrt{3}\,\Delta I_{M1}(1 + D_1)\right| \quad (19)$$

$$I_r^B = \left|a^2 2I_{M1}^{pre} + \Delta I_{M1}\left(a^2(1 - D_1) - \frac{a(1 + D_1)(1 - D_2)}{(1 + D_2)}\right)\right| \quad (20)$$

$$I_d^C = \left|j\sqrt{3}\,\Delta I_{M1}(1 + D_1)\right| \quad (21)$$

$$I_r^C = \left|a2I_{M1}^{pre} + \Delta I_{M1}\left(a(1 - D_1) - \frac{a^2(1 + D_1)(1 - D_2)}{(1 + D_2)}\right)\right| \quad (22)$$

The analysis demonstrates that the differential and restraining currents used by LCD are functions of distribution factors. The distribution factors consist of equivalent pure-fault impedance of CIS which vary significantly with the fault location, fault resistance, line length, converter control strategy, converter rating and grid fault level influencing fault severity and system condition. Thus, the presence of CIS can have significant impact the performance of LCD relay.

3 Case Studies

3.1 Test System

The 2-bus test network used to assess the LCD performance within the RTDS is illustrated in Fig. 1(a). A Modular Multilevel Converter (MMC)-based HVDC model developed in [15] is used to model the CIS at each bus. This model contains a flexible dual-sequence current controller capable of achieving different fault control objectives and FRT requirements.

Table 1 Test Network Parameters

Parameter	Description	Value
V_N	Base Voltage	400 kV
S_{base}	Base Apparent Power	100 MVA
Z_{L1}	Positive sequence line impedance	0.0292+j0.318 Ω/km
Z_{L0}	Zero sequence line impedance	0.142+ j0.84 Ω /km
C_{L1}	Positive sequence line capacitance	8.9 x 10^{-9} F/km
C_{L0}	Zero sequence line capacitance	6.4 x 10^{-9} F/km
K	Relay bias slope	0.5

In this paper, the fault response of the MMC is set as balanced current injection and the FRT strategy injects reactive current to provide voltage support during fault conditions based on the GB Grid Code [16]. Equivalent voltage sources with series impedances that can be changed to emulate different system fault levels at each bus are also incorporated. This also allows for the simulation of different levels of CIS penetration. Faults are simulated along the protected transmission line MN and the line terminal currents are input to a relay model based on equations (1)-(3). System parameters of the test network are summarised in Table 1.

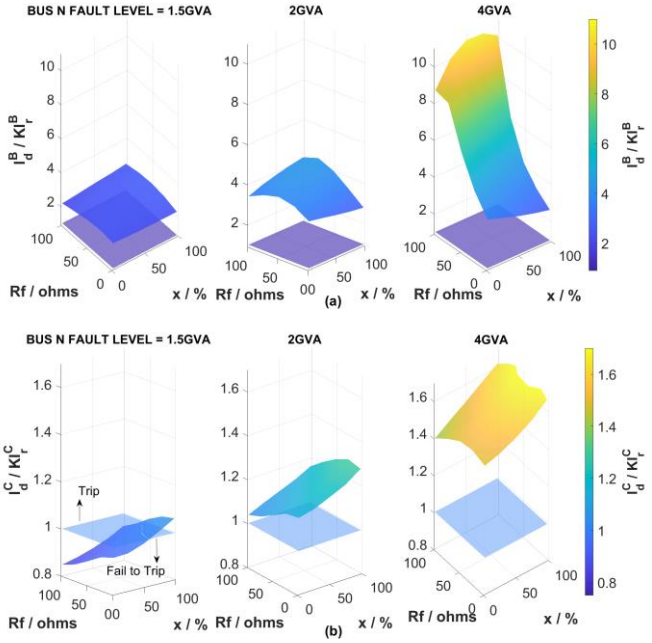

Fig. 3. Impact of system fault level on LCD performance for BC fault: (a) Phase B; (b) Phase C

3.2 Impact of system fault level on LCD performance

The test system is adjusted so that the fault contribution at bus M is completely supplied by the CIS, which is rated at 800 MVA. The line length is set as 100 km. The fault contribution at Bus N is supplied by the grid. The system fault level at Bus N is varied and different fault conditions (fault resistance, locations relative to Bus M) are simulated. The ratio of the differential and restraint current ($I_d/(KI_r)$) is plotted for the different fault and system conditions. As described in (3), a value of 1 for this quantity ($I_d/(KI_r)$) represents the tripping boundary. Values greater than 1 represent proper operation, while values below 1 represent protection failure. The results of this case study are illustrated in Figs. 3 and 4 with the tripping boundary represented as a plane with a value of 1 at the vertical axis.

Fig. 3 illustrates LCD performance for a BC fault, for different fault conditions and fault levels, when the CIS provides the fault contribution at bus M. Fig. 4(a) shows that for phase B, the LCD relay could suffer from decreased sensitivity as the fault infeed from bus N decreases. This trend is observed with a higher impact in the phase C element of the LCD performance as observed in Fig. 4(b), where phase C can fail to detect the fault in some cases (there are areas below the tripping boundary). Such potential failures are expected to occur for high resistance faults located closer to bus M, where the CIS is connected. This may be an urgent issue for utilities that adopt single pole tripping as phase-to-phase faults may be misclassified as a phase-to-earth fault, resulting in a faulted phase not being isolated. Fig. 4 illustrates the LCD performance for an AG fault with different fault conditions and fault levels. It is observed that as the remote end fault infeed decreases, the sensitivity of the LCD relay also decreases. The general trend shows that for low fault level conditions, high

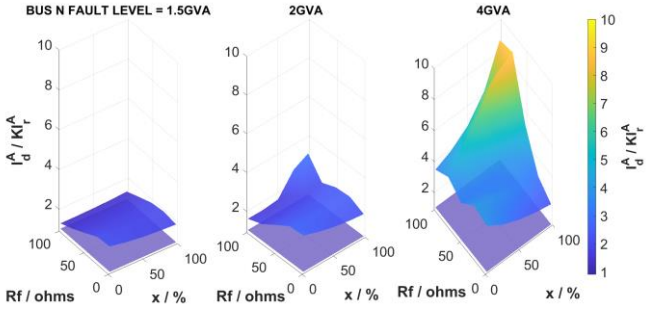

Fig. 4. Impact of system fault level on LCD performance for AG fault

resistance faults closer to the CIS can lead to decreased protection sensitivity.

3.3 Impact of CIS rating on the LCD performance

The test system is adjusted so that the fault contribution at bus M is completely supplied by the CIS. The fault contribution at Bus N is supplied by the grid with an equivalent fault level set as 2 GVA. The line length is set as 100 km. The CIS rating at Bus M is varied and different fault conditions are simulated. The results of this case study are illustrated in Figs. 5 and 6 with the tripping boundary represented as a plane with a value of 1 at the vertical axis.

Fig. 5 illustrates the LCD performance for a BC fault, for different fault conditions and system fault levels. Fig. 5(a) shows that, for a BC fault, the phase B element is expected to operate with decreased sensitivity as the CIS rating increases. This trend is observed with a higher impact in the phase C element in the LCD relay. Fig. 5(b) shows that with higher CIS penetration, phase C relay operates with decreased sensitivity for high-resistance faults closer to the CIS, eventually leading to a failure to detect the fault as the CIS penetration increases. Similar to the finding from the previous study, this may lead to the failure in isolating one of the faulted phases during phase-to-phase faults if single pole tripping is adopted.

Further increase in CIS penetration also leads to an increase in the number of fault locations and resistances where protection failure is observed. Fig. 6 shows that as the CIS rating increases, the sensitivity of the LCD relay for AG faults decreases. The general trend shows that for high penetration of CIS, high resistance faults closer to the CIS lead to decreased sensitivity.

3.4 Impact of transmission line length on LCD performance

The test system is adjusted so that the fault contribution at bus M is completely supplied by the CIS which is rated at 1.2 GVA. The fault contribution at Bus N is supplied by the grid with an equivalent fault level set at 2 GVA. The transmission line length is varied and different fault conditions are simulated. The results of this case study are illustrated in Figs. 7 and 8 with the tripping boundary represented as a plane.

Fig. 7 illustrates LCD performance for a BC fault, for different fault conditions and system strengths, when the CIS provides the fault contribution at bus M. Fig 7(a) shows that, for a BC fault, the B phase operates with decreased sensitivity as the line length increases. This trend is observed with a higher impact in the phase C element of the LCD relay with risks of

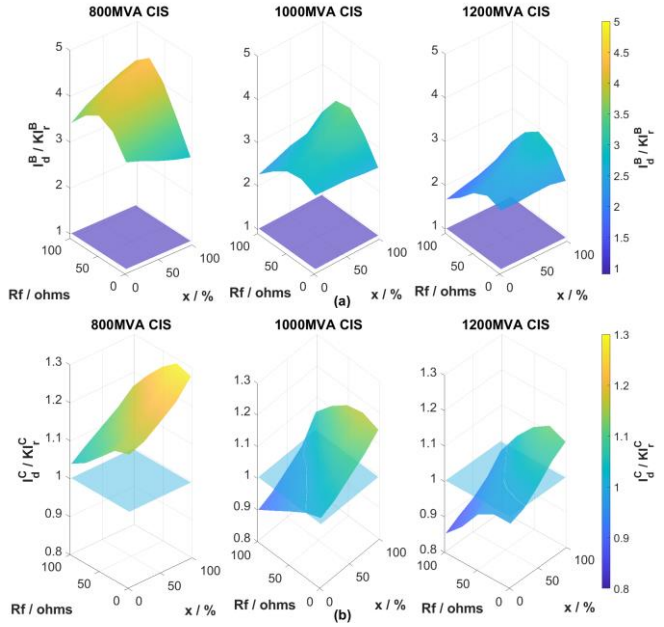

Fig. 5. Impact of CIS Rating on LCD performance for BC fault: (a) Phase B, (b) Phase C

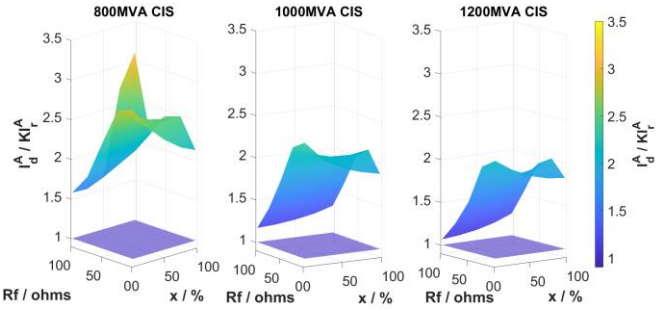

Fig. 6. Impact of CIS rating on LCD performance for AG fault

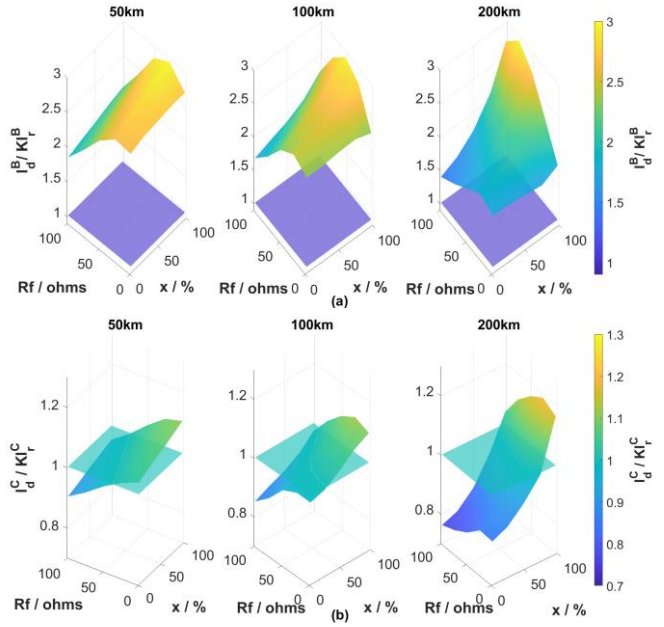

Fig. 7. Impact of line length on LCD performance for BC fault: (a)Phase B, (b) Phase C

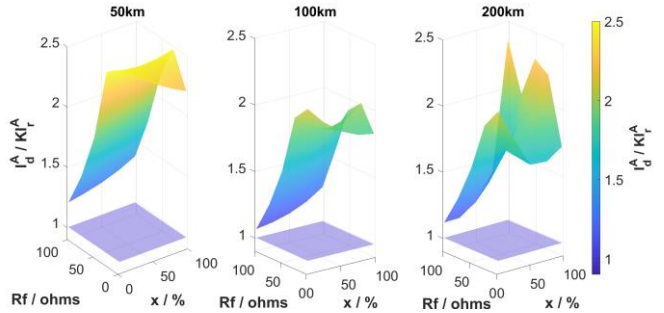

Fig. 8. Impact of line length on LCD performance for AG fault

protection failure observed for all tested line lengths. Fig. 7(b) shows that for shorter line lengths, high fault resistances limit the grid side contribution leading to protection failure. For longer line lengths, faults closer to the CIS bus are prone to protection failure regardless of fault resistance as the line impedance becomes the influential factor. Fig. 8 shows that for all line lengths the sensitivity of the LCD relay decreases for high resistance AG faults closer to the CIS bus.

3.4. LCD relay failure in the presence of CIS

Fig. 9(a) illustrates the current waveforms at the two ends of the protected line for the C phase of a 100 Ω BC fault at distance of 2% from Bus M. The CIS supplies the fault current at bus M and the system fault level at bus N is set a 1.5 GVA as in Section 3.2. It is observed that the current magnitudes are similar to each other and the phase angle separation between the waveforms is high, i.e., approximately 120º, when the CIS is present. This has the impact of reducing differential current while increasing restraint current, which impacts relay sensitivity leading to protection failure in this case. It is observed that for phase-to-earth faults, an angle difference is present but not as severe as phase-to-phase faults. Examining the analysis presented in Section 2, this can be attributed to the distribution of zero sequence currents in the faulted network for phase-to-earth faults as this is not impacted by the CIS due to the transformer connection.

In contrast, when the fault contributions at both buses consist of typical SG fault characteristics, there is very little angular difference as shown in Fig. 9(b). For comparison the simulations in the previous case studies were repeated with a voltage source, rated at similar fault levels to the CIS ratings, supplying the fault contribution at bus M. Fig. 10 illustrates an example of this comparison, where in all cases, the LCD relay operated with high sensitivity.

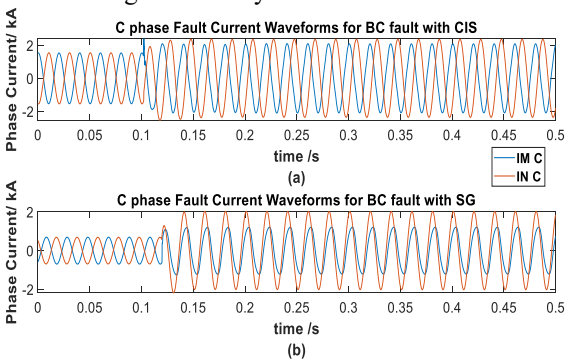

Fig. 9 Phase C fault current waveforms for BC fault: (a) With CIS at Bus M, (b) With SG at Bus M

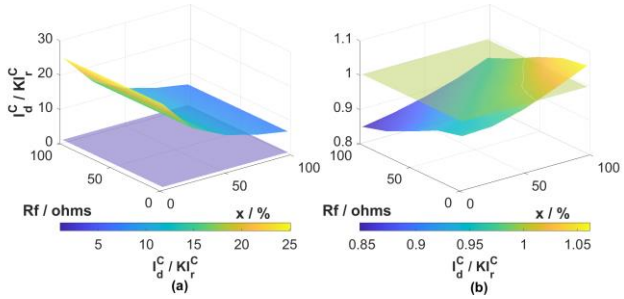

Fig. 10 Comparison of phase C LCD performance for BC fault: (a) With SG at Bus M, (b) With CIS at Bus M

4 Conclusion

This paper presented the analysis of the performance of LCD in the presence of CIS interfaced to low fault level conditions. Extensive simulations under different fault conditions, CIS ratings and system fault levels have been performed to evaluate the impact of integration of CIS on the performance of the LCD. Risks of protection failures have been observed for phase-to-phase faults, where the fault at one of the faulted phases might not be detected. This may be an urgent issue for utilities that adopt single pole tripping as phase-to-phase faults may be misclassified as phase-to-earth faults, resulting in a faulted phase not being isolated. Furthermore, for both AG and BC faults, the LCD relay operates with reduced sensitivity in the presence of CIS when compared to traditional SG fault contributions at both buses. This reduced sensitivity or protection failure occurs when the CIS fault contribution dominates the faulted loop current leading to an increased angle difference in the line terminal currents. The results indicate that this effect is prevalent for high resistance faults close to the CIS bus as this decreases the grid fault contribution. Furthermore, certain system and fault conditions can increase the dominance of CIS fault contribution, e.g. increased CIS penetration, decreased fault level and the fault locations closer the CIS bus. Therefore, more comprehensive tests and analysis with physical LCD relays will be required for fully assessing the risk of LCD failure in future networks, and this presents the future activities of this research work.

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