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Wafer bonding for microsystems technologies

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Abstract

In microsystems technologies, frequently complex structures consisting of structured or plain silicon or other wafers have to be joined to one mechanically stable configuration. In many cases, wafer bonding, also termed fusion bonding, allows to achieve this objective. The present overview will introduce the different requirements surfaces have to fulfill for successful bonding especially in the case of silicon wafers. Special emphasis is put on understanding the atomistic reactions at the bonding interface. This understanding has allowed the development of a simple low temperature bonding approach which allows to reach high bonding energies at temperatures as low as 150°C. Implications for pressure sensors will be discussed as well as various thinning approaches and bonding of dissimilar materials.

Keywords: Wafer bonding; Fusion bonding; Pressure sensors; Interface reactions; Hydrophilic bonding; Hydrophobic bonding

1. Introduction

'Wafer bonding' refers to the phenomenon that mirror-polished, flat and clean wafers of almost any material, when brought into contact at room temperature, are locally attracted to each other by van der Waals forces and adhere or 'bond' to each other. This phenomenon has been known for a long time for optically polished pieces of materials and was first investigated for polished pieces of quartz glass by Lord Rayleigh in 1936 [1]. Only in the early 1980s almost simultaneously an attempt was made by researchers at Toshiba [2] and IBM [3] to use this room temperature adhesion phenomenon coupled with an appropriate heating step for silicon wafers in order to replace epitaxial growth of thick silicon wafers or to fabricate Silicon-On-Insulator (SOI) structures, respectively. Shortly afterwards, as an extension of the well established 'anodic bonding', the bonding of structured silicon wafers was applied for the fabrication of micromachined pressure sensors and termed 'silicon fusion bonding' [4]. Wafer bonding can simply be used as a specific joining technique for all kinds of applications not only in the growing area of microsystems technology which is the subject here, but also in the area of non-linear optics and light-emitting diodes. Wafer bonding approaches are not restricted to silicon/silicon bonding but may be applied to all kind of material combinations involving silicon or other materials [5]. The availability of a variety of precision thinning approaches discussed later allows the transfer of thin layers from one wafer to another.

In the following, we will first discuss the best investigated and understood case of silicon/silicon wafer bonding including an annealing step (Section 2) and then turn to the atomic reactions at the bonding interface (Section 3), thinning procedures (Section 4) and bonding of dissimilar materials (Section 5). Since the literature on wafer bonding is fairly extensive we will not try to be exhaustive in terms of references but refer to recent conference proceedings [6–9], review articles [10–15], a special 1995 issue of the Philips Journal of Research [16] and a book on this subject [17].

2. Silicon wafer bonding and heat treatments

The fabrication of materials combinations in microsystems technologies by wafer bonding usually consists of a number of basic steps which will be outlined and detailed for the case of silicon wafers.

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(i) The surfaces of two mirror-polished silicon wafers, which may or may not contain structures such as cavities are conditioned and prepared for the bonding process. The wafers may be thermally oxidized or just contain a native oxide which is made hydrophilic by a proper surface treatment. The wafer surfaces are then typically covered by one or two monolayers of water. The surfaces may also be activated additionally by an appropriate plasma treatment. The surface oxide may also be removed by a dip in hydrofluoric acid which leads to a hydrophobic hydrogen coverage of the silicon surfaces.

(ii) The two mirror-polished wafer surfaces are brought into contact at room temperature in air either in a conventional cleanroom of class 10 or better or in a so-called microcleanroom (Fig. 1) [18] in order to avoid particles between the wafers. Equipment to perform aligned wafer bonding and/or wafer bonding in vacuum is also commercially available. Usually the bonding is initiated at a certain point by slightly pressing the wafers together locally. The bonded area then spreads over the whole wafer in a couple of seconds.

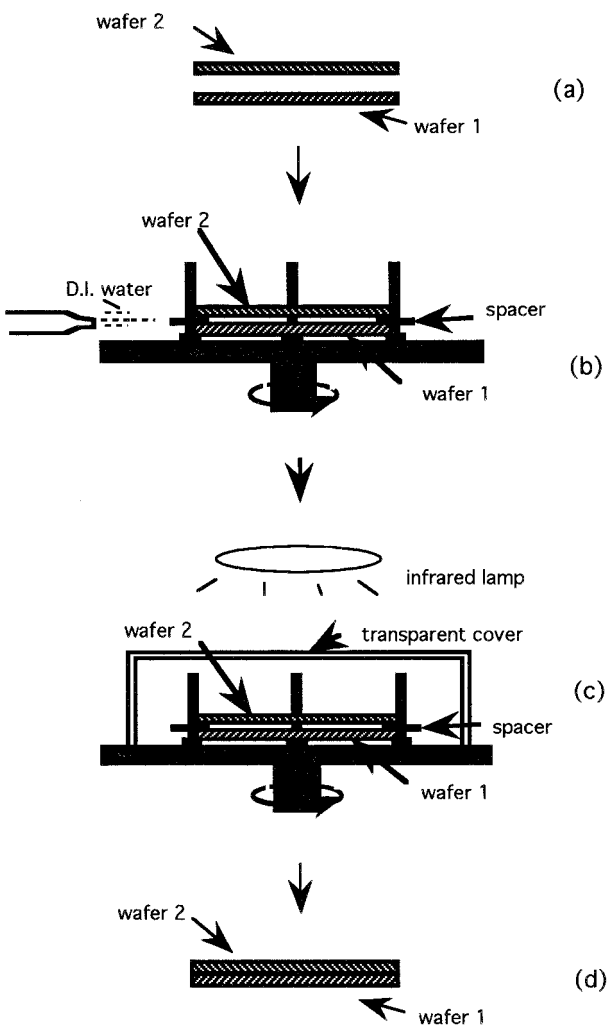

Fig. 1. Schematic of microcleanroom setup and procedure [18].

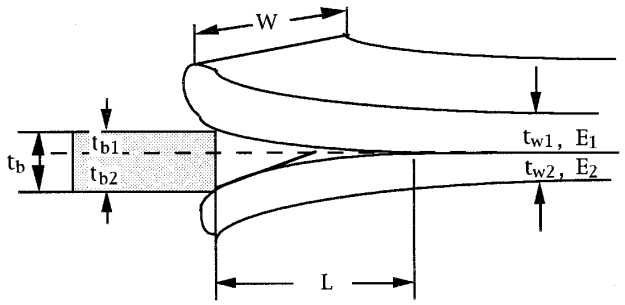

Fig. 2. Schematic of crack-opening method to determine bonding or surface energy.

(iii) Directly after room temperature bonding, the adhesion between the two wafers is determined by van der Waals interactions or hydrogen bridge bonds and one or two orders of magnitude lower than typical for covalent bonding. For most practical applications, a higher bond energy is required which may be accomplished by an appropriate heating step. This heating step is frequently performed at temperatures as high as 1100°C. Treatments at intermediate temperatures or even at room temperature are also possible if performed properly, as will be discussed later.

(iv) For many (but not all) applications, one of the bonded wafers has to be thinned down to a thickness between about 100 nm to some micrometers depending on the specific application. Many different approaches have been developed to accomplish this thinning requirements as will be discussed later.

In the following, we will comment on some selected specific questions associated with the above steps.

Whether two wafers bond depends on the bonding energy at room temperature and the roughness and waviness of the two wafers. The bonding energy may be characterized by the energy associated with opening the surface by the so-called crack-opening method first described by Maszara et al. [19] and schematically shown in Fig. 2. In the case of bonded pairs with identical wafers of thickness t_w and $E_1 = E_2 = E$, where E is Young's modulus, the expression for the surface energy per area γ is

$$\gamma = \frac{3Et_w^3 t_b^2}{32L^4} \quad (1)$$

The various parameters are given in Fig. 2. For wafers of different thickness and/or elastic properties, analogous formulae are available [20]. Eq. (1) holds only for unstructured wafers. For structured wafers (e.g., with cavities) only a fraction f_b of the surface area is available for bonding and γ in Eq. (1) has to be replaced by γf_b. Other arrangements for mechanical testing are shown in Figs. 3 and 4. The arrangement shown in Fig. 3a does not give the surface energy but the tensile strength which strongly depends on microcracks and sample preparation.

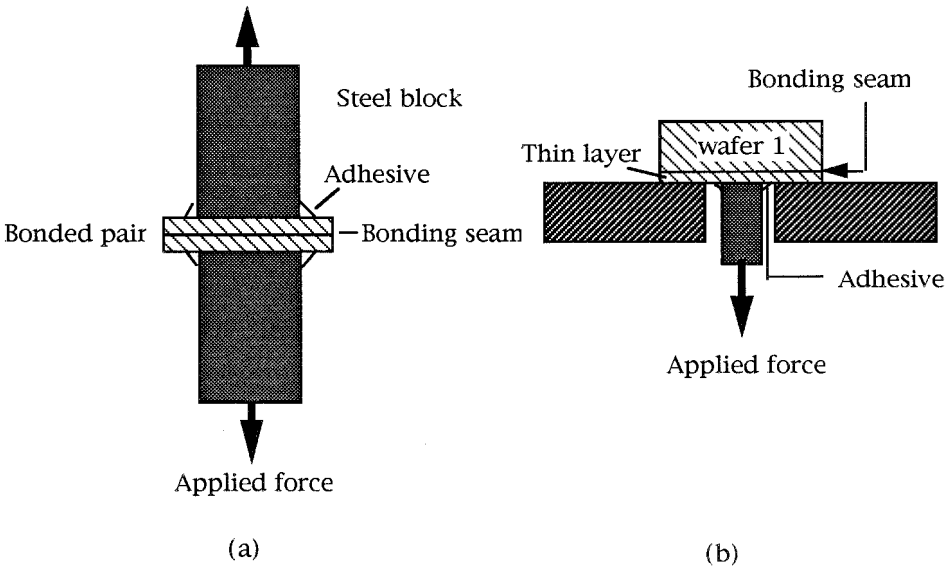

Fig. 3. Schematic of different methods of testing of mechanical properties of bonding interfaces [17].

The surface energy γ is typically around 100 mJ/m^2 for hydrophilic surfaces and around 20 mJ/m^2 for (hydrogen covered) hydrophobic silicon surfaces generated by an HF dip [21,22]. It is nowadays also possible to calculate at least approximately whether wafers with a certain waviness and roughness will bond or not [17]. For these calculations, let us assume gaps between wafers caused by a flatness nonuniformity with a lateral extension R (or spatial period $2R$) much larger than their depth (or gap height) h as schematically shown in Fig. 5. The condition for gap closing depends on the ratio of R to the wafer thickness t_w.

For $R > 2t_w$ (Fig. 5a), the condition for gap closing depends on wafer thickness t_w and is given by

$$h < \frac{R^2}{\sqrt{\frac{2}{3}\frac{E' t_w^3}{\gamma}}} \qquad (2)$$

where E' is given by $E/(1-\nu)$ with ν being Poisson's ratio. For $R < 2t_w$ (Fig. 5b), the condition for gap closing is independent of wafer thickness t_w and given by

$$h < 3.6(R\gamma/E')^{1/2} \qquad (3)$$

In Fig. 6 the regions of gap closing or not closing are shown for two silicon wafers of equal thickness t_w based on $\gamma = 100$ mJ/m^2 and for various different values of t_w. For structured wafers, in expressions (2) and (3), γ may approximately be replaced by γf_b.

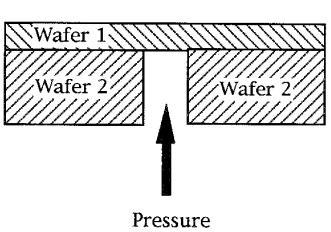

Fig. 4. Test structure to measure bonding or surface energy.

In practice, the flatness variation of 1–3 μm over commercial 4-in. silicon wafers poses no obstacle for wafer bonding at room temperature because the deformation of the two wafers can easily accommodate this scale of surface waviness. Bow and warpage of wafers up to about 25 μm are also tolerable. The above expressions may be used to predict whether wafer bonding is possible provided γ and the waviness of the surface are known. In reality the waviness is represented in a whole Fourier spectrum of amplitudes for certain wavelengths. If not only one single spatial frequency (like the macroscopic bow) is dominating, an integral formulation has to be used. The developed theoretical expressions also show that even infinitely thick pieces can be bonded provided the surface flatness is sufficiently good [23] as has been known to occur for optically polished bulk pieces of glasses or metals since almost hundred years.

For bonding a standard silicon wafer to a silicon wafer with cavities, the above equations can also be used to predict whether the parts of the unstructured wafer covering the cavities will bond to the bottom of the cavity [17].

The room temperature bonding step may either be performed in air under normal pressure or under vacuum conditions, as may be dictated by the requirement of evacuated cavities for various micromechanical sensors. Bonding even under reduced pressure (low vacuum) is helpful in bonding wafers with high surface roughness. Bonding in different atmospheres such as oxygen or nitrogen is also possible. The different behavior of the bonding or surface energy for hydrophobic and hydrophilic silicon wafers as a function of heat treatment temperature for extended times of many days after room temperature bond-

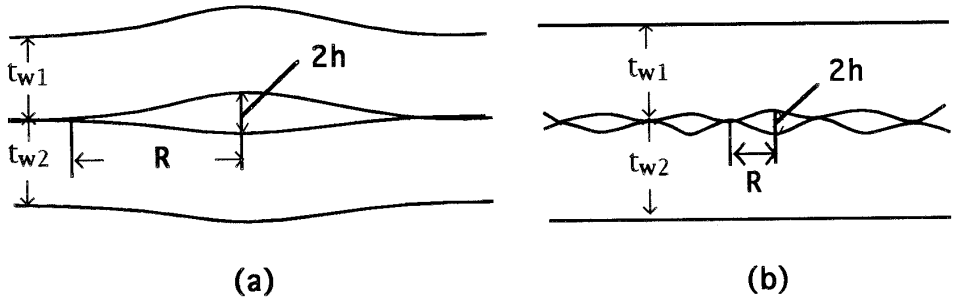

Fig. 5. Schematic of surface waviness.

ing in air is shown in Fig. 7. It can be seen that for hydrophilic surfaces about half of the full bonding energy can be reached already at temperatures around 150°C. Bonding in (low) vacuum allows to reach almost full bonding energy [24] at such low temperatures.

3. Reactions at bonding interfaces

There is a clear trend towards wafer bonding applications in micromechanics and microelectronics which do not allow annealing of the bonded structure at high temperatures, since the structure either contains temperature sensitive device or metallization layers or consists of different materials with vastly different thermal expansion coefficients. In order to address these needs of low temperature bonding processes, we systematically investigated the atomistic processes occurring at the bonding interface for different surface chemistries. We will not discuss here the also promising low temperature bonding approach based on a plasma treatment of the silicon surfaces [25–27].

Most silicon wafers used for wafer bonding are covered with either a thin native oxide (with a thickness of about 2 nm) or a purposely grown thermal oxide (as necessary for SOI substrates or for parts in microsystems which have to be electrically isolated) which has been rendered hydrophilic by a proper cleaning procedure. These oxides are typically covered with a monolayer or two of water molecules adsorbed on OH groups associated with the oxide. These hydrophilic surfaces are very similar to those present on fused quartz. Alternatively, silicon surfaces may be dealt with in diluted HF leading to the removal of native oxide layers and a direct hydrogen coverage of the silicon surfaces which renders the surfaces hydrophobic. Both hydrophilic and hydrophobic silicon wafers may be bonded at room temperature by relatively weak hydrogen bridge or van der Waals bonds. In both cases subsequent heating is required to increase the bonding energy for practical applications. Of course, only hydrophobicly bonded wafers are free of an insulating oxide layer after bonding and annealing.

For hydrophobicly bonded wafers during heating, the reaction consists of sequential hydrogen desorption (depending on the specific bonding configuration) and silicon–silicon covalent bond formation according to

$$\equiv\text{Si–H} + \text{H–Si}\equiv \Rightarrow \equiv\text{Si–Si}\equiv + \text{H}_2 \qquad (4)$$

At temperatures up to about 500°C, the hydrogen is not diffusing into the silicon but rather diffuses along the bonding interface.

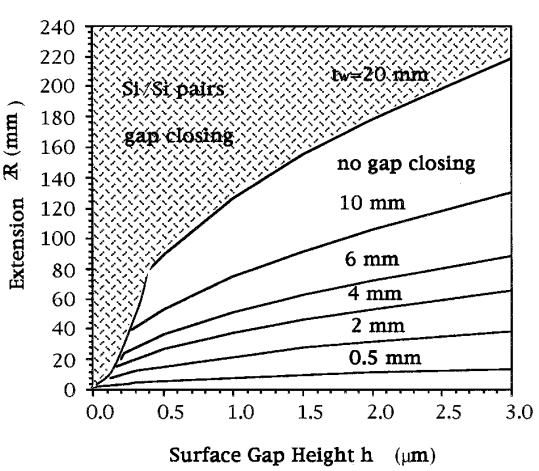

Fig. 6. Calculation under which conditions gap closure does or does not occur for different assumed wafer thicknesses from 0.5–20 mm and $\gamma = 100\ \text{mJ/m}^2$ [17].

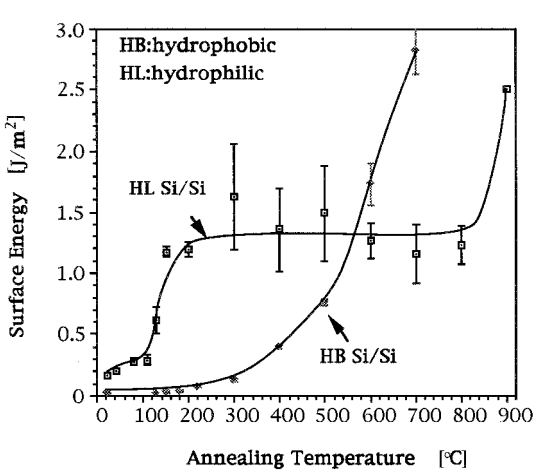

Fig. 7. Saturation values of surface or bonding energy measured by the crack opening method as a function of temperature after long-time heat treatments (up to 100 h) [17].

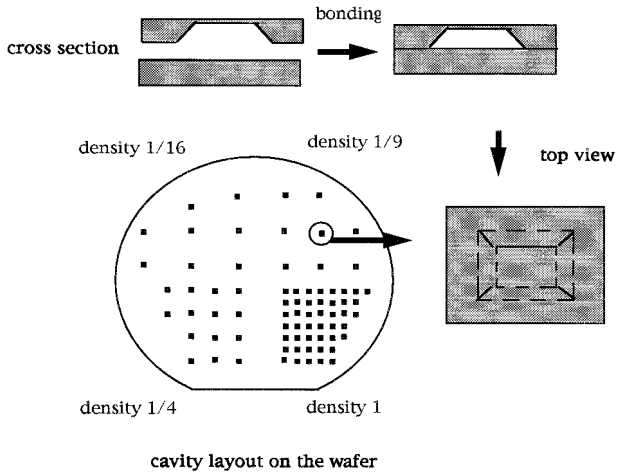

Fig. 8. Cavities used for measuring pressure increase due to interface reactions. (a) Schematic of test structure cavity. (b) Cavity layout on the wafer [31].

In the case of hydrophilic wafer bonding, the end result, namely the generation of molecular hydrogen, is the same but there are intermediate steps involved. Initially there exists molecular water at the interface in terms of monolayers of water adsorbed on hydrophilic oxides. Molecular water will also come partly from the reaction

$$\equiv Si{-}OH + HO{-}Si\equiv \Rightarrow = Si{-}O{-}Si\equiv + H_2O \qquad (5)$$

which starts to form strong covalent bonds across the bonding interface at temperatures above about 120°C. Molecular water will oxidize the surrounding crystalline silicon and form molecular hydrogen via the reaction

$$Si + 2H_2O \Rightarrow SiO_2 + 2H_2 \qquad (6)$$

A thin oxide favors reaction (6) and therefore the formation of strong bonds for a given relatively low temperature as compared to the case of much thicker thermal oxides through which the water molecules have to diffuse. On the other hand, the hydrogen molecules resulting from reaction (6) cannot appreciably be dissolved in the silicon and therefore generate a gas pressure at the interface. This pressure, which may lead to formation of interface bubbles or weakening of the interface bonding, decreases with increasing oxide thickness (since the hydrogen can be dissolved in the oxide). Therefore, for strong and high quality bonding a combination of a very thin oxide (which favors getting rid of the water via reaction (6)) and a thick oxide (which reduces the pressure at the interface) appears to be most favorable [28], as indeed was found experimentally [29].

All these reactions can in detail be investigated by Multiple Internal Reflection Spectroscopy which also allows to distinguish different reaction behavior of hydrophobic wafer surfaces of different crystallographic orientations. For details the reader is referred to the excellent articles by the group of Chabal at Bell Laboratories [30].

In the present paper we will concentrate on the movement of the reaction product (molecular hydrogen) along the interface which was investigated by Mack et al. [31,32]. For this purpose arrays of cavities of the same size but with different areal densities where fabricated in such a way that the remaining silicon membrane can be used to measure the pressure in the cavities sensitively (Fig. 8). The silicon wafers with cavities where bonded to unstructured silicon wafers either hydrophobicly or hydrophilicly under conditions of high vacuum. The bonded wafers were then heated to different temperatures and the pressure increase was measured later at room temperature as a function of time, heat treatment, and cavity density. An example of the results are shown for hydrophilic wafers in Fig. 9 [31]. It is obvious that the lower density cavities show a higher increase in pressure corresponding to the larger available bonding area around a cavity.

By mass spectrometry the main constituent in the cavities was shown to be molecular hydrogen for both hydrophilic and hydrophobic wafers [32]. The generated hydrogen gas can diffuse along the interface even at room temperature.

For both hydrophilic and hydrophobic bonding a gas pressure will develop in cavities even if the room temperature bonding is performed under high vacuum conditions. This is also true for anodic bonding [32,33] in which case oxygen develops during the bonding procedure. It would be desirable for absolute pressure sensor to avoid any gas development at all. Bonding of clean silicon surfaces without any absorbed layers of water or hydrogen should, in principle, allow this goal to be achieved. Experimentally, clean silicon surfaces require ultra high vacuum (UHV) conditions. We managed recently to obtain large area and self-propagating 4 in. (100) silicon wafer bonding under UHV conditions at room temperature [34,35], although not yet for structures containing cavities. Bonding is so strong, that without any subsequent heat treatment the bonded samples fractured in tensile tests at other locations than the interface.

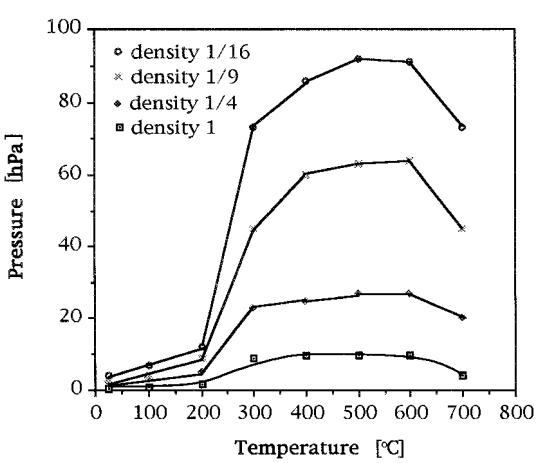

Fig. 9. Pressure increase in cavities after hydrophilic bonding and annealing at specified temperatures for 70 h [31].

4. Thinning procedures

In many cases one of the wafers has to be thinned to create a thin single crystalline silicon layer. Various thinning approaches have been developed and are used in commercial SOI production.

(i) Precision polishing allows the fabrication of layers down to about 1 μm with a thickness variation of about 0.3 μm over the whole wafer which is good enough for most bipolar applications [36].

(ii) The use of a p^+-boron-doped silicon epilayers stress compensated by the incorporation of the proper amount of germanium as etch stop layers leads to a very good thickness uniformity also in the 10 nm range [37].

(iii) An etch-stop based on a porous silicon sacrificial layer has been developed with similarly good thickness variations [38].

(iv) An especially elegant procedure has been suggested by Bruel and termed SMART-CUT [39,40]. It is based on hydrogen implantation before bonding which leads to the splitting of silicon wafers along hydrogen-filled microcracks induced by the precipitation of the implanted hydrogen during a heating step after bonding. The smart-cut procedure is schematically shown in Fig. 10 [20]. The big advantage of this procedure, which also allows a thickness variation in the 10 nm range, is that split wafers may be reused after some soft polishing (which is also required for the transferred layer) since its thickness has changed only by about a micrometer or less. Co-implantation of a much lower dose of boron allows to decrease the temperature and/or time of splitting considerably ('smarter-cut' [41]) which is most important for bonding materials of different coefficients of thermal expansion such as silicon and quartz.

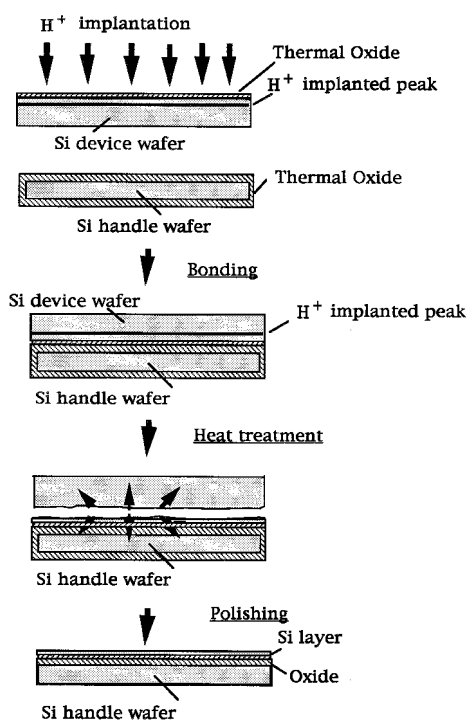

Fig. 10. Schematic of hydrogen-implantation induced layer splitting ('smart-cut') [17,39].

Layer splitting by hydrogen implantation and wafer bonding is especially interesting for expensive materials such as single crystalline SiC [42,43], diamond [42], or GaAs [44] for which the smart-cut procedure also works. Repeated transfer of thin layers onto appropriate inexpensive substrates could allow a large decrease in price of these materials and consequently lead to a more widespread and economic usage.

5. Bonding of other materials

Most materials, if properly polished and their surfaces properly conditioned, do adhere to each other at room temperature and can thus be used for wafer bonding approaches as has been shown by the group of Haisma at Philips [5,10,16]. The materials are certainly not limited to semiconductors and can be present in single crystalline, polycrystalline or amorphous form. Examples of different material combinations fabricated by wafer bonding include Si on sapphire for improved SOS material [45], crystalline quartz on silicon for high frequency applications [46], Si on fused quartz or glass for HDTV projection masks [47], and GaAs or InP on Si for combining opto- and microelectronics [48–50]. Interesting applications are combinations of different III–V compounds for the fabrication of vertical cavity surface emitting lasers (VCSEL) [51] and light-emitting diodes (LED) [52] pioneered at Hewlett-Packard. For the bonding of III–V compounds the wafer bonding process frequently is performed not at room temperature but at elevated temperatures (around 300–500°C) in flowing hydrogen or at even higher temperatures under the influence of a weight [53,54].

Wafer bonding may be performed via all kinds of intermediate layers such as oxides, nitrides, metals and silicides. Especially important is the bonding via polished polysilicon layers not only for advanced dielectrically isolated (DI) wafers [55] but also for the fabrication of complex three-dimensionally integrated devices or for micromechanics. In this context, the importance of chemomechanical polishing (CMP) should be stressed which nowadays is widely available in microelectronics facilities.

If two different materials are combined, a problem due to a mismatch of the thermal expansion coefficients may arise during the heating step following room temperature bonding. This may lead to debonding, interface sliding or breakage of the bonded pair at elevated temperatures [56]. Only a few cases of interesting materials combinations are known for which the two materials have sufficiently close thermal expansion coefficients. Examples are silicon and silicon carbide, silicon and glasses specifically developed for this purpose and last not least GaAs and sapphire

which might become important for combining GaAs based electronics with superconducting microwave devices based on thin films of high temperature superconductors epitaxially grown on sapphire. In the case of GaAs/sapphire bonding the bonding has to be performed at elevated temperatures around 500°C in order to avoid undesirable interface bubbles [57].

6. Outlook

Wafer bonding is already established for the industrial fabrication of some sensors, but it is still not as common as anodic bonding. SOI wafers with diameters up to 8 in. fabricated by wafer bonding and various thinning techniques are now commercially available in Japan, the US and Europe. For LEDs wafer bonding or fusion has recently also made its way into production. In many other areas, wafer bonding applications are just in a research or development stage. The development of new techniques such as hydrogen-implantation induced layer splitting is promising also outside of the SOI and even the silicon area.

Wafer bonding offers a new freedom in the design of materials combinations without the common restrictions imposed by the structure (amorphous, polycrystalline, orientation, lattice constant) of the materials to be bonded.

Acknowledgements

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