Wafer-level Au-Au bonding in the 350-450 °C temperature range

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Complete List of Authors:	Tofteberg, Hannah; SINTEF ICT, Microsystems and Nanotechnology Schjolberg-Henriksen, Kari; SINTEF, Microsystems and Nanotechnology Fasting, Eivind; Eivind Fasting, ; Moen, Alexander; Oslo and Akershus University College of Applied Sciences, Taklo, Maaike; SINTEF, Instrumentation Poppe, Erik; SINTEF ICT, Microsystems and Nanotechnology Simensen, Christian; SINTEF Materials and Chemistry,

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Hannah R. Tofteberg[1], Kari Schjølberg-Henriksen[1], Eivind J. Fasting[2], Alexander S. Moen[2], Maaike M. V. Taklo[1], Erik U. Poppe[1] and Christian J. Simensen[1]

[1]SINTEF, Oslo, Norway

[2]Oslo and Akershus University College of Applied Sciences, Oslo, Norway

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1 Introduction

Microelectromechanical system (MEMS) technology enables sensitive and reliable devices to be produced at low cost due to the advantages of batch processing. However, packaging of the individual devices can account for more than 70% of the device cost [1]. Wafer-level bonding lowers these costs substantially. Several bonding technologies are used in packaging of commercial MEMS devices. Glass-frit bonding [2-4], anodic bonding [5, 6] and fusion bonding [7, 8] are well known and widely used techniques for wafer-level packaging and sealing of MEMS devices.

Recently, metal thermocompression bonding has found its application as a hermetic wafer-level packaging technology that facilitates vertical integration. Thermocompression bonding, also referred to as diffusion bonding, is a form of solid-state welding. Pressure and heat are applied simultaneously to bring two metal surfaces into close contact. The atoms can then migrate from lattice site to lattice site joining the interface together [9, 10]. To enable metal-to-metal contact, the bonding mechanism must deform the two surfaces in contact in order to disrupt any intervening surface films [11].

Cu, Al, and Au are the three most commonly applied metals for thermocompression bonding. The lowest process temperature is obtained using Au [9]. Unlike copper and aluminium, gold does not readily form an oxide, and under normal processing conditions, surface cleaning prior to bonding is not necessary. A recent report describes how STMicroelectronics has shrunk the area used for device sealing by more than 30% using Au-Au thermocompression bonding instead of glass-frit bonding [12]. Switching from glass-frit to more environmental friendly metal-based wafer bonding also allows electrical interconnects, improved vacuum control [10] and improved manufacturability [13].

Wafer-level Au-Au bonding in the 350-450 °C temperature range

Eutectic Au-Si bonding is often used for die attach and can occur at temperatures above 363 °C. Disadvantages with eutectic bonding are the inherent Au contamination of the Si and a reportedly limited process control [14, 15].

The reported process parameters for Au-Au thermocompression bonding vary substantially. Bonding temperatures vary from 100 to 450 °C [9, 16] and bonding pressure varies from 0.5 to 120 MPa [12, 17] . For many applications, a low bonding temperature is desired. However, in order to activate a getter material during the bonding process, a bonding temperature of 400 – 450 °C can be demanded [18]. According to Park *et al*. and Taklo *et al*., increased bonding temperature improves the bond quality [10, 19], while Kurotaki *et al*. did not find any relationship between bonding temperature and bond strength [16]. Several authors report that an increased bonding pressure increases bond quality [10, 17, 19], while the bonding time has been found to be of low importance for the final bond strength [10, 17]. The helium leak rate of Au-Au thermocompression bonds was measured to be 2.74×10^{-11} Pa m^3/s by Park *et al*.and 3.9×10^{-10} Pa m^3/s by Xu *et al*., indicating that high quality hermetic packaging can be realized using this technology [10, 20]. As diffusion barrier and adhesion layer Cr, Ti, W, TiW and NiCr have been used [10, 12, 16, 17, 19, 20].The relatively large discrepancy in the reported bonding parameters for Au-Au thermocompression bonding indicates that the process is still not fully understood and described. This paper presents an investigation of Au-Au bonding in the temperature range 350 - 450 °C. The strength of the chips with different frame design is reported and the fractured surfaces are characterized after chip delamination.

2 Experimental

2.1 Chip design

Four different bond frames were designed. All frames were quadratic, with an outer dimension of 3×3 mm^2. Frame widths of 100, 200, and 400 µm with straight corners were named F100, F200, and F400. A frame of width 200 µm with rounded corners (F200R) was also designed, as shown in figure 1. The frame types and their nominal bond surface areas are listed in table 1. The different chip types, all with a size of 6×6 mm^2, were evenly spread over the wafer to achieve a uniform pressure distribution during bonding. The total area to be bonded for each wafer pair was 525 mm^2. On the whole wafer, there were 54 pcs of each frame type chip.

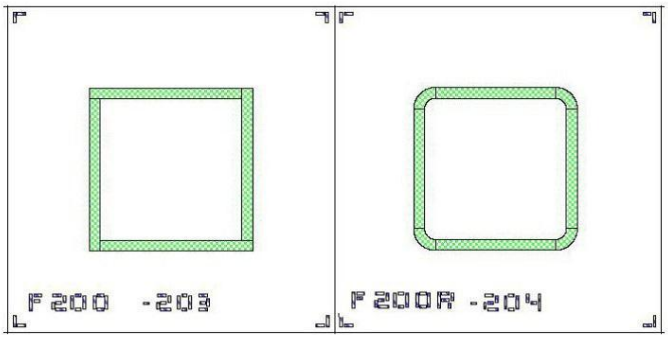

Figure 1. Chips with 200 µm wide bond frames and straight corners, F200 (left), and rounded corners, F200R (right).

Wafer-level Au-Au bonding in the 350-450 °C temperature range

Table 1. Overview of chip designs.

Name	Description	Bond area (mm^2)
F100	Frame, width 100 µm	1.16
F200	Frame, width 200 µm	2.24
F200R	Frame, width 200 µm, rounded corners	2.14
F400	Frame, width 400 µm	4.16

2.2 Chip preparation

Chips were produced by bonding together an etched and a flat wafer. Silicon wafers with <100> orientation and 150 mm diameter were used. The etched wafers were 400 µm thick. The 6 µm protruding bond frames were realized by deep reactive ion etch (DRIE) in an AMS 200 I-Prod (Alcatel). Thermal SiO_2 was used as masking material, and was removed after DRIE. The flat wafers were 630 µm thick. Metal layers of 200 nm TiW and 1 µm Au were sputter deposited on both flat and etched wafers.

Wafer laminates were created by bonding an etched wafer and a flat wafer in a wafer bonder (SB6e, Suss MicroTec). The bonding chamber was flushed with N_2 prior to bonding. The thermocompression bonding was performed in a vacuum ambient applying a tool pressure of 5 bar at 350 – 450 °C for 15 or 30 minutes. The applied tool pressure translated to an average pressure of 21 MPa on the protruding surface to be bonded. Three combinations of bonding time and temperature were applied as listed in table 2. Figure 2 shows a schematic cross-section of a chip.

Table 2. Overview of bond parameters for the three realized wafer laminates.

Wafer laminate	Temperature (°C)	Time (min)
Au350	350	30
Au400	400	15
Au450	450	30

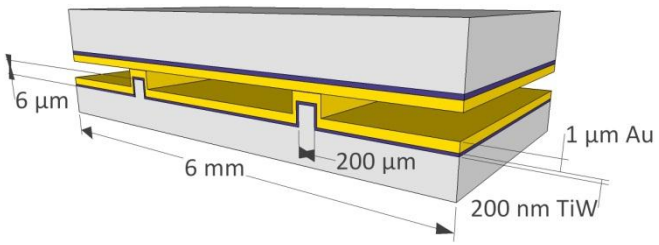

Figure 2. Schematic cross-section of a F200 chip. Two Si wafers sputter deposited with 200 nm TiW and 1 µm Au were bonded. The etched wafer had protruding bond frames.

The laminate Au350, see table 2, was prepared for electrical measurements. A layer of 1µm Al was sputter deposited and patterned for electrical contacts on both sides of the bonded laminate and sintered at 350 °C for 30 minutes. All three laminates were diced into individual chips, each chip containing one frame. One of the dice from Au450 was etched in KI after pull testing.

2.3 Characterization

Individual chips were pull tested. Diced chips were glued to screws which were mounted in a pull tester (MiniMat 2000 Rheometric Inc.). The elongation versus applied force was recorded, and the force for which fracture occurred was noted. A total of 98 chips were tested. For each frame design and bond temperature 3 - 13 chips (on average 8 chips) were tested. The bond strength defines the strength of the complete bonded system and was calculated as the fracture force divided by the bond

area. The nominal strength was calculated using the nominal bond area. During the visual inspection of the fractured surfaces, narrow lines of additional bonded areas were observed on some chips bonded at 400 °C and 450 °C. Examples of such lines are seen in Figure 5 c and 5d. Therefore, the actual bonded area was assumed to be larger than the nominal bonding area for chips with such lines. To avoid an overestimate of the bond strength, the actual bonding area was estimated. Based on a visual quantification of the number and length of lines, the additional bonding area was estimated to be 5%, 10%, 25%, 50%, or 100% of the nominal bond area. In case of doubts, the highest actual bond area was chosen in order to avoid an overestimate of the bond strength. The corrected bond strength was calculated using the estimated actual bonded area, and therefore represents a minimum estimate of the actual bond strength. It should be noted that the pull testing tests the strength of the whole bonded chip. Fractures are likely to initiate in the mechanically weakest points of the chip. Therefore, the applied definition of bond strength provides a measure of the minimum bond strength for the Au-Au bond.

The fracture surfaces were investigated by optical microscopy (PolyVar Met), macro photography (Canon EOS 600D) and scanning electron microscopy (SEM, FEI Quanta FEG 600). An electron dispersive x-ray analysis (EDX, EDAX) was performed on selected fractures to determine the materials present at the fracture surface. Also the surfaces adjacent to the bonded areas were studied with SEM and EDX. The roughness of the Au surface was measured by white light interferometry (WLI, Zygo NewView 6300) both before and after bonding.

The fracture surfaces were classified as adhesive or cohesive. Adhesive fracture is a fracture at the interface between two materials. Cohesive fracture occurs inside the bulk of a material.

3 Results

The fracture forces for the pull tested chips are shown in figure 3. The nominal and corrected average bond strengths can be seen in figure 4.

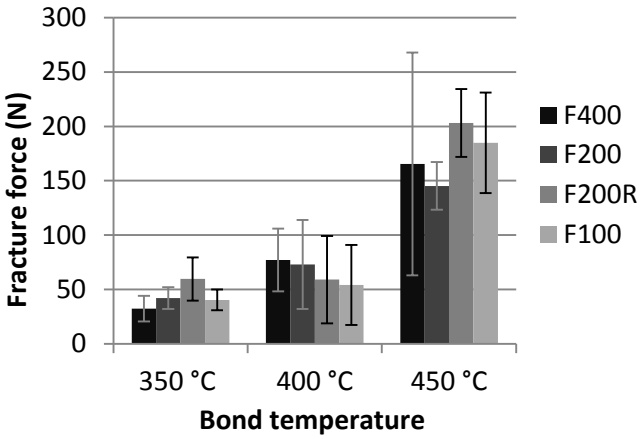

Figure 3. Average and standard deviation of the force at which fracture occurred. All four frame designs from laminates Au350, Au400 and Au450 are plotted. The error bars show the ± 1 standard deviation.

Wafer-level Au-Au bonding in the 350-450 °C temperature range

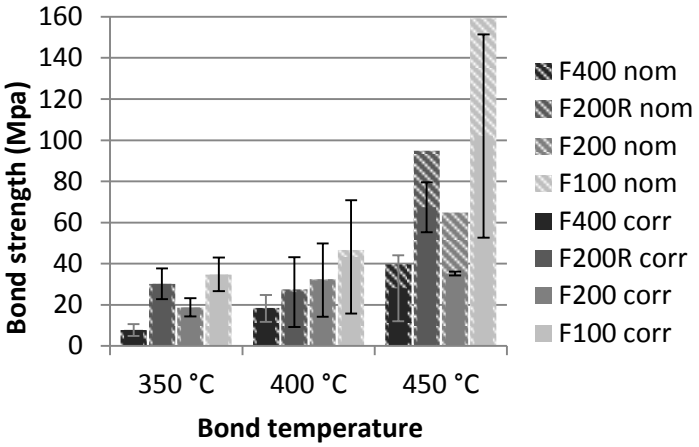

Figure 4. Average bond strength of the four frame designs from laminates Au350, Au400 and Au450 calculated from both nominal (hatched columns in figure) and corrected (solid columns) bond areas. The error bars show the ± 1 standard deviation calculated for the corrected values.

Laminate Au450 had the highest fracture force values, with all four chip types having an average fracture force above 145 N. Laminate Au400 was the second strongest, and slightly stronger than laminate Au350 for all frame designs, except F200R. Table 3 lists the average values and the standard deviation of the bond strength for each laminate and chip type.

Table 3. Average bond strength values and standard deviation for the four frame designs from laminates Au350, Au400 and Au450. Both nominal (calculated using nominal bond area) and corrected (calculated using maximum actual bond area) values of bond strength are listed.

Laminate ID	Bond strength (MPa)									
	F400		F200R		F200		F100		Average	
	nom	corr	nom	corr	nom	corr	nom	corr	nom	corr
Au350	8 ±3		30 ± 7		19 ± 4		35 ± 8		23 ±16	
Au400	19 ± 7	18 ± 7	28 ± 19	26 ± 17	33 ± 18	32 ± 18	47 ± 32	43 ± 28	31±24	30 ±21
Au450	40 ± 25	28 ± 16	95 ± 15	67 ± 12	65 ± 10	35 ± 1	159 ± 40	102 ± 49	90 ±55	58 ±43

Pictures of typical fracture surfaces after pull testing are shown in figure 5.

Wafer-level Au-Au bonding in the 350-450 °C temperature range

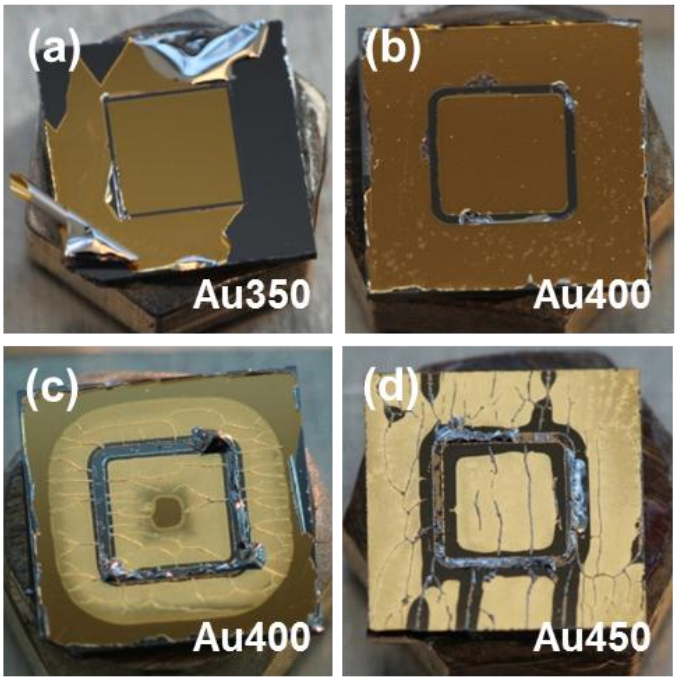

Figure 5. Macro photographs of fractured surfaces of chips from laminates Au350, Au400 and Au450. In (a) the sputtered metal film has delaminated at the interface between Si and TiW. Close to the edges of the chips the metal film has delaminated in(b) and (c). In (c) the gold has a matt appearance in the area close to the bond frame. Farther away the gold surface is glossy. In (d) the whole gold surface has a matt and cracked appearance.

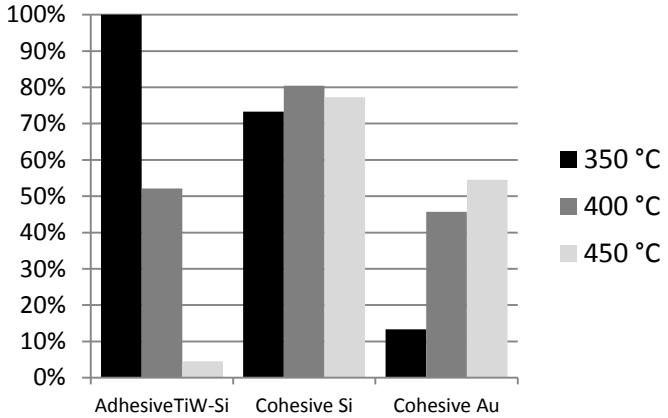

Figure 6. A comparison of fracture surfaces from laminates Au350, Au400 and Au450 with percentages of chips that showed regions of adhesive TiW-Si fracture, cohesive Si fracture, and cohesive Au fracture. There was normally more than one fracture type on each chip.

The fracture modes observed in the investigated chips are illustrated in figure 6. Chips from laminate Au350 had mainly adhesive fracture at the TiW-Si interface on the flat wafer. All chips except chip type F400 also had cohesive Si fractures in 5 to 45% of the bonded area. Bond frames from laminate Au400 had a mix of adhesive fracture at the TiW-Si interface, cohesive Si fracture, and cohesive Au fracture. Adhesive fracture at the Si-TiW interface was observed in more than half of the chips on laminate Au400. Cohesive fractures in the bulk silicon were seen in 80% of the chips, but the amount varied from 5 to 100% of the bonded area. On laminate Au450, adhesive fracture at the TiW-Si

interface was seen on only one tested chip. 77% of the chips from laminate Au450 had cohesive Si fracture, covering an area ranging from 20% to 100% of the bond frame.

On chips from laminate Au350, a large amount of the metal film outside the bond frames had delaminated. The film delaminated at the interface between the TiW film and the bulk Si. Also on most of the chips from laminate Au400, the gold film delaminated outside the bond frame between TiW and Si, but only at a small distance from the chip edges where the gold was still glossy. This can be seen in figure 5(b) and 5(c).

On the chips from laminate Au400 that had cohesive bulk silicon fracture in a large percentage of the bonded area, and on all chips from laminate Au450, the visual appearance of the gold in the unbonded area had changed. On these chips, the gold had a matt appearance. The difference can be seen in figure 5(c), where there is both glossy and matt gold. Table 4 shows WLI measurements of the surface roughness of glossy and matt gold on laminates Au400 and Au450, as well as the as-deposited gold roughness. The transition over a chip from glossy to matt gold can be seen in figure 7. The chips from laminate Au350 did not have any unbonded gold with matt appearance. Figure 8 shows the bond strength of chips from laminate Au400 comparing chips with more than 50% matt gold surface and chips with mostly glossy gold. The fracture force of the chips with more than 50% matt gold surface was more than twice the value of the chips with mostly glossy gold. As can be seen in figure 9 adhesive TiW-Si fracture was more than twice as common on chips with glossy gold.

Table 4. Surface roughness measured by WLI of glossy and matt unbonded gold on chips from laminates Au400 and Au450.

	Mean rms (nm)
As-deposited Au	1.8
Glossy Au on Au400 and Au450	2.0
Matt Au on Au400	170
Matt Au on Au450	320

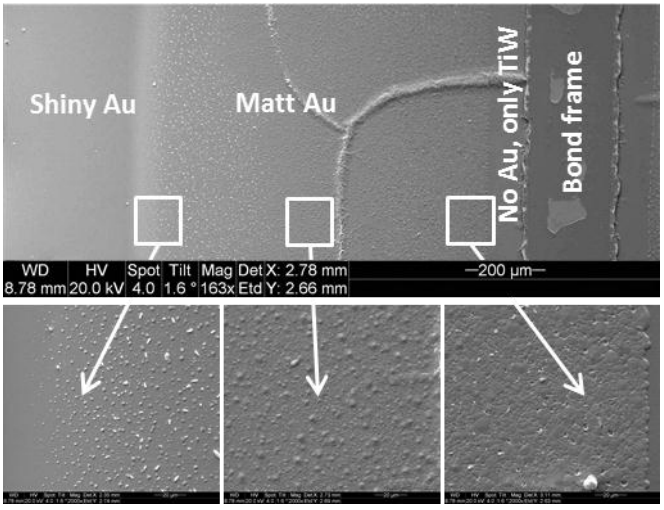

Figure 7. Scanning electron micrograph of Au surface from laminate Au400, overview (top) and zoomed areas or the transition from glossy to matt gold (left), in the middle of the matt gold (center) and close to the bond frame (right).

Wafer-level Au-Au bonding in the 350-450 °C temperature range

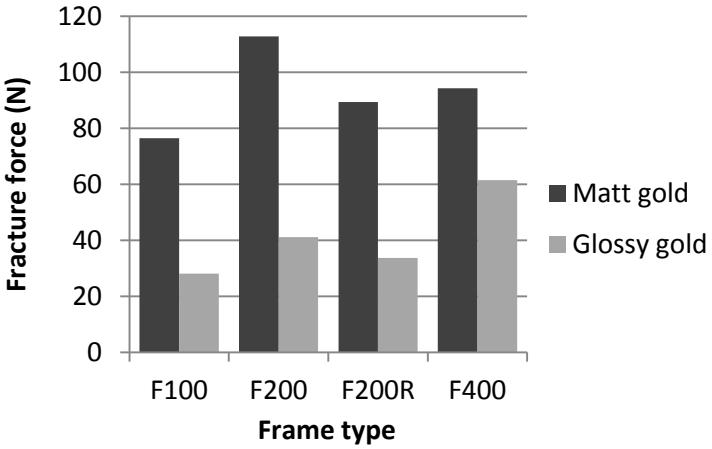

Figure 8. Comparison of fracture force of chips from laminate Au400. Dark columns show the fracture force of chips with more than 50 % matt gold surface. Light columns are chips with mostly glossy gold.

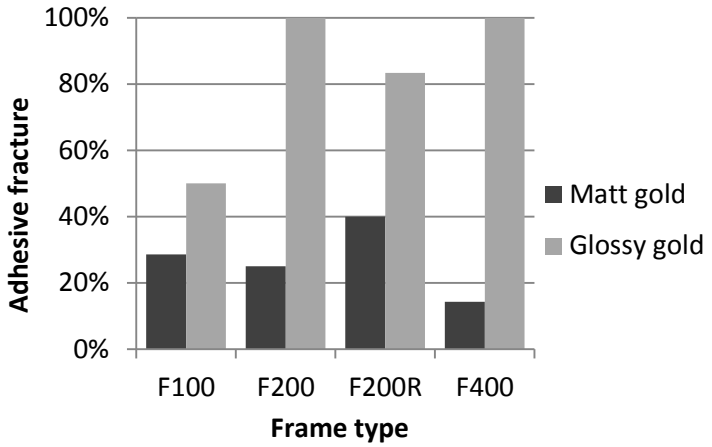

Figure 9. Comparison of the amount of adhesive TiW-Si fracture for chips from laminate Au400. Chips with mostly glossy gold had adhesive TiW-Si fracture more often than chips with mostly matt gold.

All chips from laminates Au400 and Au450 with matt gold had a crack pattern outside the bonded area. This can be seen in figure 5(c) and 5(d). In figure 10 the pattern can be identified as buckles, often surrounded by areas without gold. There were more buckles on the etched wafer than on the flat wafer. Adjacent to the bond frames and the largest buckles, there was no Au left after bonding. SEM and EDX investigations confirmed that there was no Au left in this area, but that TiW was still present.

Wafer-level Au-Au bonding in the 350-450 °C temperature range

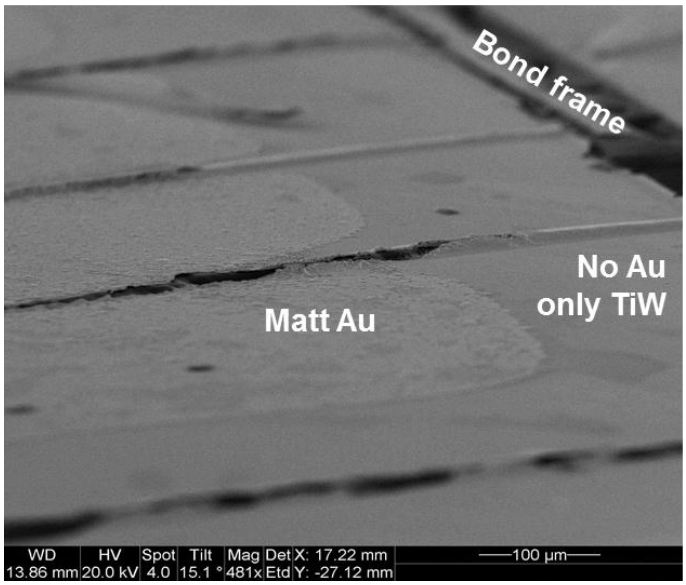

Figure 10. Scanning electron micrograph of the etched side of a chip from laminate Au450. The vertical gold formations are clearly seen. The bonding frame can be seen in the upper right corner. According to EDX scans is there no gold left in the area close to the bonding frame.

Figure 11 shows that in the actual bond frames with cohesive Au fracture, a pattern in the Au was observed. The same pattern, but mirrored, was present on both the flat and the etched wafer. In this patterned area there were also areas with only TiW and no Au. Similar areas with mirrored Au patterns are seen in figure 12.

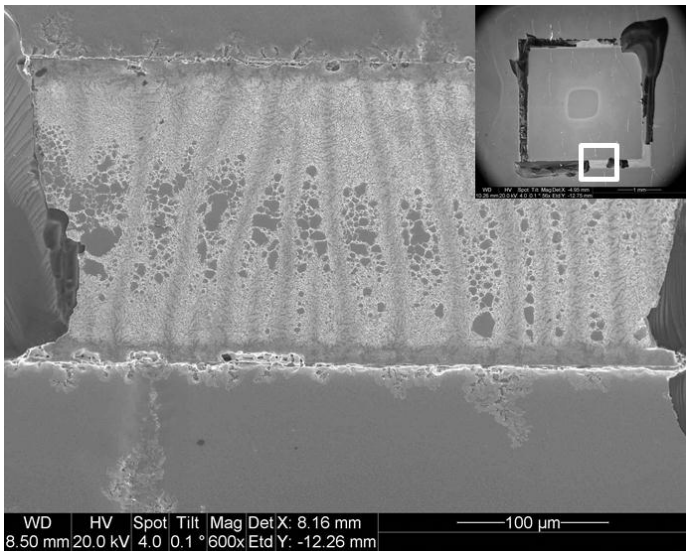

Figure 11. Scanning electron micrograph of bond frame from laminate Au400. In the dark areas of the bond frame EDX scans confirm that there is TiW, but no Au.

Wafer-level Au-Au bonding in the 350-450 °C temperature range

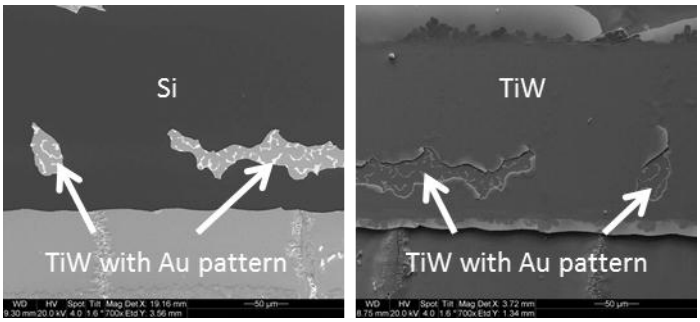

Figure 12. Scanning electron micrograph of bond frame from laminate Au400 with mostly adhesive but also some cohesive Au fracture. On the flat wafer (left) there is almost only Si, with two areas of TiW. On the TiW there is similar, mirrored Au patterns on the flat (left) and etched (right) wafer.

The surface of a pull tested die from Au450, where the Au has been etched in KI, can be seen in figure 13.

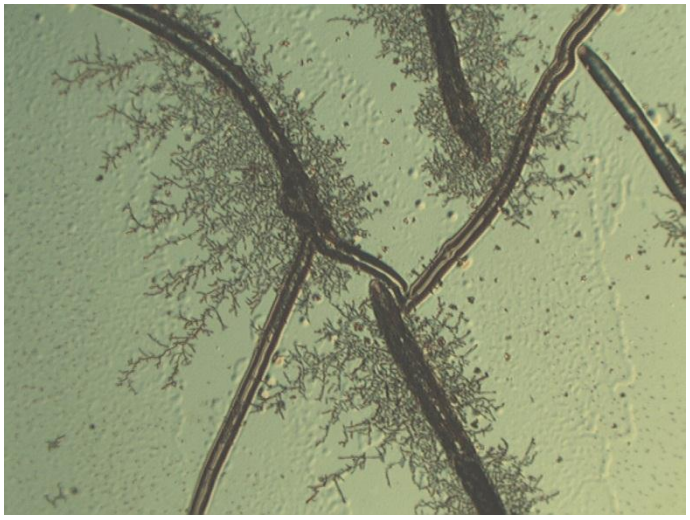

Figure 13. Micrograph of surface from die from Au450. The gold has been etched. A TiW surface with buckles surrounded by a eutectic pattern can be seen.

4 Discussion

The results in figure 3 show that the fracture force increased with increasing bonding temperature. The fracture force increased slightly when increasing the bonding temperature from 350 °C to 400 °C. Further increasing the bonding temperature to 450 °C increased the fracture force by almost 100%. However, the fracture force was not highly dependent on the bond frame area. Similar fracture forces were obtained for all four frame designs on each laminate. Hence, the calculated bond strength decreased with increasing frame width, as can be seen in figure 4 and table 3. All bond frames of widths 100 and 200 µm had average bond strengths larger than 19 MPa.

The bonding temperatures used in the current study are slightly higher than the 260 - 350 °C reported in previous studies [10, 17, 19]. The bonding times of the current study are similar to the times used in the previous studies. Both sputtered [12, 19, 20] and electroplated Au [10] has previously been used for bonding. The production volume and fab facility decides which method is preferable. It is difficult to compare the bonding pressures, since studies often present the pressure applied in the bonding tool without mentioning the actual bond area on the wafers. However, the applied bonding pressures used in the current study are probably lower than the pressures used by Tsau *et al.* [17] and higher than the pressure used by Taklo *et al.* [19]. The average bond strengths

obtained on our three laminates were higher than the ~10 MPa reported by Taklo *et al.* [19] and the ~ 20 MPa reported by Kurotaki *et al.* [16]. Mean fracture loads of 20 MPa have been reported for glass frit bonds [3], indicating that 20 MPa can be a sufficient bond strength for device seals in industrial products. All temperature and frame combinations, except frame type F400 from laminate Au350, are in the same range or higher than this criterion. However, for all such comparisons it must be kept in mind that these results are geometry dependent due to stress concentration effects. Studies of energy release rates might be more appropriate, but are less easily accessible as e.g. 4 point bending tests or similar methods are required. The shear strength of chips from Au400 and Au450 has been measured by Tollefsen *et al.* to be in agreement with earlier work [21]. The electrical resistance of laminate Au350 is reported elsewhere [22].

As can be seen in figure 5, the visual appearance of the gold outside the bond frame had changed after bonding. The amount of change increased with increasing bonding temperature. Laminate Au350 had only glossy gold, similar to the as-deposited material. Laminate Au450 had only matt gold. The gold surfaces from laminate Au400 were both glossy and matt. As seen in table 4, glossy gold had a surface roughness of 2 nm, while the surface roughness of matt gold on laminates Au400 and Au450 were 170 and 320 nm, respectively. From figure 7 it is clear that the higher surface roughness of the matt gold is due to larger grains. It is likely that both solidification of the eutectic Au-Si solder and grain growth through Ostwald ripening occurred in the Au film [23]. At 350 °C, such effects were negligible. The effects were significant at 400 °C, and very pronounced at 450 °C. This result is in agreement with the eutectic Au-Si temperature of 363 °C and the rule-of-thumb that metal recrystallization onsets at a temperature of the halved melting temperature, i.e.at 396 °C for Au. Figure 13 shows a pull tested die where the Au has been etched. It was possible to remove most of the gold. The pattern that is left around the buckles is most likely a Au-Si solder. The results from laminate Au400 in figure 7 indicate that there was a gradient in a parameter acting as driving force for the observed grain growth. Possible such parameters include pressure, temperature and concentration of Si in Au. Other parameters cannot be out-ruled.

A crack pattern can be seen around the bond frames in figure 5(c) and (d) and in figure 5. Figure 10 indicates that the cracks are due to buckling of the TiW film. Figure 6 shows that there was less adhesive fracture at the TiW-Si interface in the chips bonded at 400 and 450 °C than in chips bonded at 350 °C. We suggest that the occurrence of TiW buckling and the difference in fracture modes are related to film stress. The as-sputtered TiW-Au film incorporates a large stress. This stress is likely to have caused the delamination at the TiW-Si-interface on chips from laminate Au350. When bonding at 400 and 450 °C, the deformed structure of Au disappears and recrystallization and subsequent grain growth and Au-Si solidification take place. Stress relaxation is thought to occur by Au grain growth, which then allows TiW buckling under the transformed Au film. The results in figures 8 and 9 show that a high bond strength seems to be correlated to matt gold and low occurrence of adhesive TiW-Si fracture. Investigation of a possible causality, or an underlying common explanation, will be topic for further experiments and studies.

In the EDX analysis of the areas shown in the scanning electron micrographs in figures 7 and 10, there was no sign of interaction between the 200 nm thick TiW layer and Au or Si. This observation is in agreement with Baeri *et al.* reporting TiW to be stable at 450 °C [24], and indicates that TiW is a suitable adhesion/ diffusion barrier layer for gold thermocompression bonding. However, on the chips bonded at 450 °C, there was no Au left in the areas adjacent to some of the TiW buckles. Also, there was no Au left in the unbonded area adjacent to the bond frames on chips from laminate Au400 and Au450 (figures 7 and 10). We think that the TiW barrier layer has cracked in some of the buckles. In addition the TiW layer did not cover the walls of the protruding bond frames. In those areas, the Au could be in direct contact with the Si and rapidly diffuse into the Si. For temperatures above 363 °C, a eutectic reaction forming an Au-Si melt, can take place. It is likely that Au-Si alloys

have been formed in parts of the bond area on laminates Au 400 and Au450 resulting in a mixed mode of Au-Au thermocompression and Au-Si eutectic bonding. To avoid a reaction between Au and Si one should either keep the bonding temperature bellow 363 °C or use design rules that ensure that Au and Si are not in contact. This can be achieved by using overlapping masks for TiW and Au.

The fracture surfaces of the samples were different depending on bond temperature, see figure 6. All chips from laminate Au350 had some adhesive fracture at the TiW-Si interface, while only 13% of the chips from laminate Au450 had adhesive TiW-Si fracture. Cohesive fracture in the bulk silicon occurred on about 75% of the chips from all three laminates. The differences in fracture modes are probably related to the Au grain growth and stress relaxation of the TiW film. For a system with optimized adhesion layers cohesive fracture in the bulk of a ductile bonding layer is expected. The results from Au350 show that adhesion between TiW and Si could be further improved to increase the bond strength. The adhesion between TiW and Au seems to be acceptable.

In summary, buckling and rupture of the TiW barrier, the changes in the gold film and a eutectic Si-Au reaction seem to have caused areas without gold, both outside the bonding area and in the bonding frame (figures 10-12). This effect can prevent hermetic sealing if channels without gold are formed across the entire bond frame. The results indicate that bonding at 400 °C for 15 minutes applying 21 MPa across the bond structures may cause channels without gold across the bonding frame. For hermetic sealing, it is therefore recommended to use a temperature below the Au-Si eutectic of 363 °C.

5 Conclusions

Au-Au bonding for MEMS device sealing has been investigated on frames of outer dimensions 3×3 mm^2 and widths 100, 200, and 400 µm. The wafers were bonded at 350, 400 or 450 °C. All bond frames of widths 100 and 200 µm had average bond strengths larger than 19 MPa. The fracture force was not dependent on the frame width. However, the fracture force increased slightly when increasing the bond temperature from 350 to 400 °C, and by 99% when increasing the temperature further to 450 °C. For bonding temperatures of 400 and 450 °C, significant grain growth, Au-Si solidification, buckling of the TiW film, and stress relaxation in the TiW and Au films were observed. The grain growth was heavily dependent on the temperature. At 350 °C, negligible grain growth occurred in the bonding Au. The grain growth was significant at 400 °C, and very pronounced at 450 °C. In areas with holes in the TiW barrier, Si diffused into the Au at bond temperatures 400 and 450 °C, and it is likely that some Au-Si or silicide was formed. The grain growth and eutectic Si-Au reaction in laminates bonded at 400 and 450 °C resulted in a discontinuous Au film in the bonding seal. To avoid the observed temperature-induced effects in the metal system, Au-Au thermocompression bonding should be performed at temperatures below 400 °C when applying a TiW adhesion and barrier film. However, for a hermetic sealing it is recommended either to use design rules to avoid contact between Au and Si or to perform the process at a temperature below the Au-Si eutectic temperature at 363 °C.

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Wafer-level Au-Au bonding in the 350-450 °C temperature range

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