Open access • Proceedings Article • DOI:10.1109/ECTC.2004.1320376

Wafer-level integration of on-chip antennas and RF passives using high-resistivity polysilicon substrate technology — Source link

Paulo Mendes, S.M. Sinaga, A. Polyakov, M. Bartek ...+2 more authors

Institutions: Delft University of Technology

Published on: 01 Jun 2004 - Electronic Components and Technology Conference

Topics: Polycrystalline silicon, Silicon, Wafer-scale integration, Substrate (electronics) and Q factor

Wafer-Level Integration of On-Chip Antennas and RF Passives Using High-Resistivity Polysilicon Substrate Technology

P.M. Mendes[1,2], S. Sinaga[1], A. Polyakov[1], M. Bartek[1], J.N. Burghartz[1], J.H. Correia[2],
[1]Lab. of ECTM/DIMES, Delft University of Technology
[2]Dept. of Industrial Electronics, University of Minho,
Campus de Azurém, 4800-058 Guimarães, Portugal
Tel.: +351-253510382, Fax: +351-253-510189,
e-mail: paulo.mendes@dei.uminho.pt

Abstract

High-resistivity polycrystalline silicon (HRPS) wafers are utilized as low-loss substrates for three-dimensional integration of on-chip antennas and RF passive components (e.g. large inductors) in wafer-level chip-scale packages (WLCSP). Sandwiching of HRPS and silicon wafers enables to integrate large RF passives with a spacing of >150 μm to the conductive silicon substrate containing the circuitry, while providing mechanical stability, reducing form factor and avoiding any additional RF loss. Antenna performance comparable to glass substrates and high quality factors for large spiral inductors (Q=11 at 1 GHz; 34 nH) are demonstrated. The HRPS substrates have high dielectric constant, low RF loss, high thermal conductivity, perfect thermal matching, and processing similar to singlecrystalline silicon.

Introduction

Wireless multi-hop networks are promoted as a new concept of unobtrusive monitoring and communication [1]. In spite of promising demonstrations made at system level [2]-[3], it is still a long way from the presently realized fist-size wireless sensor nodes to the ultimately desired form factor of a few mm^3 for such microsystems. Such devices require, first of all, operation at extremely low power levels and thus passive components of very high quality. Spiral inductors and on-chip antennas, in particular, should be integrated on an ideal radio-frequency (RF) substrate and be spaced sufficiently far away from the conductive silicon sections containing the active circuitry [4]-[5]. An ideal substrate for RF and microwave passives has very high resistivity throughout, a high thermal conductivity, a high dielectric constant and low polarization losses [6]. High-resistivity silicon (HRS) meets most of those requirements but is prone to losses caused by surface channels and is comparably expensive because it is based on sophisticated float-zone crystallization of polysilicon rods.

Silicon material with resistivities up to 10 kΩ-cm is made by float-zone processing of undoped polysilicon rods. High-resistivity polycrystalline silicon (HRPS) wafers can be fabricated directly from the polysilicon rods, thus eliminating the expensive float-zone process.

Application of wafer-level chip-scale packaging (WLCSP) techniques like adhesive wafer bonding and through-wafer electrical via formation, combined with the selected radio frequency (RF) structures allows a new level of on-chip integration [7]-[8]. These new techniques made possible the integration of new materials together with the standard materials already used for integrated circuits fabrication. Bonding of a low-loss HRPS substrate to a core RF silicon wafer followed by wafer-to-wafer electrical interconnect formation enables realization of a variety of novel RF structures (high-Q passives, transmission lines, suspended ground planes, integrated antennas, on-chip shielding, etc.) and represents a truly added value to the concept of wafer-level chip-scale packaging. When compared to other solutions, like glass or thick polymer layers (e.g. BCB, polyimide), higher thermal conductivity and easier processability makes HRPS a very interesting option.

Fig.1 illustrates the concept, where wafer-level chip-scale packaging is used to stack HRPS substrate on top of a RF silicon process and to integrate high-quality passive devices.

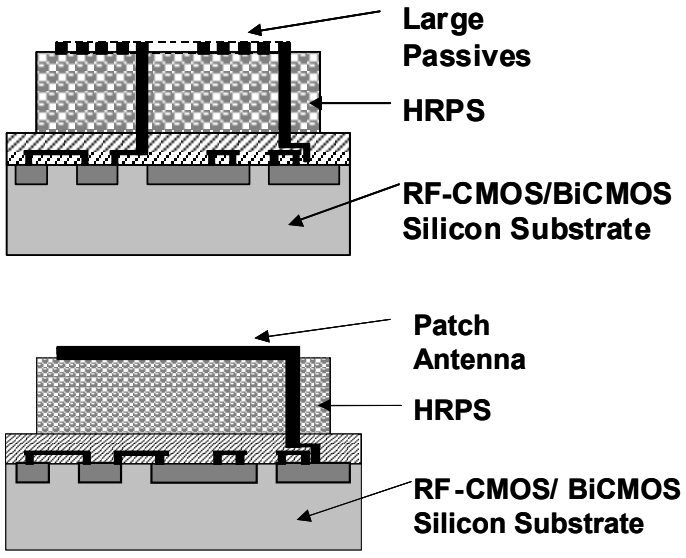


Figure 1: HRPS used as a spacer in WLCSP for integration of high-Q passives (top) and on-chip antennas (bottom).

The structure shown schematically in Fig. 1 benefits from very good thermal and mechanical matching between the core-process wafer and the HRPS spacer.

In this work, the HRPS spacer technology is introduced and the HRPS material is electrically characterized using measurements on CPW's. Next to that, application to on-chip patch folded-patch antennas, and spiral inductors is demonstrated. The HRPS performance is compared to devices on glass substrates (Schott AF45 and Pyrex #7740).

High-Resistivity Polycrystalline Silicon Characterization

Several different methods can be used to extract the electrical intrinsic properties of a material [9]. From the most widely used techniques in the microwave region, the transmission line technique is the simplest method for electromagnetic characterization in wideband frequencies [10]. The S-parameters measurements of a planar test cell can be used to obtain the desired parameters. Both microstrip and CPW can be used as test cell [11]. In this work, the electrical properties of HRPS were obtained from S-parameters measurements performed on CPW lines. Those values were used to extract the losses in dB/mm, the electrical permittivity and the loss tangent (or conductivity) [8]. Fig. 2 shows the CPW cell configuration used to measure the S-parameters used in the extraction method.

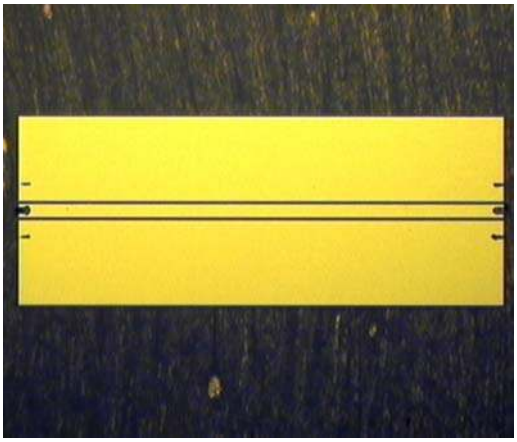


Figure 2: Photograph of the CPW cells used in substrate material characterization.

The CPW cells were fabricated directly on top of the HRPS substrate. The metal layers were fabricated with 2 μm of aluminum on top of the wafer under characterization. Since the exact electrical permittivity value at the desired frequencies was not known, different CPW cells were designed in order to obtain a suitable configuration for the material properties extraction. It is recommended the use of some mismatch in order to obtain a good accuracy [12]. In this way, the CPW cells were designed with different *W/S* ratios in order to obtain different characteristic impedances. Namely, lines with the following dimensions were used: CPW 1 - (W = 75 μm, S = 50 μm), CPW 2 - (W = 100 μm, S = 15 μm), and CPW 3 -(W = 75 μm, S = 15 μm).

All measurements performed on CPW cells were made on-wafer. First, two-port calibration was applied and then the necessary S-parameters were measured. The obtained characteristic impedance related to the CPW cells used is presented in Fig. 3.

As the characteristic impedance, the electrical permittivity was also obtained from the measured S-parameters and is displayed in Fig. 4. This plot shows the results obtained from the three different CPW cells. As can be observed in that figure, for high frequencies, and as expected, the electrical properties show only a slight variation with frequency. Also, we can observe an abrupt change on the measured characteristics at low frequencies. This happens because at those frequencies the assumptions behind the theoretical formulation are not anymore valid. At the frequencies of interest (5-6 GHz), the obtained dielectric constant is $\varepsilon_r \approx 11.5$.

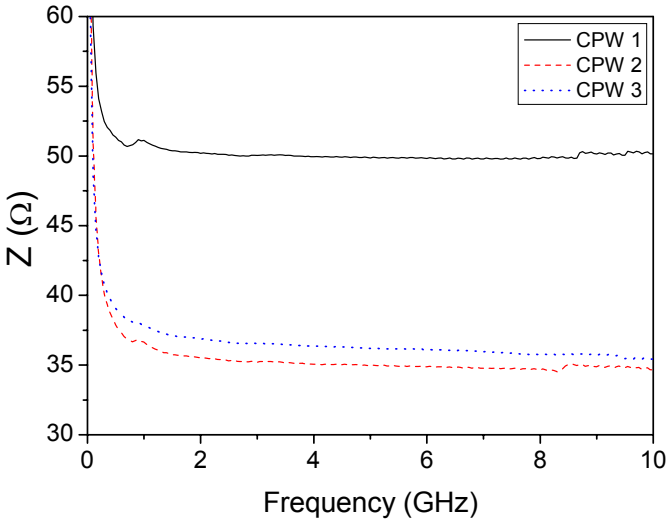


Figure 3: Measured characteristic impedance of the CPW cells.

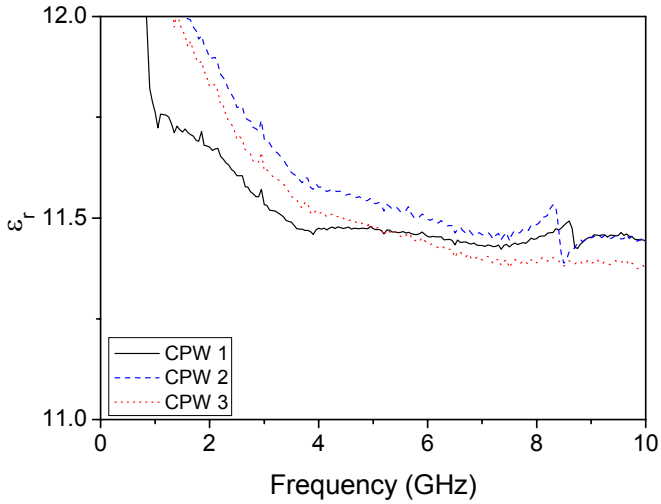


Figure 4: Extracted dielectric constant for three different CPW cells.

Together with dielectric constant, loss tangent is also a fundamental parameter as it represents the performance achievable with the designed passives. The results obtained for loss tangent are plotted in Fig. 5. As expected, all the CPW lines show similar values since the substrate is always the same.

The method used to obtain the data in Fig. 5 is based on the measured total losses coming from the CPW lines. Then, assuming no radiation losses, it is possible to identify the metal losses and substrate losses. In this way, it is important to refer that the obtained values for loss tangent are heavily dependent on the models used to describe the losses in these kinds of transmission lines.

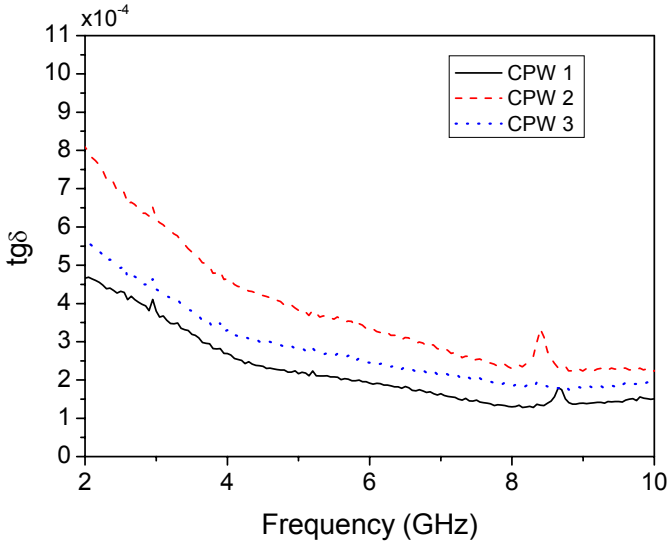


Figure 5: Extracted loss tangent for three different CPW cells.

Application of HRPS in Wafer-Level Packaging

The possibility to integrate on-chip antennas and RF passives is highly dependent on the achievable device dimensions and efficiency. Reduction of dimensions and efficiency improvement can be obtained through proper device geometry. However, substrate losses have a big impact in the achievable efficiency/losses. To evaluate how much, a patch antenna and an inductor were fabricated on top of an HRPS wafer. Also, using the obtained HRPS electrical parameters and HFSS 3D electromagnetic simulation tool, an analysis was conducted for a shorted-folded patch antenna.

On-chip antennas using HRPS

The patch antenna was built on top of an HRPS wafer, without any insulating layer between the metal patch and the substrate. The design was made with HFSS FEM tool. The antenna was designed to operate in the 5-6 GHz ISM band, which yields antenna dimensions of 7.7x7.6 mm^2. The patch metal layer was made with 2 μm of sputtered aluminum and the feeding was realized through a microstrip line.

For a measurement purpose, the antenna die was placed on top of a PCB substrate and the feeding microstrip line was connected to a SMA connector. The fabricated antenna prototype is shown in Fig. 6.

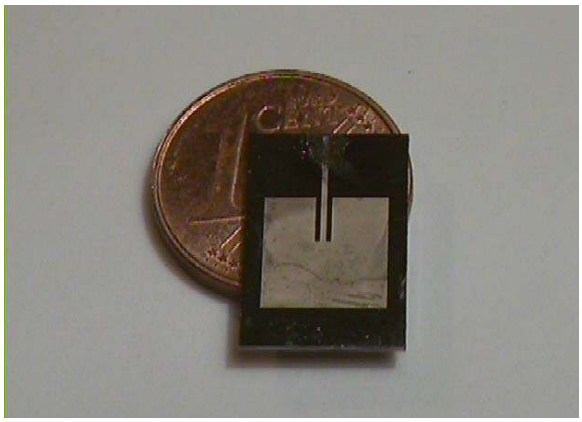


Figure 6: Patch antenna prototype fabricated on HRPS.

All the measurements were performed using the HP 8510 vector network analyzer, which was previously calibrated with one-port calibration. The antenna efficiency was measured using the Wheeler cap method [13]. This method is based on the measurements of the antenna input return loss when it is radiating or not radiating. The last condition is usually met with a metallic cap enclosing the antenna under test. With those measurements the efficiency can be easily computed. The antenna efficiency was also obtained from simulations and compared with the measured values.

The measured values used in the Wheeler cap method are plotted in Fig. 7. The figure shows measured values when the antenna is radiating and when it is not. Using the data from measurements, it was obtained an efficiency of 25.6 %, which is in good agreement with the value computed by HFSS, that was 28.6 %.

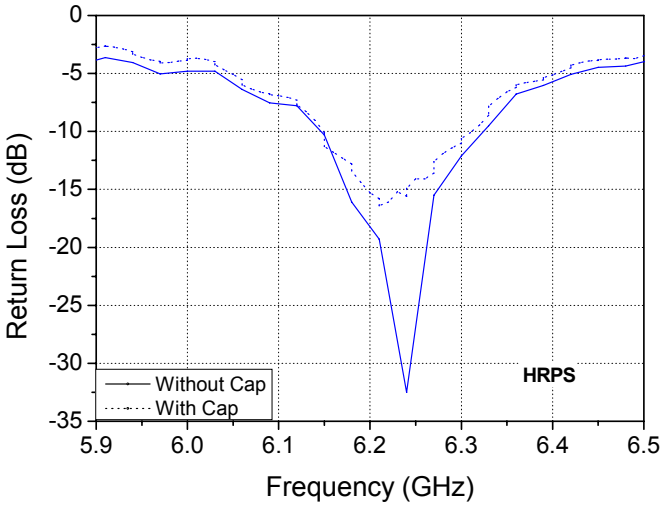


Figure 7: Measured return loss versus frequency used to obtain the operating frequency, bandwidth and efficiency.

It was also verified that this antenna has an operating frequency of 6.25 GHz, with a –10 dB return loss bandwidth of ~200 MHz.

For comparison, a similar patch antenna was fabricated on a Pyrex #7740 wafer. Similarly, 2 μm of sputtered aluminum were used to obtain the metal patch layer. Such antenna has a measured operating frequency of 5.995 GHZ and the -10 dB return loss bandwidth is ≈100 MHz. From the measurements we obtained an efficiency of 51%, which is higher than the obtained with HRPS. The drawback is the increase in the antenna size.

Since the patch antennas are rather large for on-chip integration, the use of HRPS to fabricate a shorted-folded patch antenna was also considered. The cross-section of such antenna is displayed in Fig. 8.

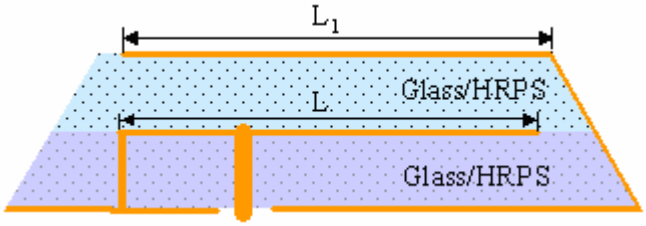


Figure 8: Cross-section of a shorted-folded patch antenna.

This type of configuration allows a reduction in antenna dimension and increase in efficiency with the added cost of fabrication complexity. With this type of antenna following material combinations can be formed: glass/glass, HRPS/HRPS, or glass/HRPS. An option to avoid the difficult task of doing through-wafer vias in glass could be to replace the glass wafers by HRPS. This will inevitably increase a bit the dielectric losses, but at the same time the antenna dimensions could be reduced. Other option is to substitute only the bottom glass wafer by HRPS. In this way, the vias in glass are not required and the overall losses are expected to be smaller.

All the proposed options were analyzed based on a FEM model built using HFSS. Considering a 10 kΩ-cm substrate, the predicted results are summarized in Table 1. For various substrate options, the dimensions of the antenna model were kept constant as possible, only some minor adjustments were implemented to adjust the operating frequency and/or to achieve impedance matching.

Table 1: Summary for the different stack options.
Parameters shown: F_c – operating frequency, BW – bandwidth, Eff. - efficiency, L_1 - top patch length, L - middle patch length.

	glass/glass	HRPS/HRPS	HRPS/glass
F_c	5.66 GHz	5.66 GHz	5.64 GHz
BW	60 MHz	57 MHz	63 MHz
Eff.	66 %	64 %	65 %
L_1	3.2 mm	1.8 mm	3.2 mm
L	2.6 mm	1.65 mm	2.3 mm

As can be seen from Table 1, the antenna built on a stack of two glass wafers has the highest efficiency and the largest dimensions. The antenna on a stack of two HRPS wafers is the smallest and has the lowest efficiency. When the glass/HRPS stack is used, a compromise can be obtained. The losses are slightly increased and the dimensions don't change significantly. The antenna dimensions are strongly dependent on the projected efficiency and bandwidth and also on the substrate thickness [14] but, if we use HRPS/HRPS, they can fit inside an area of 3x3 mm^2. The achievable –10 dB return loss bandwidth is around 50 MHz (+/- 10 MHz).

The use of a 10 kΩ-cm HRPS wafer makes on-chip antenna integration possible with an antenna efficiency and electrical performance similar to the one obtained with glass [14]-[15], but with the benefit of a smaller size (12.4x11.7 vs. 7.7x7.6 mm2 for patch antenna and 4x4 vs. 3x3 mm2 for folded-patch antenna at 5.7 GHz) since the dielectric constant is two times higher for HRPS. Next to that, the inherent problems associated with glass substrate processing (e.g. difficulty to form high-aspect ratio vias) are avoided.

Integrated RF passives

Inductors and transmission lines are fundamental passive components needed for RF circuit design and need to be investigated.

The transmission line losses were computed from the same CPW lines that were used to characterize the HRPS substrate and compared to the values obtained when glass wafers are used. The total attenuation measured in the CPW transmission lines fabricated with the HRPS substrate is plotted in Fig. 9.

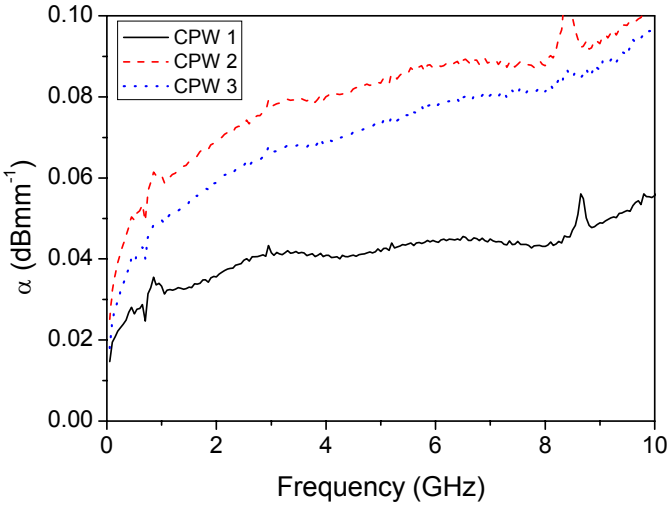


Figure 9: Measured return loss for three different CPW cells.

For comparison, the losses obtained with different types of glass wafers were also characterized and compared with the losses obtained with HRPS wafers. The obtained results are plotted in Fig. 10.

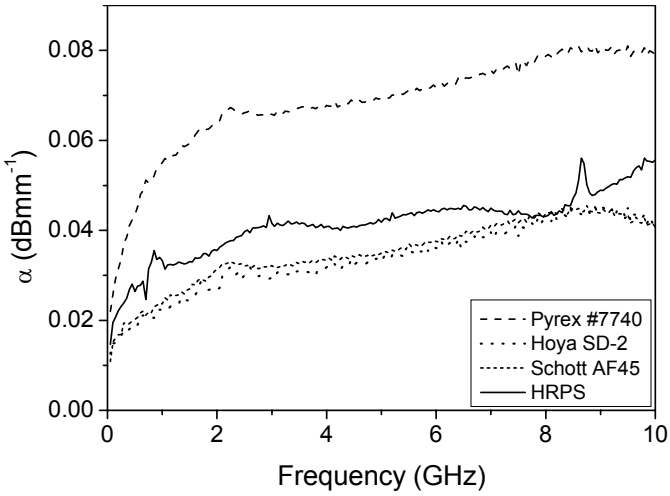


Figure 10: Losses for the different substrate types for a CPW cell with W = 75 μm and S = 50 μm.

Compared to Pyrex #7740 (α=0.7 dB/cm) and Schott AF45 (α=0.38 dB/cm), a comparably low loss figure was measured for CPW's on HRPS (α=0.44 dB/cm) at 6 GHz.

Last but not least, the performance of RF inductors was also investigated. During the past decade, the spiral inductor has established as a standard passive component in the high-frequency silicon technologies [16]. When implemented directly in a planar silicon technology, the spiral inductor suffers considerably from substrate losses, which limits the achievable quality factor Q. Moreover, the spiral inductor consumes excessively the chip area, which makes it a rather costly component, especially when higher inductance values (L > 5 nH) are required. Solution to this problem can be found by placing the spiral inductor above or underneath the active circuitry. By using a high-resistivity substrate and sufficient

separation, the achievable Q factor will not be degraded (see Fig. 11).

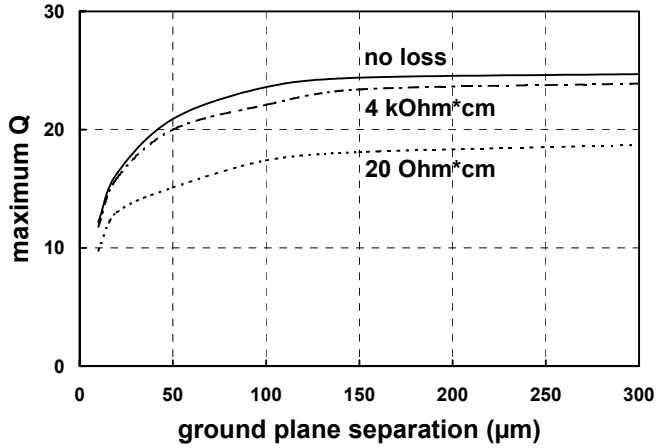
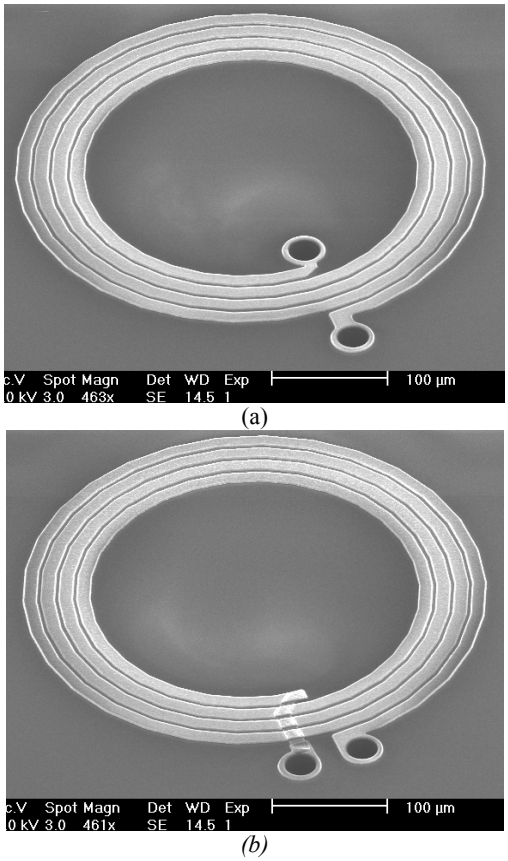


Figure 11: Quality factor of a 17-nH spiral inductor (in 4-µm Al metallisation) vs. the separation of a metal ground plane for three different substrate resistivities.

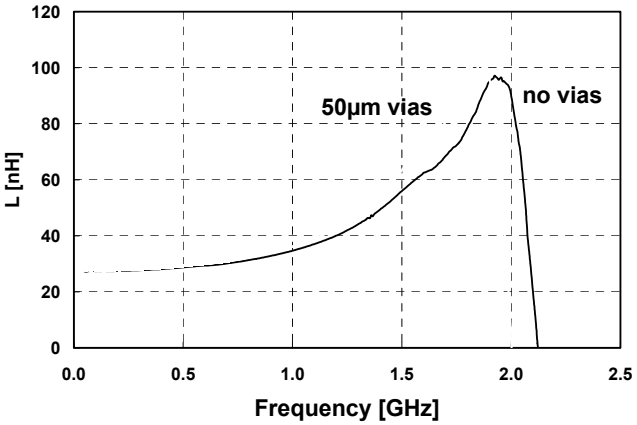
To demonstrate this concept, large spiral inductors (up to 34 nH) were realized on a high-resistivity polysilicon with and without 1µm thick PECVD oxide isolation layer (Fig. 12). A quality factor Q>10 at 1 GHz was measured for a very large 34-nH coil (A=820x820 µm^2) as shown in Fig. 13.



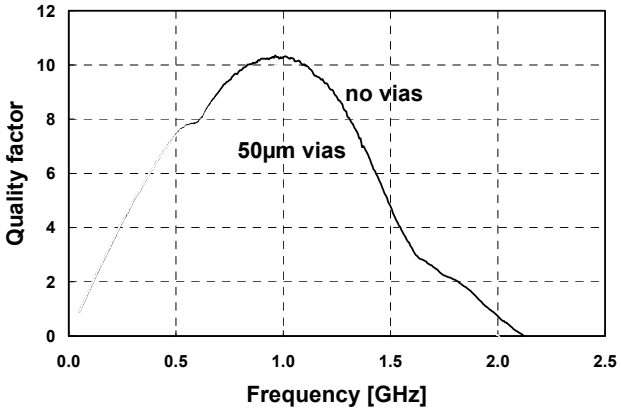
(a)

(b)

Figure 12: SEM photographs of a spiral inductor on high-resistivity polysilicon (HRPS) with via connections through the HPRS substrate without (a) and with (b) underpass.



(a)



(b)

Figure 13: Inductance and quality factor (Q) of a 34 nH inductor on HPRS with and without through-substrate vias.

It was particularly remarkable that the CPW's and inductors were also functional without any dielectric isolation layer (α=0.9 dB/cm at 6 GHz; Q=7.5 for 34 nH coil).

From all the presented information we have found that HRPS exhibits clear advantages over the glass substrates, if one considers that the dielectric constant is about two times larger (ε=11.7 vs. 4.8-6.2), which allows smaller structures, and nearly independent on frequency, that the thermal conductivity is more than 100-times larger, and that the thermal expansion coefficient is perfectly matched to silicon so that mechanical stress in a HRPS/Si sandwich is minimum.

Conclusions

In conclusion, HRPS is presented and demonstrated as a new material for 3D-integration of RF systems in silicon technology. HRPS provides a low RF loss, a high dielectric constant, a high thermal conductivity, good mechanical properties, and a perfect match to the integrated circuit silicon substrate in thermal expansion coefficient. Last but not least, the fabrication technology know-how available for standard single-crystalline Si substrates is directly applicable to processing of HRPS.

Acknowledgments

The authors wish to acknowledge the support by Philips Semiconductors and Philips Research in the context of the Philips Associate Centre at DIMES (PACD); the Portuguese Foundation for Science and Technology (SFRH/BD/4717/ 2001, POCTI / ESE / 38468 / 2001, FEDER), and the EC (project Blue Whale IST-2000-10036). Dr. Manfred Grundner and Wacker Siltronic are acknowledged for supplying polysilicon rod material. Bernd Lux from the Institute of Crystal Growth (IKZ), Berlin, Germany is acknowledged for arranging the wafer dicing and polishing.

References

1. M. Weiser, "The computer for the 21st century," Scientific American, Vol. 265, No. 3, 1991, pp. 94-100.
2. J. Rabaey, "Ultra low-energy transceivers for wireless sensor networks," Proc. 15th Symposium on Integrated Circuits and Systems Design, Porto Allegre, Brazil, September 2002, p. 386.
3. A. Chandrakasan, R. Min, M. Bhardwaj, S.-H. Cho, A. Wang, "Power Aware Wireless Microsensor Systems," ESSCIRC, Florence, Italy, September 2002.
4. J. B. Yoon, C. H. Han, E. Yoon , and C. K. Kim, "Monolithic High-Q Overhang Inductors Fabricated on Silicon and Glass Substrates," Dig. IEDM, Washington DC, USA, 1999, pp. 753-756.
5. K.T. Ng, N.P. Pham, P.M. Sarro, B. Rejaei, J.N. Burghartz, "Characterization of a Bulk-Micromachined Post-Process Module for Silicon RF Technology," IEEE topical meeting on Silicon Monolithic integrated Circuits in RF systems, April 26-28, 2000, pp. 99-102.
6. J.N. Burghartz, M. Bartek, B. Rejaei, P.M. Sarro, A. Polyakov, N.P. Pham, E. Boullaard, K.T. Ng, "Substrate Options and Add-On Process Modules for Monolithic RF Silicon Technology," Proc. BCTM 2002, Monterey, CA, Sept. 29 - Oct. 1, 2002, pp. 17-23.
7. P. M. Mendes, A. Polyakov, M. Bartek, J. N. Burghartz, J. H. Correia, "Integrated 5.7 GHz Chip-Size Antenna for Wireless Sensor Networks," Transducers'03, Boston, USA, June 8-12, 2003, pp. 49-52.
8. A. Polyakov, P.M. Mendes, S.M. Sinaga, M. Bartek, B. Rejaei, J.H. Correia, J.N. Burghartz, "Processability and Electrical Characteristics of Glass Substrates for RF Wafer-Level Chip-Scale Packages," Proc. ECTC 2003, New Orleans, USA, May 27-30, 2003, pp. 875-880.
9. Hewlett Packard, "Basics of measuring the dielectric properties of materials", Application Note 1217-1.
10. J. Hinojosa, "S-Parameter Broadband Measurements On-Coplanar and Fast Extraction of the Substrate Intrinsic Properties," IEEE Microwave and Wireless Comp. Letters, Vol. 11, Nº 2, 2001, pp. 80-82.
11. J. Hinojosa, K. Lmimouni, G. Dambrine, "Fast Electromagnetic Characterization Method of Thin Planar Materials Using Coplanar Line up to V-band," Electron. Lett., Vol. 38, Nº 8, 2002, pp. 373-374.
12. J. Hinojosa Jimenez, "Contribuition a l'Elaboration d'une Nouvelle Methode de Caracterisation Electromagnetique de Materiaux a Partir de Lignes Plaquees – Applications a l'Etude de Nouveaux Materiaux," Univ. Sciences et Technologie de Lille, France, Ph.D. Thesis, May 1995.
13. Edward H. Newman, Peter Bohley, C. H. Walter, "Two Methods for the Measurement of Antenna Efficiency," IEEE Trans. Ant. Prop., Vol. 23, Nº 4, 1975, pp. 457-461.
14. P.M. Mendes, A. Polyakov, M. Bartek, J.N. Burghartz, J. H. Correia, "Design of a Folded-Patch Chip-Size Antenna for Short-Range Communications," European Microwave Conference 2003, Munich, Germany, 7-10 October 2003, pp. 723-726.
15. P.M. Mendes, M. Bartek, J.N. Burghartz, J.H. Correia, "Design and Analysis of a 6 GHz Chip Antenna on Glass Substrates for Integration with RF/Wireless Microsystems," Proc. 2003 IEEE AP-S, Vol. 2, Columbus, June 22-27, 2003, pp. 667-670.
16. J.N. Burghartz, B. Rejaei; "On the Design of RF Spiral Inductors on Silicon", IEEE Transactions on Electron Devices, Vol. 50, No. 3, 2003, pp. 718-729.