Wafer-Level Parylene Packaging With Integrated RF Electronics for Wireless Retinal Prostheses

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***Abstract*—This paper presents an embedded chip integration technology that incorporates silicon housings and flexible Parylene-based microelectromechanical systems (MEMS) devices. Accelerated-lifetime soak testing is performed in saline at elevated temperatures to study the packaging performance of Parylene C thin films. Experimental results show that the silicon chip under test is well protected by Parylene, and the lifetime of Parylene-coated metal at body temperature (37 °C) is more than 60 years, indicating that Parylene C is an excellent structural and packaging material for biomedical applications. To demonstrate the proposed packaging technology, a flexible MEMS radio-frequency (RF) coil has been integrated with an RF identification (RFID) circuit die. The coil has an inductance of 16 μH with two layers of metal completely encapsulated in Parylene C, which is microfabricated using a Parylene–metal–Parylene thin-film technology. The chip is a commercially available read-only RFID chip with a typical operating frequency of 125 kHz. The functionality of the embedded chip has been tested using an RFID reader module in both air and saline, demonstrating successful power and data transmission through the MEMS coil. [2010-0008]**

***Index Terms*—Accelerated-lifetime soak testing (ALST), chip packaging, Parylene C, radio-frequency (RF) coil.**

I. Introduction

WIRELESS retinal prostheses employ electronic systems to partially restore the lost visual function of blind patients due to diseases, such as retinitis pigmentosa and age-related macular degeneration. In particular, an epiretinal approach has been developed by implanting high-density electrodes on the inner retinal surface to electrically activate remaining nerve cells [1]–[3]. For such systems that involve completely intraocular implantation, there is a need for chip integration and packaging technologies that are capable of high-lead-count interconnections while ensuring system biocompatibility, flexibility, and long-term reliability [4]. Traditional integration methods use soldering, wire bonding, flip chip, and tape-automated bonding to form interconnections between discrete components [5]. They are labor intensive, inefficient, and costly, limiting the achievable integration density. In addition, because the bonding materials used in these technologies are generally not biocompatible, extra protection layers would be required for biomedical applications. Butler *et al.* [6] developed a multichip module packaging process, by which microelectromechanical systems (MEMS) devices can be integrated with complementary metal–oxide–semiconductor (CMOS) electronic dies using the "chip first" General Electric high-density interconnect technology. Although this technology bypasses many issues with traditional interconnecting methods, its lack of flexibility and biocompatibility remains a problem unsolved. In recent years, much effort has been placed on the development of advanced packaging methods for bioimplant systems using polymers or glass [7]–[9]. For example, a microflex interconnection technology has been demonstrated [8] by bonding individual components on a predefined flexible polyimide substrate. While devices packaged with this technology are flexible enough, their long-term biocompatibility has not been proven. The process is also tedious and costly for the integration of high-electrode-density devices. Harpster *et al.* [9] demonstrated the long-term hermeticity of glass-silicon implantable packages, but these packages are too rigid for retinal prostheses.

To overcome the challenges encountered in current technologies, we developed a chip-level integrated interconnect packaging method [10] that enables the integration of CMOS integrated circuit (IC) chips and prosthetic electrodes [11], and have now extended it to an embedded chip integration technology that can readily incorporate multiple monolithic chips in silicon housings and functional Parylene-based MEMS devices (e.g., MEMS coil) [12] to achieve high-level system functionalities. In this new approach, chip-to-packaging interconnections are established using standard microfabrication techniques, such as photolithography and metal etching; therefore, no wire bonding, bump bonding, or soldering is needed. In addition, the interconnect density is limited only by photolithography resolution and microfabrication tolerance, which offers the possibility to achieve high-lead-count (> 1000) integration. Finally, the favorable mechanical and chemical properties of Parylene C [13] allow our final devices to be highly flexible and biocompatible. Other advantageous properties of Parylene C include its transparency and conformal pinhole-free deposition

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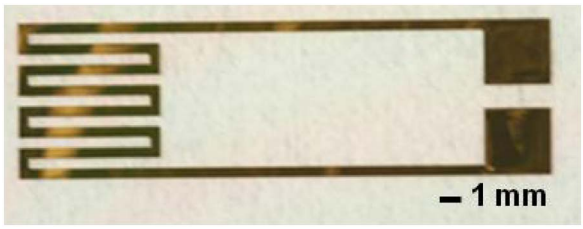

Fig. 1. Fabricated thin-film resistor with pure gold metallization and Parylene C packaging.

in a room-temperature chamber, allowing our packaging technology to be post-IC compatible.

II. Parylene-C Packaging Behavior

Parylene C is known to have lower water and gas permeability compared with two other commonly used polymers, namely, polydimethylsiloxane and polyimide [14]. However, human body fluid, fairly well approximated by an oxygenated saline solution with a salt content of about 0.9% at $pH \sim 7.4$ and 37 ± 1 °C [15], is very corrosive for metal and electronic circuits. The long-term stability and reliability of Parylene C packaging in liquid environments have not been fully understood yet and therefore deserve further investigation prior to in-depth technology development. In this paper, we have studied Parylene packaging behaviors through accelerated-lifetime soak testing (ALST) in hot saline (0.9% NaCl solution), which is a close imitator of body fluid. Two major structures used in the system integration, namely, Parylene-coated metal and Parylene-coated circuitry, have been tested, as discussed in the following sections.

A. Parylene-Protected Metal

To study the lifetime of Parylene-protected metal, thin-film resistors consisting of Parylene-C-coated gold wires are designed as test structures [16], [17]. Samples are microfabricated using a Parylene–metal–Parylene thin-film technology [18], starting with Parylene C vapor deposition (PDS 2120 system, Special Coating Systems, Indianapolis, IN) on a standard 4-in silicon wafer. After that, a 200-nm layer of gold is deposited in an e-beam evaporator (SE600 RAP, CHA Industries, Fremont, CA), followed by metal wet etching with photoresist as a mask. After the photoresist mask is removed, Parylene deposition is performed again to seal the metal structure. Then, photoresist is spun and patterned to expose contact pads, as well as to define the device shape. Finally, unwanted Parylene C is removed using oxygen plasma in a reactive ion etch (RIE) system (Semi Group Inc. T1000 TP/CC), and devices are then released from the substrate in a water bath. Fig. 1 shows an example of fabricated devices that have the same metal linewidth and edge space width of 500 μm. Prior to soak testing, all fabricated samples are treated in a vacuum oven with nitrogen backfill at 200 °C for two days. It has been experimentally demonstrated that this thermal treatment can enhance the adhesion of Parylene/Parylene interface and also lower the water permeation of Parylene thin film [17], [19].

TABLE I
Soak Testing Results of Parylene-Protected Metal Under Both Passive and Active Conditions

Testing Condition	Thickness of Parylene Coating (μm)	MTTF	
		77 °C	90 °C
Passive	4.7	> 250 days	~ 70 days
Active	4.7	N/A	< 2 days
	9.2	N/A	~ 62 days

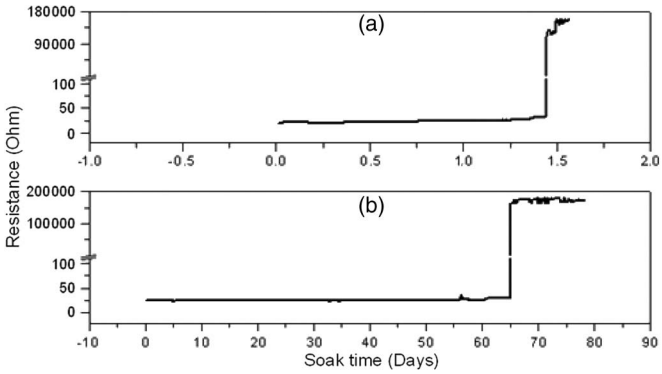

Fig. 2. Typical aging curve of tested samples under active conditions. (a) Sample with 4.7-μm Parylene coating failed after less than two days of soaking. (b) Sample with 9.2-μm Parylene coating can withstand long-term soaking of approximately 60 days.

The process typically takes effect at temperatures of over 180 °C, below which Parylene delamination occurs after only one day of soaking, indicating that no significant improvement is achieved. It is of note that the process temperature must be lower than the melting temperature of Parylene C (290 °C), as strong recrystallization of Parylene can happen beyond this point [20], [21], resulting in brittle polymer films.

The samples are tested under accelerated conditions both passively and actively. In the passive soak testing, devices are immersed in saline at elevated temperatures and then removed daily from the oven in order to monitor for failures under an optical microscope. The active soak testing is conducted in a simplified electrochemical setup that consists of a platinum wire as a reference electrode and the tested sample as a working electrode. During the experiments, the reference electrode is grounded, and a square wave with a magnitude of 6 V and a frequency of 50 Hz is continuously applied on the working electrode to create a potential difference between the two electrodes in saline. The test unit is then heated in a convection oven, and the dc resistance of the thin-film resistor is recorded every 10 min using an HP 4145 B semiconductor parameter analyzer (HP/Agilent Technologies Inc., Santa Clara, CA) controlled by a LabView program (National Instruments, Austin, TX). Five samples are tested under each condition, and their mean times to failure (MTTFs) are recorded when failures are observed, as summarized in Table I. In the passive mode, sample failures are considered as uniform water bubbles or delaminations at the interface of Parylene/Parylene or Parylene/metal. While in the active mode, we define sample failures as soaking time points when resistance increases significantly, usually by over three orders of magnitude of the original value (Fig. 2).

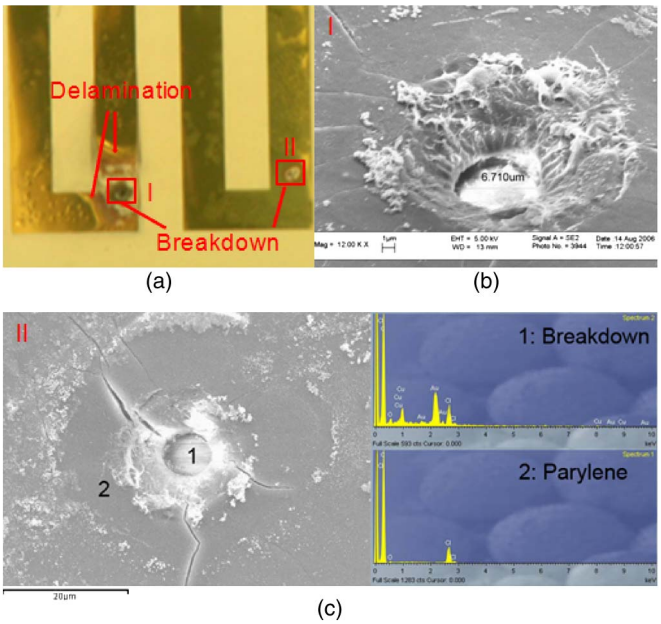

Fig. 3. (a) Parylene breakdowns occur in a 4.7-μm Parylene-coated sample, and delaminations are observed surrounding the breakdown area. (b) SEM image showing a crater-shape breakdown hole. (c) SEM images and EDS spectra on another failed area. Exposed gold element is detected inside the breakdown hole, indicating that a through hole is formed.

The passive soak tests are carried out at both 77 °C and 90 °C, so that the MTTF at body temperature can be extrapolated using an Arrhenius relation in (1) [22]

$$MTTF = A \exp\left(-\frac{E_a}{kT}\right) \tag{1}$$

where A is the pre-exponential constant, E_a is the activation energy, T is the temperature in Kelvin, and k is the Boltzmann's constant. Based on the data in Table I, an activation energy of approximately -1.07 eV and an A of around 9×10^{-14} can be calculated for Parylene-protected metal, resulting in an MTTF of over 67 years at a body temperature of 37 °C.

Samples with two different thicknesses of Parylene coating are tested under the active condition. Parylene breakdowns occur in samples with 4.7-μm Parylene coating after a short period of soaking, followed by Parylene delaminations expanding gradually from the breakdown areas. The breakdown regions (Fig. 3) are analyzed using scanning electron microscopy (SEM) and energy-dispersive X-ray spectroscopy (EDS) (LEO 1550VP Field Emission SEM—Oxford EDS). The EDS spectra confirm that the Parylene is locally melted into a through hole over the metal and the embedded metal is exposed. Parylene cracks radiate from the breakdown hole, which is mainly caused by thermal stress. It is also noted that the breakdown only appears on one side of the sample, while the other side remains intact, indicating that the failure is initiated either at the interface of Parylene/metal or inside the Parylene film.

Although the mechanism of Parylene breakdown is not completely clear, it is possible that the failures are initiated from certain areas where large defects and particles reside. Electrochemical reactions are accelerated at these areas due to high electric field concentrations and the direct exposure of metal

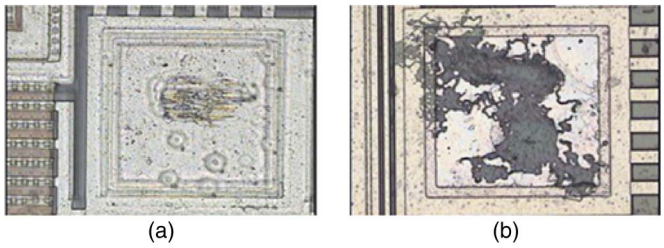

Fig. 4. Microscope images of chip metal pads on (a) a chip with Parylene coating after six months of soaking and (b) a bare chip without Parylene coating after two days of soaking.

to the saline, resulting in local metal corrosion. The circular shape of breakdown crater is mainly confined by the shape of exposed metal [23], which is similar to the size of particles. In samples coated with 9.2-μm Parylene C, without seeing Parylene breakdown, water bubbles are observed uniformly across the metal–Parylene interface. It is possible that thicker Parylene films may conformally coat particles and thus can prevent the unwanted particle-induced breakdown. The thickness of polymer films should be carefully selected in order to cover the majority of defects and particles while not compromising the flexibility of polymer package. Preliminary results suggest that flexible films with a thickness of approximately 10 μm could cover most defects or particles generated under our cleanroom conditions (Class 1000).

B. Parylene-Protected Chip

Similar ALSTs are performed using Parylene-coated IC chips. A die-form passive read-only radio-frequency identification (RFID) chip (EM 4100, EM Microelectronic, Switzerland) is selected as a test chip. This chip is a CMOS IC with exposed contact pads made of layered Al–Ni–Au metals. It can be powered with a pair of coils through an electromagnetic field. By turning the modulation current on and off, the chip sends back a 64-b sequence stored in the memory array, which can be detected with an oscilloscope. The operation frequency of the chip is between 100 and 150 kHz, with 125 kHz being typical.

Unpowered soak testing is performed in saline at 77 °C. Prior to soaking, RFID chips are cleaned with isopropanol and deionized water, and then completely coated with approximately 10-μm Parylene C. During the soaking period, the samples are examined daily under a microscope. The soak lasts up to six months, and the samples are removed from saline for functionality measurement using a Wentworth Labs 11PO900 probe station (Wentworth Laboratories, Inc., Brookfield, CT). In order to access the contact pads, the Parylene coating on the pads is removed with oxygen plasma etching or probe tip scratching. Preliminary results show that the samples with Parylene protection have no observable metal damage on the contact pads even after six months of soaking (Fig. 4). The chip still functions, indicating that Parylene-protected IC circuits can remain intact in 77 °C saline for more than six months.

Parylene C packaging performances in liquid environments are studied using the long-term ALST. The test results suggest that Parylene C is very promising for metal and IC circuit

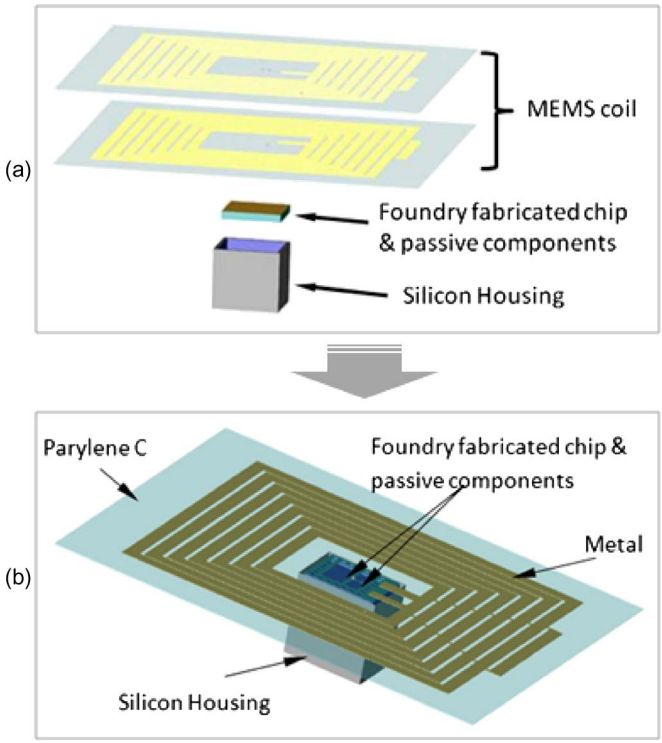

Fig. 5. Conceptual schematic of the embedded chip packaging. (a) Discrete components before integration. (b) Parylene-based MEMS RF coil is integrated with an IC chip embedded in a silicon shell.

protection in intraocular retinal prostheses, and pave the way for the development of the flexible Parylene-based chip integration technology. There are also outstanding issues that deserve future investigation. For example, the ovens used for testing have a temperature variation of $+/-2$ °C. Due to the exponential nature of the Arrhenius relation, this temperature change can significantly affect the accuracy of prediction. In addition, only a small sample set has been analyzed in the initial study because these tests are very time consuming. Continuous experiments will be necessary to collect more data in order to further refine our knowledge of Parylene packaging behavior.

III. RF-Coiled Chip Integration

A. Integrated System Design

An embedded chip integration technology is proposed, in which individual prefabricated chips and discrete components (e.g., capacitors) are embedded in a carrier silicon wafer and sealed with Parylene C. Other surface MEMS structures, such as electrode arrays and RF coils, can be constructed subsequently on the same platform. All interconnections between MEMS devices and chips can be made simultaneously, using standard photolithography and metal patterning process. Fig. 5 shows a conceptual schematic of the embedded chip packaging technology, showing how a prefabricated IC chip is directly integrated with a dual-metal-layer MEMS coil.

The same EM 4100 read-only RFID chip is integrated with an RF MEMS coil for the demonstration of this integration scheme. To determine the dimensions of Si housings, these chips are imaged with a WYKO interferometer (Veeco Instrument Inc., Woodbury, NY) and are measured to have mean dimensions of 1 mm in length, 0.98 mm in width, and 182 μm in thickness. A planar microcoil is designed for wireless power and data transmission, which has two metal layers with 22 turns on each layer and an overall size of 2 cm by 2 cm. Having known the coil geometries, the electrical characteristics of the coil, including its self-inductance, series resistance, and parasitic capacitance, can be predicted using established analytical models, as discussed in [24]–[28]. Because of the low power consumption of the RFID chip, only the coil is needed to power the circuit, and no extra capacitor is required.

B. Fabrication

Fig. 6 shows the detailed fabrication process, starting with a standard 4-in wafer that is ~ 550 μm thick and coated with a layer of sacrificial photoresist. A 5-μm layer of Parylene C is then deposited on top of the photoresist. To secure Parylene on the substrate, Parylene anchors surrounding the chip housings are etched into silicon using Bosch process in a deep RIE system (Unaxis Corporation, St. Petersburg, FL) [29]. After Parylene deposition, a 500-nm layer of gold is deposited in an e-beam evaporator and patterned to form the first layer of coil wires. Next, cavities matching the chip dimensions are etched into the Parylene and silicon using RIE and the Bosch process, and the chips are then dropped into the cavities with an average lateral displacement of less than 10 μm. During this procedure, epoxy is applied to the bottom of the cavities as needed in order to compensate for cavity depth inaccuracy and to fill the gaps surrounding the chips. A metal pole with a flat silicon piece attached on one end is used to push the chips into the cavities and to level the surface. After the chips are fitted into the cavities, Parylene deposition is performed again to seal the chips in place and to form an insulation layer between two metal layers, followed by oxygen plasma etching to properly open interconnection vias. A second 500-nm layer of gold is then deposited and patterned as the top layer of coil wires and chip interconnects. Another 5-μm layer of Parylene C is coated on top, followed by oxygen plasma patterning to define the profile of devices. Through-wafer trenches surrounding the chips are then etched from the backside of the wafer using the Bosch process, and the Parylene-based coils are released from the substrate, carrying the chips that are completely encapsulated in silicon housings. Lastly, the entire device can be sealed with Parylene for extra protection.

In this integration method, minimizing the vertical displacement of the chip from the wafer surface is crucial for subsequent photolithography and metallization steps. Large vertical displacements can lead to broken wires and open circuits. The surface heights of the chips are measured with a stylus profilometer P-15 (KLA-Tencor, San Jose, CA) after the chips are anchored in place in the silicon shell. Fig. 7 shows the surface profiles of four successfully integrated chips with respect to the surrounding substrate. The overall vertical displacements from the wafer surface are within 6 μm, providing sufficient flatness for subsequent processes.

Another important aspect is the horizontal alignment of perimeter interconnects to the embedded chips, which limits the

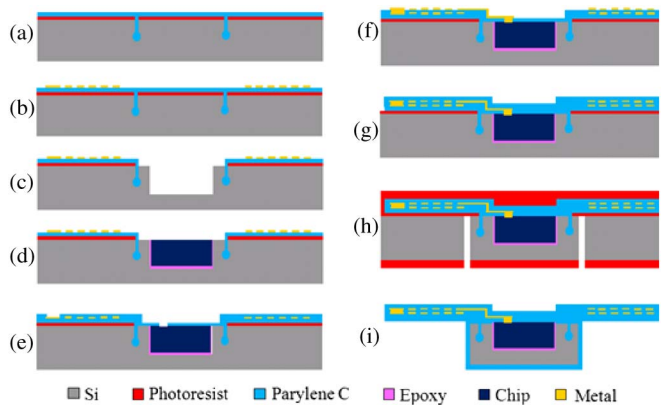

Fig. 6. Detailed process flow of the embedded chip integration scheme.

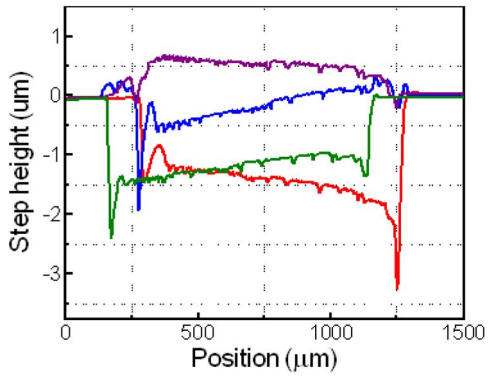

Fig. 7. Vertical displacements of four successfully integrated chips: The wafer surface corresponds to 0-μm step height.

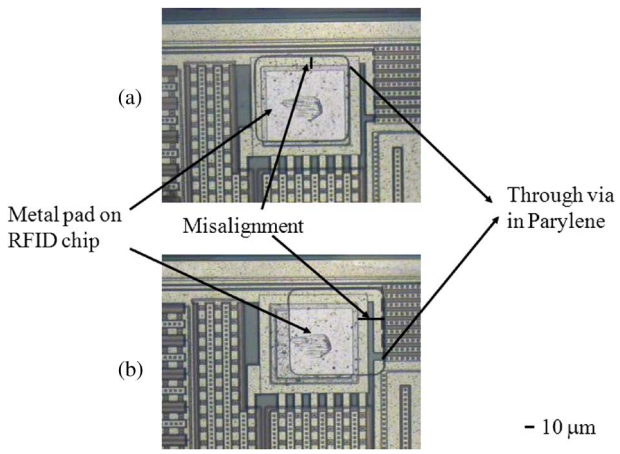

Fig. 8. (a) Example of $<$ 10-μm lateral misalignment of the chip. (b) Example of $>$ 10-μm lateral misalignment of the chip.

interconnection density of the integration. By design, the chips should be self-aligned in the silicon housing to within 10 μm of lateral displacement; however, some chips were misaligned by more than 10 μm due to the dimension variation of the chips themselves (Fig. 8). With tighter tolerance on cavity sidewalls, or with more precise chip-alignment lithography, this alignment deviation can be reduced in the future to achieve high-lead-count integration.

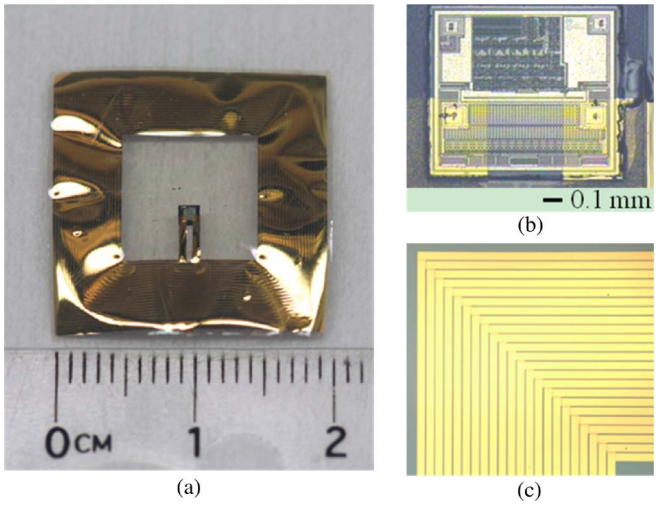

Fig. 9. Integrated RFID tag. (a) Overall view of the device. (b) Close-up view of the embedded RFID chip. (c) Close-up view of the metal traces of the MEMS coil.

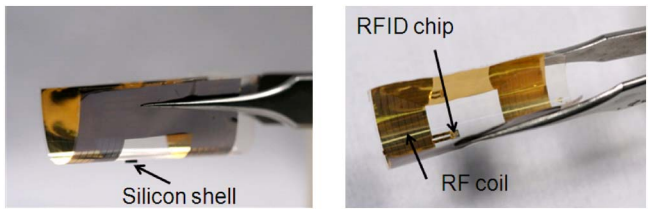

Fig. 10. Flexibility of the Parylene–metal–Parylene thin-film structure.

C. Fabrication Results

We have successfully integrated the RFID chip with the Parylene-based RF coil, and Fig. 9 shows an example of a fabricated embedded RFID tag. In this device, the self-inductance of the receiver coil is approximately 16 μH, and the dc resistance is around 275 Ω. The quality factor (Q-factor) of the coil is calculated with a value of approximately 0.05 at 125 kHz. The total thickness of the Parylene–metal–Parylene thin film is approximately 20 μm.

Because of the excellent mechanical strength and intermediate flexibility (Young's modulus $\approx$4 GPa) of Parylene C, this final device is very flexible and foldable, allowing the device to be placed in direct contact with delicate tissue during surgical implantation (Fig. 10). The coil area is puckered due to thermal stress, which can be allayed with a postfabrication annealing process. During this treatment, the devices are sandwiched between two metal plates and annealed typically at 200 °C. The annealing treatment can also be used to reshape Parylene–metal–Parylene thin films into geometries of interest for target applications [11], [12].

D. Testing Results and Discussion

The functionality of the embedded RFID chip is tested with a commercially available RFID reader module (Parallax Inc., Rocklin, CA). This module contains an integrated coil to transmit RF energy and receive the data from the RFID chip. The transmission coil has dimensions of 60 mm by 66 mm. Fig. 11

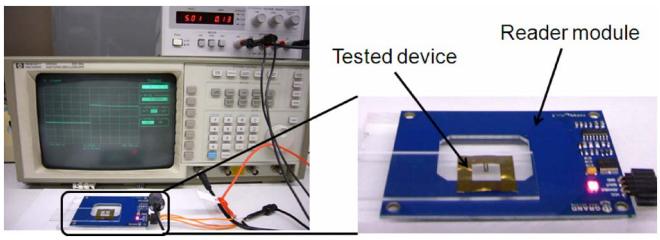

Fig. 11. Test setup to verify the function of the integrated RFID tag. The tested device is placed on top of a commercially available RFID reader module, and the output signal is observed using an oscilloscope.

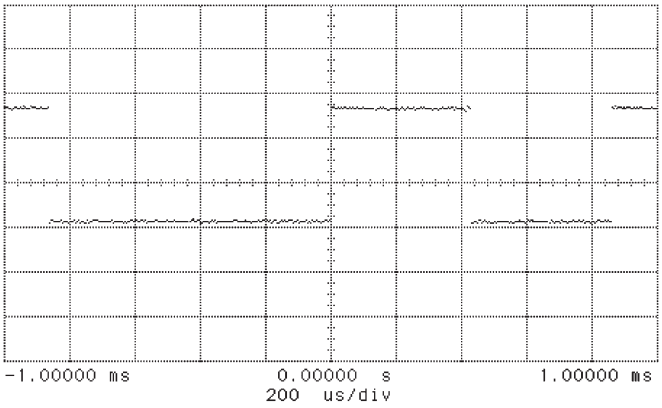

Fig. 12. Typical signal readout from the RFID reader module.

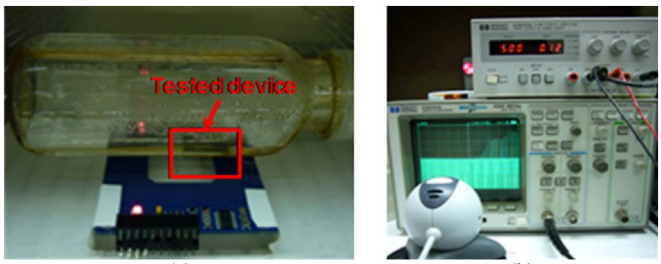

Fig. 13. (a) Test setup to evaluate the function of the integrated RFID tag in saline solution, showing a test unit heated in the convection oven. (b) Real-time monitoring of the signal readout using a webcam.

shows a typical test setup, in which the reader module is driven by a 5-V dc voltage power supply and the output port of the reader is connected to an oscilloscope in order to monitor the signal readout. When the RFID tag is placed within the reading distance of the reader, the information stored in the chip will be sent back to the reader, and an 8-b transistor–transistor logic signal sequence can be observed on the oscilloscope (Fig. 12). The spatial separation between the primary and secondary coils is varied during the measurement, and a maximal detectable range of 3–4 mm is found. This reading distance is mainly limited by the low Q-factor of the receiver coil, which can result in low power transfer efficiency through the electromagnetic field.

The function of the integrated RFID tags is also validated in saline solution to simulate *in vivo* conditions (Fig. 13). From the aforementioned soak testing results, we can deduce that thicker Parylene films can cover small defects and particles and thus prevent unwanted particle-induced Parylene breakdown.

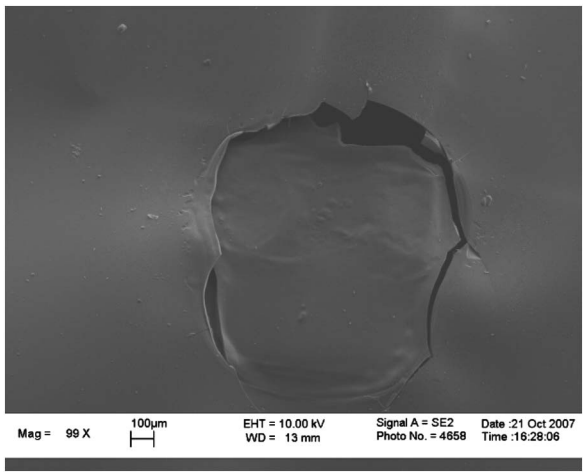

Fig. 14. Typical SEM image shows Parylene cracks along the edges of the embedded chips after active soak testing.

In this experiment, the integrated device is coated with an additional layer of Parylene C that is approximately 12 μm thick and placed in a plastic container filled with saline. The reader module is placed externally with respect to the container and continuously transfers power and data through inductive coupling. The RFID tag is heated in a convection oven at 77 °C, and the signal readout is monitored using a webcam in order to determine the device lifetime. Similar output signal has been observed, indicating the successful power and data transmission in saline. Unfortunately, the devices only functioned for a short time period, and no output could be detected after two to three days of soaking. Parylene microcracks are found along the edges of the embedded chips when examining the failed samples under SEM (Fig. 14). Although the mechanisms that cause these cracks are not entirely understood, it is believed that the coefficient of thermal expansion (CTE) mismatch between the Parylene package (linear CTE of Parylene C $\sim 10^{-5}/^{\circ}$C) and the embedded silicon chip (linear CTE of silicon $\sim 10^{-6}/^{\circ}$C) plays an important role. Consequently, the Parylene coating is torn from the silicon substrate when the device is heated to 77 °C. In addition, the heat generated during intensive active operation could accumulate due to poor heat dissipation in hot saline, which could possibly result in thermal stress concentration along the edges. More experiments are expected to enable a complete understanding of failure mechanisms and shed insight on methods to mitigate them. Further modifications can include using a thicker Parylene coating combined with epoxy or silicone to smooth out the sharp corners of the chip.

IV. Conclusion

Long-term ALST has been done in hot saline, which shows positive results for Parylene-protected metal and Parylene-protected chips, respectively. A Parylene-based embedded chip integration technology has been developed and successfully demonstrated by integrating a flexible MEMS RF coil with a commercially available read-only RFID chip. The functionality of the embedded chip is validated using an RFID reader module in both air and liquid environments. The preliminary results

of active soak testing suggest that the integrated devices can withstand high-temperature soaking with intensive electrical stressing for a few days. Further modifications will be needed in order to improve the reliability and stability of the integrated system. Although specifically tailored to the needs of retinal prostheses, this technology can also be used for other biomedical or IC applications by varying circuitry and passive components to achieve different system functionalities.

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