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Wafer-level SLID bonding for MEMS encapsulation

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Abstract Hermetic packaging is often an essential requirement to enable proper functionality throughout the device's lifetime and ensure the optimal performance of a micro electronic mechanical system (MEMS) device. Solid-liquid interdiffusion (SLID) bonding is a novel and attractive way to encapsulate MEMS devices at a wafer level. SLID bonding utilizes a low-melting-point metal to reduce the bonding process temperature; and metallic seal rings take out less of the valuable surface area and have a lower gas permeability compared to polymer or glass-based sealing materials. In addition, ductile metals can adopt mechanical and thermo-mechanical stresses during their service lifetime, which improves their reliability. In this study, the principles of Au-Sn and Cu-Sn SLID bonding are presented, which are meant to be used for wafer-level hermetic sealing of MEMS resonators. Seal rings in 15.24 cm silicon wafers were bonded at a width of 60 μm, electroplated, and used with Au-Sn and Cu-Sn layer structures. The wafer bonding temperature varied between 300 °C and 350 °C, and the bonding force was 3.5 kN under the ambient pressure, that is, it was less than 0.1 Pa. A shear test was used to compare the mechanical properties of the interconnections between both material systems. In addition, important factors pertaining to bond ring design are discussed according to their effects on the failure mechanisms. The results show that the design of metal structures can significantly affect the reliability of bond rings.

Keywords Micro electronic mechanical system (MEMS) · Solid-liquid interdiffusion (SLID) bonding · Transient liquid-phase (TLP) bonding · Defects · Shear test · Reliability

1 Introduction

Micro electronic mechanical system (MEMS) devices often require a sealed environment for optimal performance. In a large variety of applications, the functional structures in MEMS devices have to be capped hermetically and protected from such things as moisture, particles, gases, and physical loads. For many MEMS devices, there is a requirement for low operating pressure inside the package, which originates from the need to minimize the air film damping of the vibrating structures. In these packages, leaking may induce losses such as air damping, which will compromise the device's performance or even make the device stop functioning altogether. Thus the lifetime of the MEMS devices is highly dependent on the integrity of the bonds. The encapsulation methods that are traditionally used include anodic, glass frit, and metal bonding. Metal bonding can also be divided into the following sub-categories: eutectic bonding, solder bonding, and solid-liquid interdiffusion (SLID) (or transient liquid-phase (TLP)) bonding [1–3].

SLID bonding designed for semiconductor joining was described as "a process whereby high-temperature phases are formed by diffusion in the presence of liquid", and also "a technique which utilizes these phenomena in producing high-temperature-stable bonds which have been fabricated

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at low temperatures" by Bernstein [4]. Ag-In, Au-In and Cu-In metal systems had been discussed in his study. And later, researchers figured out how to exploit more metal systems for SLID bonding, including Ag-Sn [5], Au-Sn [6–10], Cu-Sn [11–13] and Ni-Sn [14, 15], for semiconductor packaging. Some ternary metal systems have also been developed, such as Cu/Ni/Sn [16, 17]. This SLID bonding method, which is already commonly utilized to assemble power electronic components [18], is now also becoming more and more popular in other fields as well, such as 3D packaging. Agarwal et al. [13] utilized Cu-Sn SLID for die stacking in 3D integration. Similarly, Liu et al. [19] performed wafer-level Cu-Sn SLID interconnects in a vacuum, which is promising for 3D assembly and packaging. For their part, Klumpp et al. [20, 21] proposed a wafer-level, 3D integration approach called inter chip via-solid-liquid interdiffusion (ICV-SLID), which is a new chip-to-wafer stacking technology that can be combined with SLID for copper and tin and the inter chip via (ICV) process to form multiple device stacks. In some cases, the SLID can even be used in other applications besides the semiconductor industry, such as superalloy bonding [22] and the joining of structural intermetallic compounds (IMCs) [23].

Most of the SLID bonding applications designed for the electrical interconnections and the die attachments in the 3D packaging can directly be used for the MEMS packaging. In addition, the application of the SLID bonding technology in hermetic sealing for vacuum is becoming more and more attractive and important in terms of MEMS packaging for the industry in addition to the traditional AuSn solder and eutectic Au-Si bonding, especially considering the fact that the melting temperature of the sealing metals is much lower than the re-melting temperature of the formed IMCs. In addition, metals have a higher density than glass materials, and, as such, a lower gas permeability, thus making metals very suitable for hermetic sealing. The flexibility of utilizing many different metal combinations can meet the various requirements for manufacturability, functionality, and reliability, especially when considering that the low melting point metal combination (<400 °C) can lower the bonding process temperature, which can lead to lower thermo-mechanical stresses. In addition, the footprint of the devices can be minimized by using narrow metallic seal rings. Therefore, the metal encapsulation may also significantly increase the lifetime of MEMS devices in high temperature applications [24]. Welch et al. [25, 26] tested the Ni-Sn and the Au-In metal combinations to MEMS wafer level vacuum packaging. They sealed the Pirani gauge in the vacuum with the bond rings, and focused on the pressure change of the sealed space in a long service time. This SLID bonding was also combined with wafer-level solder transfer technique by Welch et al. [27] to transfer a metal MEMS cap and bond it to a device wafer simultaneously. Vivek et al. [28] proposes two prospective candidates, Al-Ge and Pt-In, for hermetic sealing of MEMS sensor for rugged environment applications. They made a conclusion that Al-Ge eutectic is a more prospective candidate for harsh environments due to its immunity to thermal degradation. Marauska et al. [29] present the low temperature and high quality SLID bonds of Au/Sn and Cu/Sn electroplated material systems designed for MEMS wafer-level hermetic vacuum sealing.

However, the design of the metal layers and the important factors concerning of both the microstructure and the bond quality are not quite available. Thus, in this work, the design of two metal bond combinations of Au-Sn and Cu-Sn are studied. The principle for the layer's structure design is discussed. The microstructure of the rings after bonding is also studied. We chose to use the shear test to evaluate the mechanical properties of the bond rings. Failure analysis will reveal the effect of the bond ring design on mechanical properties and the reliability of the bond rings.

2 Principle of SLID bonding

SLID bonding uses the low melting temperature of the filler alloy and forms a high-melting and non-ductile joint. The difference between the low processing temperature and the final high-melting temperature is one of the most interesting benefits of SLID bonding, which allows for sequential processing at the same process temperature. With the SLID process, at least one low-melting metal and one high-melting metal are involved, which can form IMC phases. The metal thickness has to be in the range of a few microns to finish the process within a reasonable amount of time. Generally, SLID bonding consists of four stages: melting, dissolution, isothermal solidification, and homogenization. Once the bonding temperature is above the eutectic point for the metal system in question, a liquid phase appears. Then, the low-melting-point metal begins to react with the base metals and is gradually transformed into IMCs, which have a higher melting point than that of the interlayer. Depending on the process parameters (namely temperature and time), the joint is either formed by way of solidification from a specified nominal composition or it undergoes isothermal solidification. The former is typical in Au-Sn-based solutions and the latter in Cu-Sn-based solutions. A valuable review of the theory of the SLID bonding process has been provided by Zhou et al. [30].

Figure 1 schematically shows the formation of the hermetic bond using the Au-Sn system. The phase diagram used here is from a study by Okamoto [31]. After the initial contact of the metallizations has been obtained and temperature has risen above the eutectic temperature of 215 °C

for the system, liquid forms at the interface. Typically, the process temperature is well above the melting point of Sn and the dissolution of the Au is rapid (in the order of μm/s), since the solubility of Au in liquid Sn is high. In principle, the Sn liquid is first consumed by the formation of AuSn, which is then re-melted when more gold is diffused from the reaction layer. Basically, a concentration profile in liquid should then exist, which should be in equilibrium with both the AuSn and hcp phase. However, since these reactions occur quite rapidly, the solid state diffusion mechanisms do not have time to contribute to the process. Therefore, the analysis can be simplified by assuming that the dissolving Au is mixed into the Sn liquid, thereby forming a certain average nominal composition. This composition is defined by the process temperature, the time, as well as the thickness of the Sn layer. Take the nominal Au atomic percentage of 76 % as an example, as shown in Fig. 1. The nominal composition is located in the region of "L + hcp". Within the structure, the liquid Au-Sn phase will come into equilibrium with some amount of the primary hcp phase. When the cooling starts, the grains of the primary hcp phase grow upwards, and liquid phase remains in equilibrium with the hcp phase until a eutectic temperature of 278 °C is reached. Once the eutectic temperature has been reached, the rest of the liquid is consumed by the simultaneous formation of the AuSn and hcp phase. As the cooling continues, the relative amount of the hcp phase decreases while the AuSn phase increases until the hcp phase becomes unstable at 190 °C and is transformed into Au_5Sn. Hence, the stable structure at room temperature consists of the primary Au_5Sn phase and a two-phase mixture eutectic structure of the AuSn and the Au_5Sn. It must be emphasized that thermodynamic equilibrium is assumed throughout our analysis and that, for example, nucleation as well as the undercooling effects are neglected in this paper.

Since the nominal Au atomic percentage is up to 84 %, as shown in Fig. 2, the composition is located in the region of the "hcp" phase. If there is still a base Au left, the hcp grain initials on the interface and then grows gradually into the liquid until it consumes all of the tin. The structure consists of a residual gold and hcp phase. When cooling to 190 °C, the hcp phase becomes unstable and is transformed into Au_5Sn. Thus, the stable structure at room temperature mainly consists of the Au_5Sn phase.

Figure 3 schematically shows the formation of the hermetic bond utilizing the Cu-Sn system. The phase diagram comes from a study by Fürtauer et al. [32]. After the initial contact of the metallizations, and after the temperature has increased above the eutectic temperature (222 °C of the Cu-Sn system), the formation of liquid occurs at the interface between Cu and Sn. In principle, the liquid Sn is first consumed by the formation of Cu_6Sn_5, which is then transferred into Cu_3Sn in a solid state when more copper is diffused from the reaction layer, as shown in Fig. 3. Hence, the stable structure at room temperature consists of a residual Cu and Cu_3Sn phase, which is thermally stable up to 640 °C [33–35].

3 Experimental procedure

For the sample preparation of both the Au-Sn bonding and the Cu-Sn bonding, standard double side polished (DSP) 150 mm silicon wafers were used as handle wafers and single side polished (SSP) wafers as cap wafers. The back

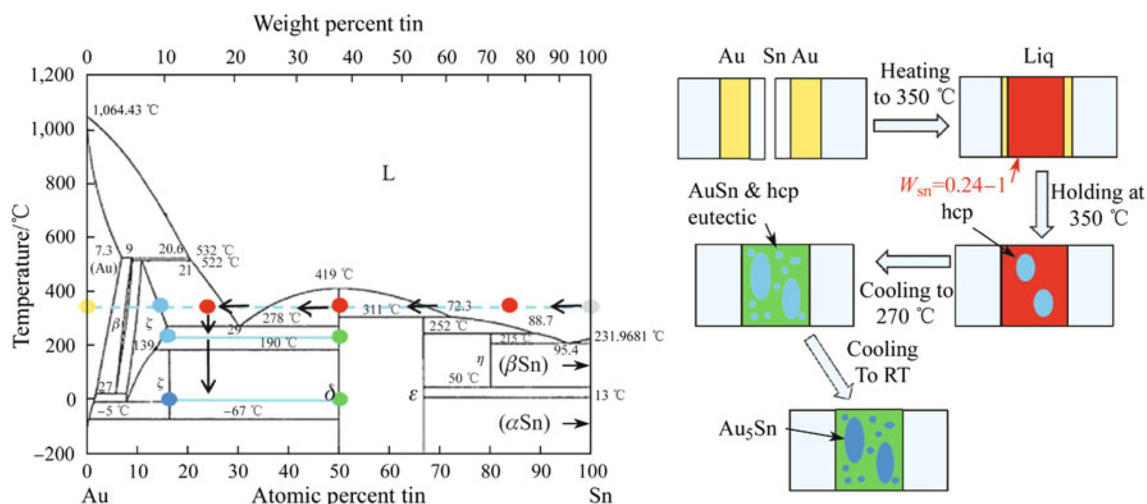


Fig. 1 Schematic presentation of the formation of the Au-Sn SLID joint (with a higher Sn ratio): the *yellow* and *gray dots* in phase diagram [31] represent the original Au and Sn, the *red dot* is the average composition of the liquid before cooling, and the *dark blue*, *light blue* and *green dots* represent the composition of the Au_5Sn, hcp and AuSn phases, respectively

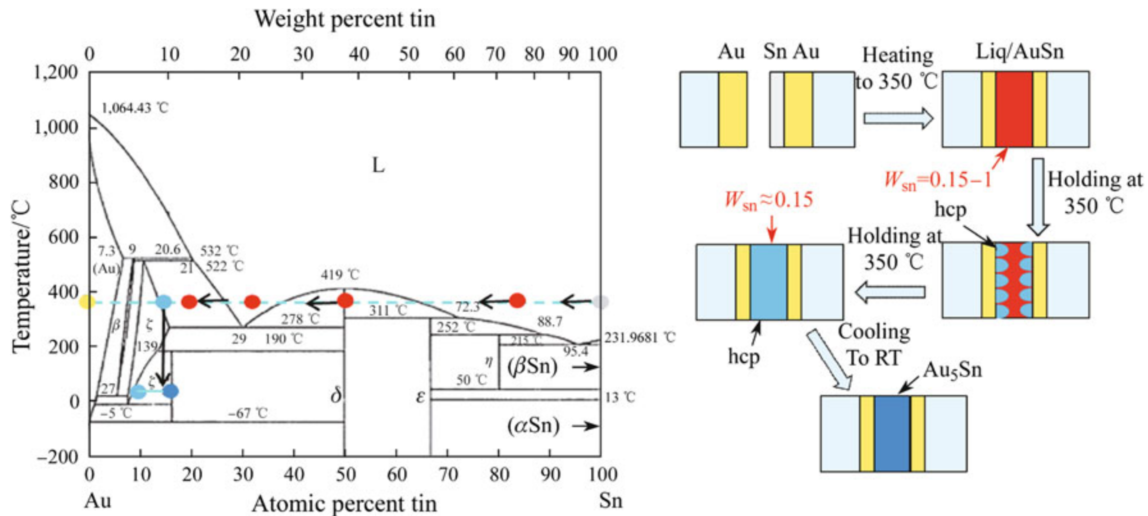


Fig. 2 Schematic presentation of the formation of the Au-Sn SLID joint (with a lower Sn ratio): the *yellow* and *gray dots* in phase diagram [31] represent the original Au and Sn; the *red dot* is the average composition of the liquid before cooling; and the *dark blue* and *light blue dots* represent the composition of Au_5Sn and hcp, respectively

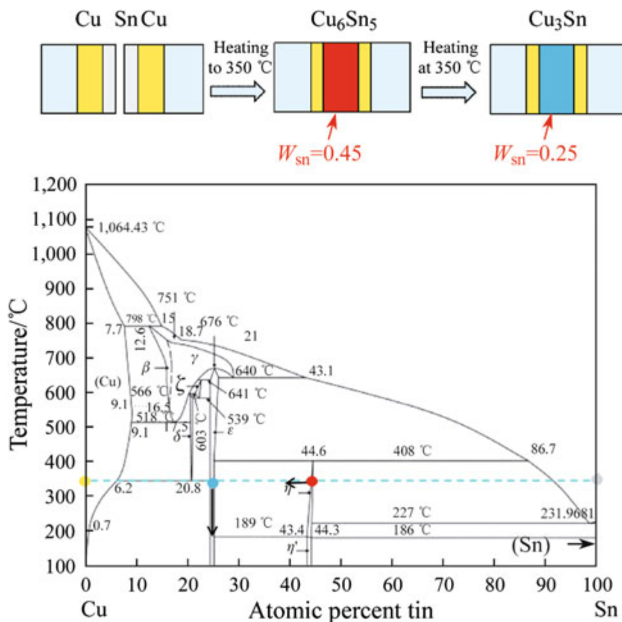
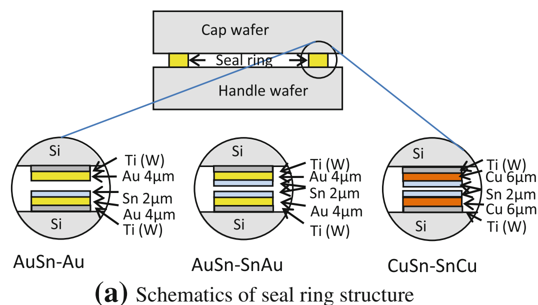


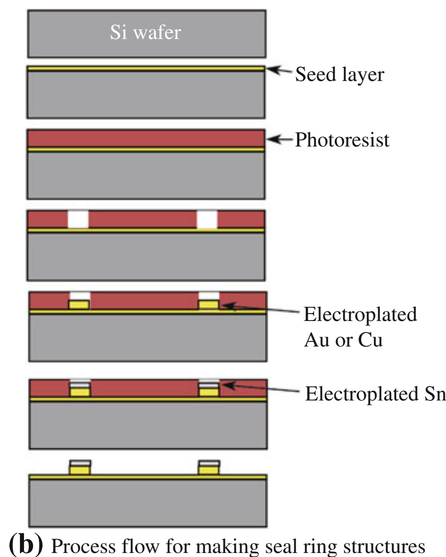
Fig. 3 Schematic presentation of the formation of the Cu-Sn SLID joint: the *yellow* and *gray dots* in phase diagram [32] represent the original Au and Sn, while the *red dot* and *blue dot* represent the composition of Cu_3Sn and Cu_6Sn_5, respectively

side alignment marks were fabricated on the handle wafer before bonding for alignment. A thin titanium tungsten layer was used as an adhesion layer between the silicon and the seed layer. Gold or copper seed layers were sputtered to the front side of both the handle and the cap wafers. A copper seed layer was used for making CuSn seal rings and a gold seed layer for making AuSn seal rings. During the lithography process, a thick photoresist was coated on the surface and removed from the seal ring areas. The seal rings were electroplated to the resist openings using the Everplate Cu 200 chemicals from Atotech for the copper bath, Neutronex 309 from Enthone for the Au bath and Solderon BP from Rohm & Haas for the Sn bath. The target thickness for the gold and copper electroplating in both the handle wafer and cap wafer was 4 µm and 6 µm, respectively. Three different bonding schemes were tested in this study, as shown in Fig. 4a: (i) The handle wafer has Sn and Au layers, whereas the cap wafer has only an Au layer (for short, written as AuSn-Au); (ii) the handle wafer and the cap wafer have the same Sn and Au layers structure (for short, written as AuSn-SnAu); and (iii) the handle wafer and the cap wafer have the same Sn and Cu layers structure (for short, written as CuSn-SnCu). The total thickness of the Sn is 2 µm for AuSn-Au bonding and 4 µm for AuSn-SnAu and CuSn-SnCu bonding. The seal ring thickness and thickness uniformity were measured after resist removal using a profilometer. The dimension of the ring is 1,576 µm × 783 µm, with the width being 60 µm. The seal ring fabrication process steps are shown in Fig. 4b.

After the seal ring structures were ready, the wafers were aligned and placed on a bonding chuck using EVG620 bond aligner. Then, the bonding chuck was transferred to the bonding chamber of the EVG501 wafer bonder. The wafer pair was kept in a vacuum (0.1 Pa) for 30 min, after which the wafers were brought into contact; a pressing force of 3.5 kN was applied and the chamber heating was switched on. Three different bonding parameters were used for the three bonding schemes: (i) For AuSn-Au, the bonding chamber was heated to 350 °C and kept at this temperature for 30 min; (ii) for AuSn-SnAu, the bonding temperature was 320 °C and lasted for 60 min; and (iii) for CuSn-SnCu, the bonding temperature was



(a) Schematics of seal ring structure



(b) Process flow for making seal ring structures

Fig. 4 Schematics of the seal ring structure and production process flow

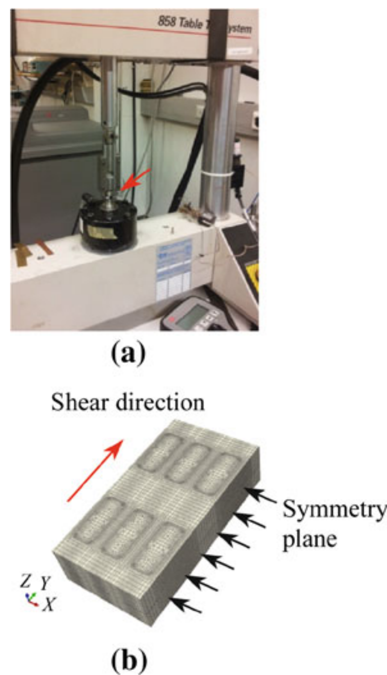


Fig. 5 Shear test setup and simulation model

300 °C and lasted for 30 min. The whole bonding process took 3.5–6.0 h, including both the heating and cooling process. All the wafers were diced into small chips with a dimension of 5 mm × 5 mm, and each chip included 12 seal rings arrayed in 2 columns. The bonding quality of the seal rings was analyzed using cross-sectional scanning electron microscopy (SEM).

The MTS 858 table test system was used for conducting a shear test of the chips from the diced bond wafers in order to evaluate the bonding quality as well as to find out the mechanical failure mechanism of the bond rings. Figure 5a shows the designed holder for the specimens and the general experimental setup. The shear direction is along the long side of the seal rings. The shear speed used in this study was 0.01 mm/s. Finite element analysis was employed to study the non-uniform stress distribution in the seal rings during the shear test. The simulation was carried out using a finite element package: the ABAQUS v. 6.12-3. As shown in Fig. 5b, only half of the sample was modeled due to symmetry and the right-sided surface was the symmetry surface. In terms of boundary conditions, the bottom of the lower silicon chip was fixed, while displacement loading was applied to the top silicon chip.

4 Results and discussion

4.1 Au-Sn materials system

Two different Au-Sn compositions are compared to demonstrate the design of the seal ring structures, which was achieved using AuSn-Au and AuSn-SnAu bonding, as described above.

4.1.1 AuSn-Au bonding

In AuSn-Au bonding, the Sn layer only exists on the handle wafer side. During bonding, the Sn layer will melt and react with the Au layers along both sides of the wafer. The thickness of Sn is 2 μm and the total thickness of the two Au layer on both the substrate side and the cap side is 8 μm. The Sn mole percentage is approximately 13.5 % in the seal ring, if complete mixing is assumed. Based on the discussion in Sect. 2, the microstructure of the ring should include Au_5Sn and residual Au after remaining at a temperature of 350 °C for 30 min. In the final rings, it is quite common to find out that the residual Au existed only in the cap wafer side, as shown in Fig. 6a.

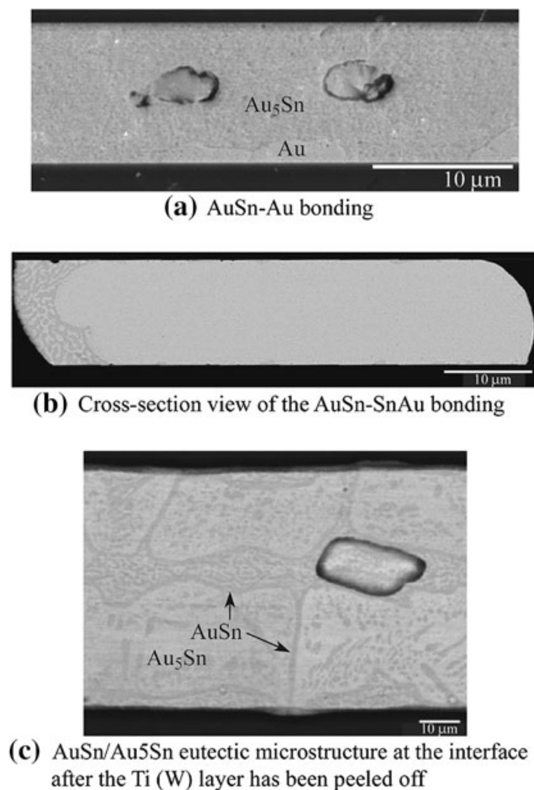


Fig. 6 Microstructure of the Au-Sn bonding at different ratios

4.1.2 *AuSn-SnAu bonding*

In AuSn-SnAu bonding, both the handle wafer and the cap wafer had the same AuSn layer structure: 2 μm for Sn and 4 μm for Au. The average Sn mole percentage in the seal ring is now 23.8 %. According to the Au-Sn binary phase diagram in Sect. 2, the excessive amount of Sn will consume all of the Au layer in the ring after bonding at 320 °C for 60 min and the final microstructure should consist of a primary Au_5Sn and Au_5Sn/AuSn eutectic structure. As shown in Fig. 6b, the real cross-sectional SEM image shows the main part of the ring is primary Au_5Sn, and the eutectic structure can be found at the edge of ring. The interfacial microstructure can be observed after peeling off the cap wafer and the Ti(W) adhesion layer, as shown in Fig. 6c. The Au_5Sn and AuSn eutectic structure can also be found at the interface close to the Ti(W) adhesion layer.

4.2 Mechanical properties of Au-Sn seal rings

We conducted shear tests to evaluate the bonding quality as well as the effects of defects in the seal rings. Normally, the shear loading is assumed to be uniformly distributed over all the seal rings, and then this uniform assumption is often used to calculate the shear strength of the bonding. However, in reality the stress-strain distributions in the seal rings are extremely heterogeneous. Figure 7 shows the first principal stress and strain distributions of the seal rings at the time point just before cracking. It is obvious that the stress concentration was located at the ring's short edges, close to the outer boundaries. This finding tells us that at the initial stage of the shear test, the short edges were holding most of the shear loading until they failed due to cracking. The crack propagation path in one ring should start from the short side close to the boundary and proceed to the other short side close to the chip center. Furthermore, among the three short edges shown in the strain distribution image, the leftmost one experienced the highest level of stress because the seal ring was located close to the free edge of the sample. The seal ring located in the top left corner is supposed to fail first, following by the rest of the seal rings.

In the real tests, the average maximum shear force for the void samples involved in AuSn-Au bonding was 365 N, with a standard deviation of 30 N. In comparison, the average maximum shear force is only 183 N (with a standard deviation of 23 N) for AuSn-SnAu bonding, which is only half of the value of the AuSn-Au bond rings. There are two different failure mechanisms found for AuSn-Au bonding, and AuSn-SnAu bonding occurs separately.

4.2.1 *AuSn-Au bonding*

We observed large voids in the middle part of the ring, as shown in Fig. 8a. These voids can affect the crack propagation path during the shear test. The fracture surface of the seal ring from the cap wafer and handle wafer can be observed in Fig. 8b and c. Only a small part of the bond remains on the handle wafer side. The major part of the bond is left on the cap wafer side. The location of the voids in the ring can easily be found in the middle of the fractured ring, as shown in Fig. 8b. Figure 8d shows a cross section of the two departed pieces. Based on the higher stress level at these locations during the simulation, we can assume that the crack initiates at the interface of the Au_5Sn and Ti(W) layer along the outer short side of the rings. Then, when the crack tip reaches the void location, the crack will propagate into the voids due to the stress concentration generated by the voids. Eventually, the crack will emerge from the void and go back to the interface along the inner short side of the rings.

The voids come from the uneven Sn layer on the Au metallization, especially when the Sn plating chemistry is not in optimal condition. At the edges of these rings, there will be much thicker Sn than on the other parts of the ring, as shown in Fig. 9. The high edge of the rings may stop the contact of the middle part; in such instances, the voids in the middle of the ring will form during cooling. This means

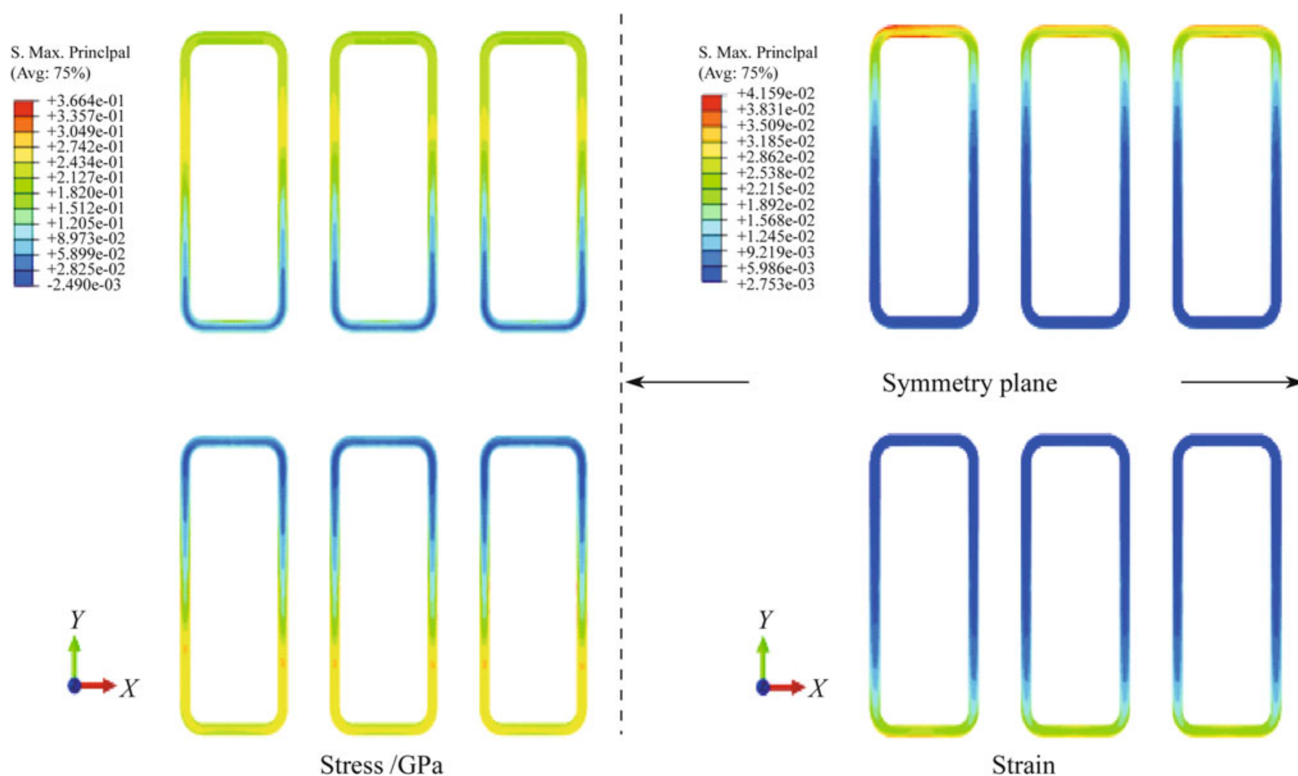


Fig. 7 First principal stress and strain distributions of the seal rings during the shear test

that the thickness uniformity of the layers in the ring is extremely important concerning the mechanical reliability of the rings.

4.2.2 *AuSn-SnAu bonding*

We used flat and uniform Au and Sn layers for AuSn-SnAu bonding, rarely finding the voids. The failure analysis shows that the crack mainly propagates along the interface between the Au-Sn seal ring and the Ti(W) adhesion layer, as shown in Fig. 10. It is highly probable that the direct contact of the AuSn eutectic structure with the Ti(W) layer is the main reason that the average maximum shear force is much lower than the AuSn-Au force.

4.3 Discussion on design of Au-Sn metals system

The results in Sect. 4.2 indicate that the interface bond between the Au_5Sn/AuSn eutectic structure and the Ti(W) layer is weaker than the Au_5Sn and Ti(W) interface. And it should be noticed that in AuSn-Au bonding both of the two different interfaces, the Au-Ti(W) interface and the Au_5Sn-Ti(W) interface, existed in the same ring, but it was rare to find the fracture at the Au and Ti(W) interface. Likewise, all of the observed failures were at the Au_5Sn and Ti(W) interface. It means that the bonding at the Au-Ti(W) interface seems to be much stronger than at the Au_5Sn-Ti(W) interface. Anyhow, the results show that the most reliable interface, which should also be the target interface, is the Au-Ti(W) interface, especially when designing the metallization thicknesses with respect to bonding process parameters. On the one hand, in order to meet the reliability requirement, the direct contact of the Au_5Sn-AuSn eutectic structure with the Ti(W) adhesion layer is not acceptable. On the other hand, the thickness of the Sn layer decides the amount of liquid needed during bonding, which definitely has a limitation that needs to be reduced. Hence, to solve this problem, the choice can either be to increase the amount of Au, which will clearly increase costs, or to utilize a diffusion barrier. For example, Ni seems to be a good choice for barrier material, since the reaction between Ni and AuSn IMCs is rather slow.

4.4 Cu-Sn materials system

In CuSn-SnCu bonding, Sn layers exist on both the cap and handle wafers. The total thickness of Sn is 4 µm, whereas the thickness of the two Cu layers from both the substrate and the cap wafers is 12 µm. The average Sn mole percentage is approximately 12.7 % in the seal ring, if complete mixing is assumed. After bonding at 300 °C for 30 min, the targeted microstructure of the ring should mainly include Cu_3Sn and residual Cu, as shown in Fig. 11a. A small amount of Cu_6Sn_5 will still be

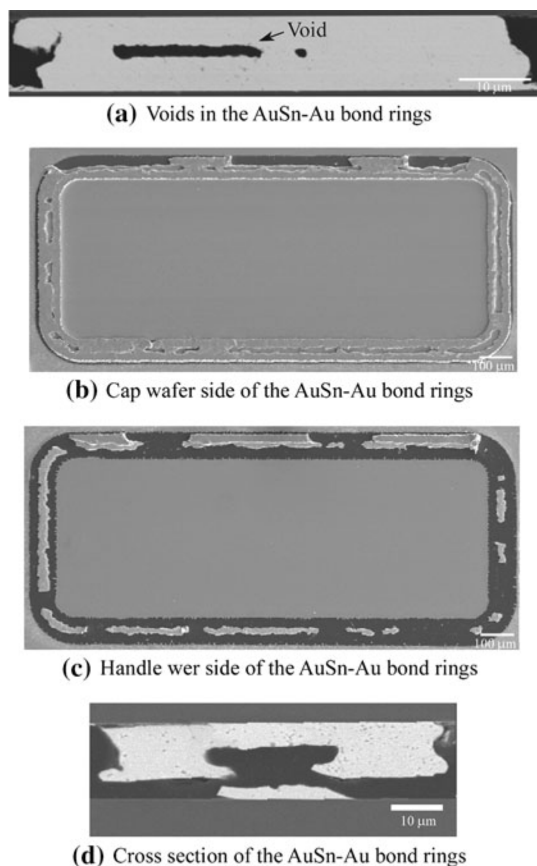


Fig. 8 AuSn-Au microstructure after bonding and the defect for the huge void in the middle of the ring

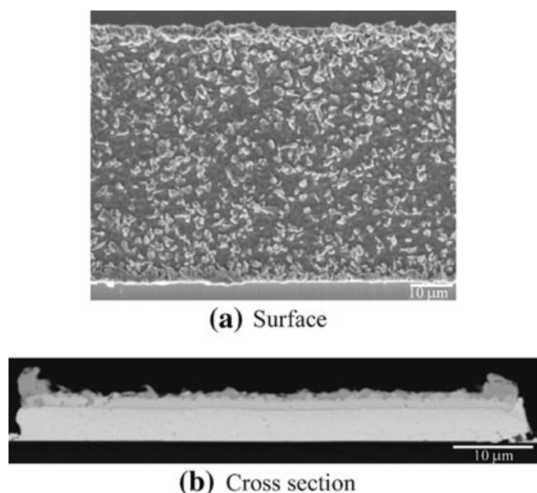


Fig. 9 Uneven Sn layer in the plating rings before bonding

unconsumed at the corner of the rings in most cases, as shown in Fig. 11b. Since Cu_6Sn_5 has a lower elastic module [36] and a smaller fracture toughness than Cu_3Sn [37, 38], it is more prone to fracture under the mechanical load. Such Cu_6Sn_5 might be the initial nucleation site for cracks, and then the cracks could propagate along the interface between Cu_6Sn_5 and Cu_3Sn and finally go inside the bonded region and proceed into the Cu_3Sn layer.

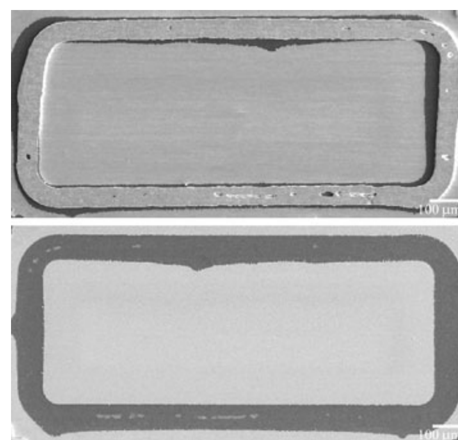


Fig. 10 Two sides of the AuSn-SnAu bond ring shear fracture surface

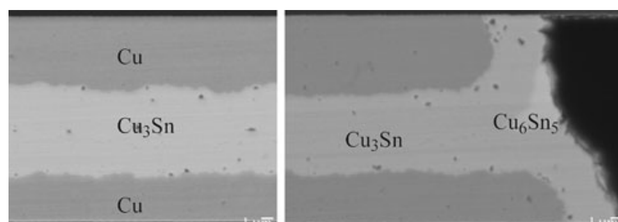


Fig. 11 Microstructure of CuSn-SnCu bonding

Table 1 Thickness of Cu layer and Cu + Sn layers at different positions on both the handle wafer and the cap wafer

		Thickness at different positions/μm								
		C	N	E	S	W	M N	M E	M S	M W
Sub	Cu	6.3	6.0	6.5	6.6	6.0	6.0	6.1	6.2	6.1
	Cu + Sn	8.6	8.3	8.0	9.1	8.3	–	–	–	–
Cap	Cu	7.7	5.5	5.2	5.8	5.6	6.0	6.0	6.5	6.3
	Cu + Sn	11.2	9.1	8.7	9.2	8.9	–	–	–	–

Sub substrate wafer, *Cap* cap wafer, *C* center, *N* north, *E* east, *S* south, *W* west, *M* middle

Here it has to be pointed out that the uniformity of the Cu layer thickness, which is similar to the Sn layer thickness in Au-Sn bonding, also plays an important role in the mechanical property of the bond rings. We measured the thickness of pure Cu after Cu plating and the thickness of both the Cu and Sn layers after Sn plating separately at 9 positions on the wafer, and the corresponding values of each point can be found in Table 1. It can easily be seen that the rings at the center of both the handle wafer and the cap wafer are generally thicker than the ones along the edge of these wafers. The thickness distribution at the

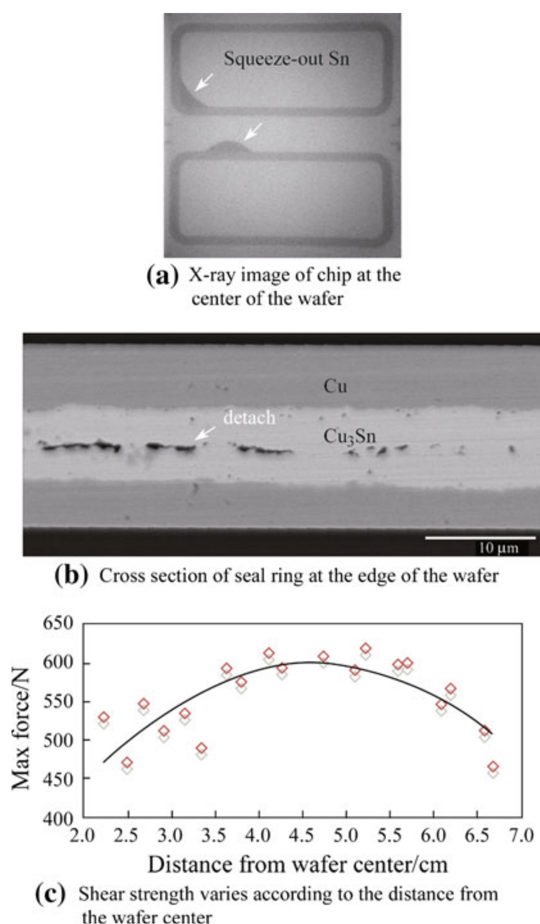


Fig. 12 Effect of Cu layer thickness on the bond's quality and shear force

middle part of the wafer is more uniform. This non-uniformity of thickness can cause a difference in bonding quality all around the wafer: More squeeze-out (containing Cu and Sn) at the center parts of the wafers and more non-bonded regions in the rings along the outer parts of the wafers, as shown separately in Fig. 12a and b. In comparison, the middle part of the wafer has a better quality, as shown in Fig. 10, since the middle part on the wafer has a more uniform thickness after plating. We tested the shear strength of the chip at different locations. Figure 12c shows that the trend of maximum shear force is drawn with distance from the wafer's center. The rings at both the center and the edge of the wafer have lower shear force than the ones in the middle part. The maximum force differences can reach more than 150 N, over one quarter of the average shear force.

5 Conclusions

The design principles for Au-Sn and Cu-Sn SLID bonding are studied in this paper. A different ratio of the metals, especially the Au-Sn ratio, will result in a different microstructure in the rings. Metal systems, including AuSn-Au, AuSn-SnAu, and CuSn-SnCu, are chosen in this work to achieve real bonding for MEMS devices.

For AuSn-Au bonding, the as-bond ring consisted of Au_5Sn and residual Au. The voids in the center of the rings are the main defects that can significantly change the crack propagation path. The cracks in the bond rings started at the Au_5Sn and Ti(W) interface and then propagated into the defect of voids. For AuSn-SnAu bonding, the as-bond ring consisted of primary Au_5Sn and the eutectic structure of Au_5Sn and AuSn IMCs. The excessive Sn atoms that accumulated at the interface will reduce the shear strength of rings significantly. The comparison between AuSn-Au and AuSn-SnAu bonding shows that the Au-Ti(W) interface, which is stronger than the Au_5Sn-Ti(W) interface and the AuSn/Au_5Sn-Ti(W) interface, should be the target interface for bond structure design.

For CuSn-SnCu bonding, the ring mainly consisted of Cu_3Sn and residual Cu. Only a small amount of Cu_6Sn_5 existed at the corner of the rings, which can initiate the cracks during shear testing. The non-uniformity of the Cu layer can induce large variations in the shear strengths around the wafer area.

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