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Wafer-Scale Functional Circuits Based on Two Dimensional Semiconductors with Fabrication Optimized by Machine Learning

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Wafer-Scale Functional Circuits Based on Two Dimensional Semiconductors with Fabrication Optimized by Machine Learning

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Abstract: Triggered by the pioneering research on graphene, the family of two-dimensional layered materials (2DLMs) has been investigated for more than a decade, and appealing functionalities have been demonstrated. However, there are still challenges inhibiting high-quality growth and circuit-level integration, and results from previous studies are still far from complying with industrial standards. Here, we overcome these challenges by utilizing machine-learning (ML) algorithms to evaluate key process parameters that impact the electrical characteristics of MoS_2 top-gated field-effect transistors (FETs). The wafer-scale fabrication processes are then guided by ML combined with grid searching to co-optimize device performance, including mobility, threshold voltage and subthreshold swing. A 62-level SPICE modeling was implemented for MoS_2 FETs and further used to construct functional digital, analog, and photodetection circuits. Finally, we present wafer-scale test FET arrays and a 4-bit full adder employing industry-standard design flows and processes. Taken together, these results experimentally validate the application potential of ML-assisted fabrication optimization for beyond-silicon electronic materials.

Two-dimensional layered materials (2DLMs) have potential applications from mainstream logic and analog circuits to flexible electronics [1-8]. Semiconductive transition metal dichalcogenides (TMDs) are a family of 2DLMs with versatile band structures, among which MoS_2 is the most widely studied representative of TMDs [9-18]. The atomically thin channel with dangling-bond-free interfaces and low in-plane dielectric constants ensure high carrier mobility in extremely scaled devices with robust control over short-channel effects (SCEs) [19-21]. While intrinsic advantages of 2DLMs are promising for More-than-Moore electronic applications [22-25], it is still difficult to meet the stringent requirements for large-scale circuit- and system-level applications, where the primary challenges are wafer-scale material synthesis and device processing [26-29]. Recent progress in chemical vapor deposition (CVD)/metal-organic chemical vapor deposition (MOCVD) growth has enabled semiconductive TMD films with large areas [30-32]. Although satisfied crystalline quality and large-scale uniformity still require further improvement of synthesis techniques, currently available wafer-scale TMD films are practically sufficient for fabricating large-scale circuits.

In order to realize complex cascaded circuits, voltage level matching and high noise margins are also important [33], placing the need for the accurate control of threshold voltage V_T. So far, a circuit based on MoS_2 consisting of 115 field-effect transistors (FETs) with gate-first technology has been reported [33,34]. However, compared to conventional gate-last processing [35], gate-first technology requires a more complex film transfer processing and an extra step of via etching, which not only introduces defects to MoS_2 films but also drastically reduces yield and reproducibility of wafer-scale fabrication. Hence, large-scale 2DLM based circuits require more emphasis on fabrication optimization towards wafer-scale uniformity and reproducibility.

In this work, to realize batch fabrication using 2 in. MoS_2 wafer, machine-learning (ML) algorithms were used to analyze experimental data and evaluate various key process parameters that significantly impact the electrical characteristics of 2D-FETs, enabling optimized electrical performance for enhancement-mode FETs fabricated

using ML-guided gate-last processing. Calibrated by measured electrical data, the device modeling is conducted to guide the design of basic digital, analog, and optoelectrical circuits. With wafer-scale processing using industry-standard design flows and processes, our work illustrates the feasibility of using ML in device processing optimization for emerging novel materials and shortens the learning cycle from fundamental research to practical application.

High quality, uniform MoS_2 was grown using customized CVD equipment (see SI for details). Raman mapping results indicate the synthesized wafer is uniform at the wafer-scale, as shown in Fig. 1a (see Fig S1 for more details). Although the growth of wafer-scale MoS_2 films has been demonstrated [30-32], fabrication of MoS_2 FETs still requires optimizing individual process modules, such as channel doping, S/D contact, and gate stack interface. These process steps are strongly correlated to the final device performance metrics, including carrier mobility (μ), threshold voltage (V_T), and subthreshold swing (SS), as shown in Fig. 1c. For practical applications, it is necessary to optimize the combination of these quantities, and different applications of the device also require different optimization strategies, as illustrated in Fig. 1b. Due to the extremely high sensitivity of channel carriers to the ambient environment, multiple processing steps impact various aspects of electrical performance, making comprehensive process optimization complicated and challenging. After optimizing wafer-scale material and device fabrication processes, we continue to carry out device characterization, SPICE modeling, and circuit design. The obtained device and circuit characterization results can also be further used to guide improvements to the fabrication process, as illustrated by Fig. 1d.

The fast-developed ML technology is commonly used for the efficient understanding of complex mathematical or logical models. ML has been used in many disciplines, such as the exploration of novel materials [36], but there has never been any report on using ML to optimize process modules for 2D devices. Here, we show that ML can improve the fabrication process of devices built on emerging semiconductors more effectively than the conventional process optimization method. Specifically, ML

is used to understand the impact of each processing step on the final device performance. This is essential for materials, such as MoS_2 grown via CVD, which are synthesized on an insulating substrate, making device measurements after each processing step difficult.

A complete process for fabricating MoS_2 top-gate FETs (TG-FETs) is shown in Fig. 2a. The FET performance is measured at the end of the process flow. Ensemble learning (EL), a supervised ML method where multiple learning algorithms are aggregated for more accurate prediction [37], is used here as it is effective for classifying imbalanced data (see SI for more details). The decision tree method is used as a weak classifier because it can efficiently handle discrete data (Fig. 2b). More than 560 MoS_2-FETs on over 40 different wafers were fabricated using specially designed process flows to provide a comprehensive database. We first focus on two device performance parameters, μ and V_T, as μ is directly correlated to operation speed and V_T is essential for fabricating an enhancement mode FET. The importance of each processing step can be determined using only one parameter (μ or V_T) as the sorting standard for EL analysis (see Fig. 2c and Table S1 for detailed processing steps). The generated results are reasonable since V_T is primarily influenced by the top gate structure (metal work function and charge impurities/dipoles in the deposited gate dielectric), while μ depends on more factors, including the contact resistance and charge scattering. The TG electrode metallization also becomes an essential step as indicated by ML analysis, which is unexpected (details see Fig. S6). μ, V_T, and other performance parameters can be comprehensively considered by multiplying a weighting factor for each parameter, depending on the requirements of various functionalities (also see SI).

ML can also be used to co-optimize all process parameters, as shown in Fig. 2d. After EL training, a score predictor can be used to predict the results from any processing combination. All possible processing combinations are then sorted using a grid search method, as shown in Fig. 2e. To demonstrate this, we chose more than 500 devices, which are summarized in the μ-V_T plot in Fig. 2f. While one recipe provides a high μ value (red stars), another recipe provides a positive V_T value. However, both values

decrease when the two recipes are combined, which is mainly due to crosstalk between different processing steps. Therefore, the combination of multiple steps with each optimized recipe does not necessarily generate an optimized device. By following the suggestion of this sorting result, seven devices with better performance were successfully fabricated (red stars in Fig. 2f). This recipe combination (details see Supplementary Table 6) also gives rise to an average μ about 75 $cm^2/V \cdot s$ and V_{th} about 2.1 V, as well as a high wafer-scale uniformity that is important for large scale circuits, as shown in Fig. 2g. The application of the ML algorithm in MoS_2 device optimization is only a case study, and its capability to speed up the learning cycle for performance optimization of devices with multiple processes can be conveniently extended to other 2DLMs and emerging electronic materials.

Since the FETs built on the wafer have high uniformity, we use an RPI model (level = 62) to simulate MoS_2 FETs in an HSPICE simulator. As is shown in Fig. 3a-b, to fit the transfer and output characteristics of MoS_2 FETs, the parameters of the model are configured by adjusting the empirical parameters and characteristic parameters (such as mobility and V_T extracted from transfer curves; thickness and permittivity of the dielectric; W and L of MoS_2 channel). The voltage transfer characteristics (VTC) for a pseudo-NMOS type MoS_2 inverter (M1 as a load transistor and M2 as a pull-down network) were also simulated in HSPICE using the simulation parameters from the same model. By sizing the aspect ratio W/L of two MoS_2 FETs (Fig. 3c) and shifting the V_T value (Fig. 3d) of the M1 independently, the voltage switching point can be tuned to the proper position (around half of V_{DD}) to achieve rail-to-rail output swing and large noise margin (see Fig. S10 for more details).

A flip-flop is a fundamental storage element for sequential ICs [38-41]. Fig. 3e shows a circuit schematic and a die photo of a negative edge triggered D flip-flop (DFF) based on 8 NANDs with 2 inputs and 3 inverters. The measured waveforms from the DFF are plotted in Fig. 3f, where the device outputs correct logic values for given input data on the falling edge of the clock (CLK) and holds the data until the next falling edge. A full adder is another key combinational circuit usually used as a fundamental building block

in an arithmetic logic unit (ALU) [33,42]. Fig. 3g shows a circuit schematic of a 1-bit full-adder and a photograph of the die. The 1-bit full-adder consists of 10 NANDs, 3 inverters, and 1 NOR with 39 n-FETs in total. The measured output waveforms from the 1-bit full-adder are shown in the bottom plots of Fig. 3h, where the outputs ("S" and "Co") produce the correct rail-to-rail voltage for all possible input combinations with 3.0 V supply voltage.

A ring oscillator (RO) is an industrial standard benchmarking circuit for performance evaluation [42,43]. We then fabricated and measured a 5-stage pseudo-CMOS RO with an output buffer (Fig. 3i) to assess the high frequency switching capability of MoS_2. Such RO circuit is composed of five inverters cascaded in a loop chain. High uniformity of all inverter stages, such as their large noise margin, is essential for robust oscillator performance. As shown in Fig. 3j, an oscillation frequency of 19.5 kHz with a propagation delay of $\tau_{pd} = 1/(2nf) = 5.13\ \mu s$ per stage was measured at $V_{DD} = 3$ V, where n is the number of stages. In the future, various methods could be applied to increase the oscillation frequency, which is correlated to gate parasitic capacitance, drive current, and supply voltage.

For memory applications, we present dynamic memory arrays built from MoS_2 FETs (Fig. 3k). A schematic diagram of a 1T-1C circuit is shown in Fig. 3l. An oscilloscope was used to test its function as memory (Fig S14) [44-48]. The experimental results are shown in Fig. 3m. During a write operation, the MoS_2 FET is turned on to provide a low-impedance path, and a positive current pulse (red curve) is collected by the oscilloscope, which indicates the capacitance has been recharged. During the holding state, the MoS_2 FET is turned off and presents a high-impedance path. If the current pulse detected by the oscilloscope is negative during a read operation, it indicates that a charge remains in the capacitor after the hold time. Due to the ultralow leakage current from our MoS_2 FET, the charge saved in the capacitor is expected to be ideally stored, thereby achieving long-term retention. By integrating the current pulse during a read operation, we can estimate the charge retained in the capacitor as a function of hold time, as shown in Fig. 3n. The retention time is defined as the hold time at which the retained

charge (Q_{read}) is zero compared with a read voltage of 0.5 V; the average retention time is on the order of seconds.

Furthermore, our wafer-scale MoS_2 devices can be extended for optoelectrical application[49]. A thin layer Au (~10nm) deposited as TG electrode will have higher optical transmittance, as shown in Fig. 3o. The transfer characteristics (Fig. 3p) from a typical device show a considerable photocurrent of ~1 μA/μm under white light (1.5 mW/cm^{-2}) when V_{TG} = 4 V and an on-off ratio of approximately 100 when V_{TG} = 0 V. In Fig. 3q, we use a 9×9 MoS_2 FET array to demonstrate a simple function of image sensing. The photocurrents are recorded from each pixel by scanning a focused white beam across the array. We set the illumination position to form the English letters F, D and U deliberately. The color pattern representing the photocurrent value exhibits high On/Off contrast and high spatial uniformity.

Here we have demonstrated logic, analog, memory, and optoelectronic functions, which can be conveniently integrated into a single device. In the future, if we further take advantage of the atomically thin and flexible nature of 2D materials, it is possible to prepare three-dimensional monolithic integrated circuits (3D integration) by stacking 2DLMs with different functions [50]. Thus, it provides a new route to implement a complex system to realize various applications.

To demonstrate the potential for high volume production, we fabricated MoS_2 TG-FET arrays and 1-bit full-adder arrays on a 2-inch wafer, as shown in Fig. 4a. Similar to what is normally completed in a semiconductor fabrication facility, the full-adder arrays were placed in the center region of the wafer as a functional block, and MoS_2 TG-FETs were placed surrounding the functional blocks and used to monitor wafer-scale uniformity. Each block contained 16 FETs, and 81 blocks in total were distributed across the wafer. The average mobility and V_T values extracted from the transfer curves in each FET array are plotted in Fig. 4b, showing a wafer-scale uniformity acceptable for batch fabrication. The average mobility and V_T values for all 1296 MoS_2 FETs are 46.7 cm^2 V^{-1} s^{-1} and 1.9 V, respectively, with a standard deviation < 30%. In the rest of the wafer area, we tested 144 1-bit full-adder circuits, revealing 50% yield (right graph of Fig. 4b).

This indicates our wafer-scale MoS_2 film together with device processing have the potential to achieve industrial high-volume production. To the best of our knowledge, these are among the highest mobility and V_T values observed in wafer-scale-fabricated MoS_2 TG devices with high uniformity (Supplementary Table 7). Finally, we fabricated a 4-bit full-adder composed of four parallel 1-bit full-adders consisting of 156 FETs; the microscope image and truth table are shown in Fig. 4c. The 4-bit full-adder was tested using 8 input signal combinations (A3 A2 A1 A0, B3 B2 B1 B0, Ci), including (0000, 0000, 0), (0000, 0111, 0), (1111, 1000, 0), (1111, 1111, 0), (0000, 0000, 1), (0000, 0111, 1), (1111, 1000, 1), and (1111, 1111, 1). The output results in Fig. 4d show that the 4-bit full-adder exhibits correct logical function and rail-to-rail conversion. Thanks to the machine learning optimized fabrication process, we demonstrated the first complete 4-bit full-adder based on MoS_2 TG-FETs, paving the way to constructing future large-scale 2D integrated circuits.

Conclusion

In this work, based on a wafer-scale MoS_2 film, we integrated ML algorithms to analyze experimental data for extracting key process parameters to optimize device performance. Following this strategy, we successfully fabricated enhancement-mode MoS_2 TG-FETs using ML-guided gate-last processing recipes, and the corresponding 62-level SPICE modeling was also built. Basic logic, analog, and optoelectrical circuits were constructed. Finally, wafer-scale device fabrication and measurements using industry-standard design flow and processing were performed. Our results show that ML can be used for device optimization and shortening the learning cycle for novel materials. We also show that our MoS_2 TG-FET technology is a potential route for fabricating large-scale integrated circuits compatible with current silicon-based technologies, and will promote the future application of 2D materials in large scale integrated circuits.

Methods

Synthesis of wafer-scale MoS_2. A crucible with MoO_3 power (Alfa Aesar 99.95%) is placed in Zone 2 while an appropriate amount of sulfur powder (Alfa Aesar 99.999%)

is placed in Zone 1 which is upstream of the flow in the tube. The distance between two zones is 30 cm. A carefully rinsed sapphire substrate is placed face-down on the MoO_3 power. During the synthesis process, 300 sccm argon gas serves as carrier gas. The synthesis temperature for Zone 1 and Zone 2 is controlled at 180 °C and 650 °C, respectively. Continuous monolayer MoS_2 film is synthesized at atmospheric pressure with 10 min sulfuration time.

Fabrication of MoS_2 FETs and circuits. The MoS_2 FETs and circuits are fabricated on the wafer-scale MoS_2 film on the sapphire substrate. The contact electrodes, source and drain contacts, are patterned by laser direct writing technology (Micro-Writer ML3) and subsequently deposited using Electronic Beam (E-beam) evaporation. CF_4 plasma etching is performed to define MoS_2 channel region. A seeding layer is deposited by E-beam evaporation and subsequently annealed in an oxygen atmosphere at 100 °C. Then HfO_2 is then grown by Atom Layer Deposition (ALD) as the FET dielectric layer. Another lithography/lift-off/deposition process is utilized to form the top metal layer. For electrical probing or further fabrication of more complex circuits, SF_6 plasma etching is used to remove the HfO_2 layer on top of the source/drain electrodes to form via holes defined by the lithography.

The machine learning method. The details of ensemble learning, random forest algorithm and feature importance assessment are described in the supplementary information

Electrical measurement. The electrical properties of MoS_2 FETs and circuits are carried out in a probe station connecting to an Agilent B1500A semiconductor analyzer with 8 source measure units. To investigate the circuit's dynamic response, an Agilent 33622A arbitrary waveform generator is used to input signals while a RIGOL DS1054Z digital oscilloscope captures the output voltage.

Data availability. The data that support the findings of this study are available from the corresponding author on request.

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Author contributions: W. B., J.W. P.Z were in charge, advised, and led on all aspects of the project. Y.X., Z.W. and Y.W. developed the ML algorithms. X.C., Y.S., H.T., Y.X., T.W., C.W., S.X. and S.M. contributed to circuit design. X.C., Y.S., H.T., Y.W., F.L., J.M., X.G. and L.T. fabricated the devices and circuits. X.C., H.T., Y.W., S.B, H.S., F.B. and D.H. contributed to the electrical measurements. Z. X., Z.S., Z.X. and Z.D. prepared the 2DLM materials. Y.L., X.G, J.W. advised industrial wafer-scale circuit design and test. All authors discussed the results and commented on the manuscript.

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Figure 1

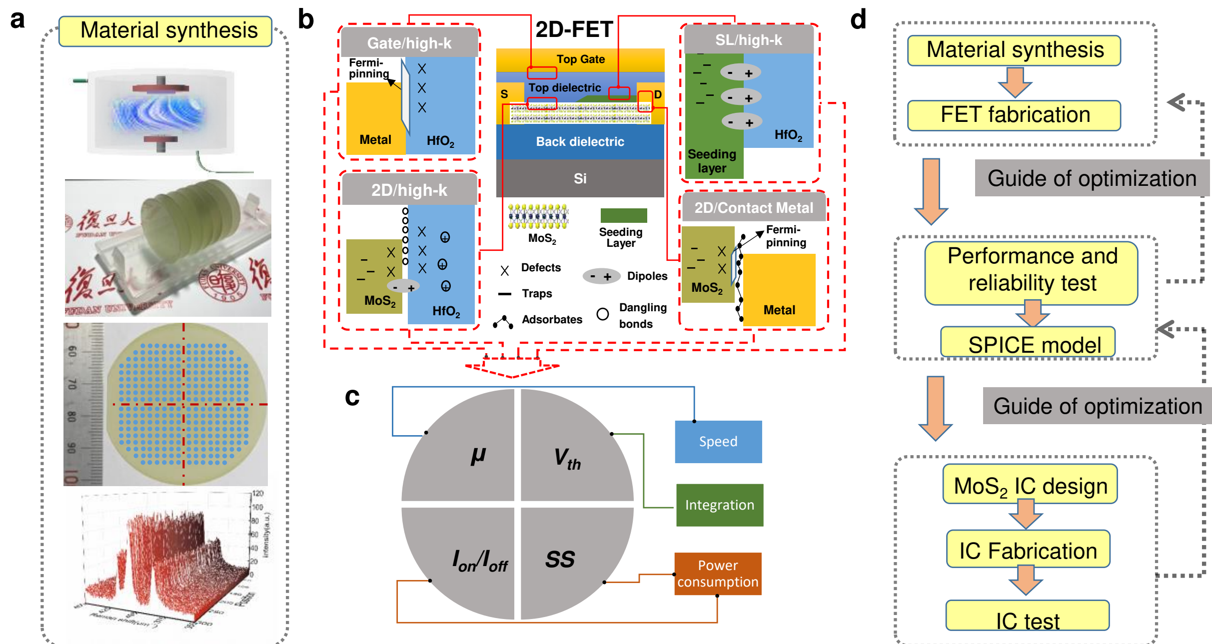


Fig. 1. a, Demonstration of uniform wafer-scale MoS_2 growth by CVD, including a schematic diagram of the material growth equipment, a batch of 2 in. wafer-scale sapphire substrates uniformly covered with MoS_2, a 2 in. sapphire wafer uniformly covered with MoS_2 marked with Raman test points, and Raman mapping spectra from different locations marked in the previous picture. **b,** Schematic cross-section of an MoS_2 FET with TG and global BG. Various factors that influence the device performance are categorized. **c,** Schematic diagram of the relationship between performance parameters of the transistor and performance limitations of the integrated circuit. **d,** Process flow and feedback optimization diagram from material synthesis to industrial-grade circuit design, fabrication, and test.

Figure 2

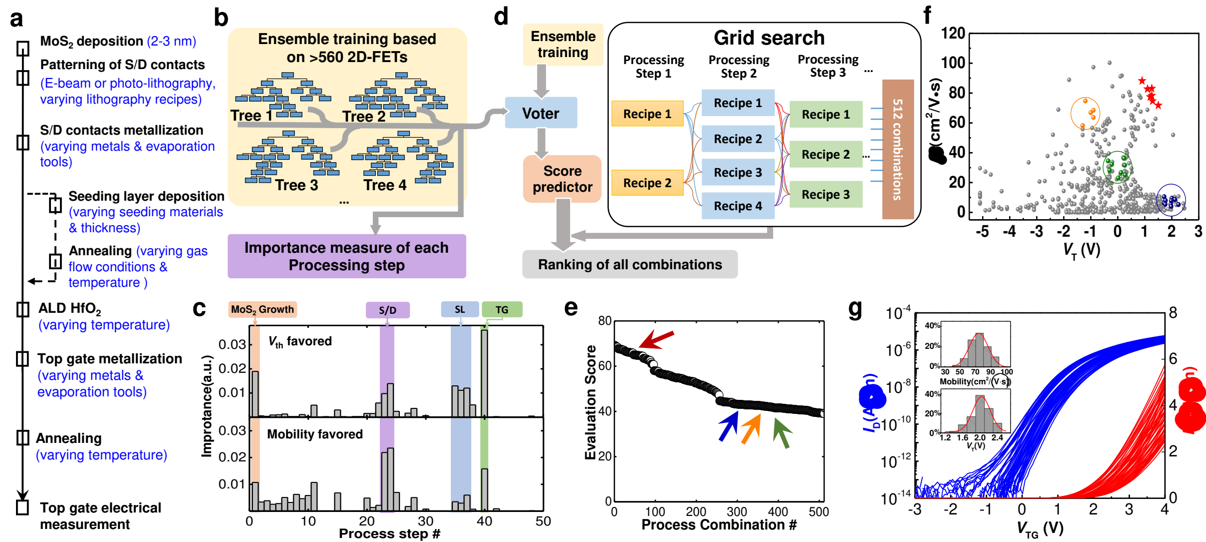


Fig. 2. a, Process flow for fabricating TG MoS_2 FETs. The variations in each step are marked in blue. The end shows a three-dimensional hierarchical structure of an integrated circuit built with gate-last technology. **b,** Graphical representation of ensemble learning based on decision tree algorithm. The importance of each processing step is extracted during the creation of decision trees. **c,** Importance of processing steps for μ and V_T based on random forest regression. **d,** Fabrication co-optimization based on ML. After training with EL, a score predictor can predict the overall device performance for all processing combinations using a grid search method. **e,** Ranking of all possible processing combinations. The high score combinations can be referenced for device fabrication. **f,** More than 500 MoS_2 TG-FETs summarized in a μ-V_T plot. Each color corresponds to one type of processing flow, and the red stars are devices fabricated with the guidance of ML analysis. **g,** Transfer characteristics for 60 MoS_2 TG-FETs on one wafer at V_{DS} = 0.5 V in linear and logarithmic coordinates. The inserts show histograms and Gaussian fits of statistical data for Y-function calculated mobility (upper) and threshold voltage (downside) to Gaussians.

Figure 3

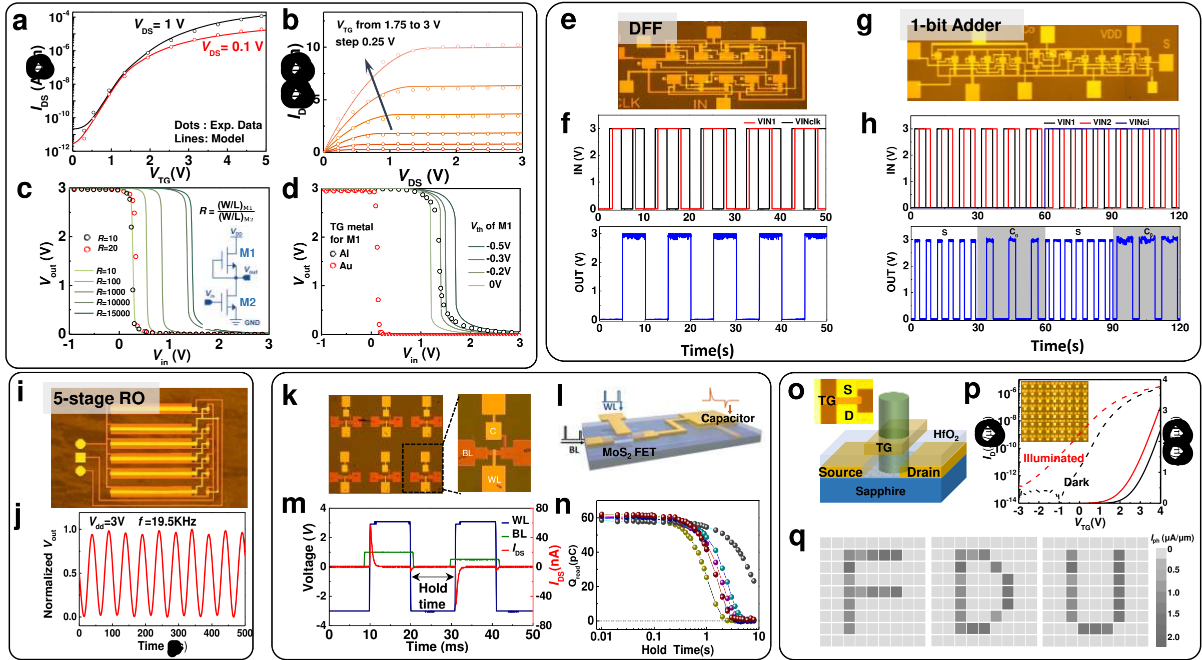


Fig. 3. Experimental data (circular dots) and simulation (lines) for **a-b** transfer and output characteristics of MoS_2 TG-FETs, and **c-d** display VTCs of an MoS_2 inverter with M1 and M2 FETs. The geometry parameter $R = (W/L)_{M1}/(W/L)_{M2}$ is used to adjust the switching point of the VTC curve in **c**, while a different method is used in **d** by independent tuning V_T of M1. **e** shows a photograph of a negative edge-triggered D flip-flop (DFF), and **f** shows the corresponding experimental results. The upper two waveforms are inputs with a 0 to 3 V voltage swing, and the lower graph shows the measured output. **g,** Photograph of a 1-bit full-adder and **h** is the corresponding experimental results. **i,** Photograph of a 5-stage ring oscillator, and **j** is the corresponding output characteristics at 19.5 kHz with V_{DD} = 3 V. **k,** Photograph of MoS_2 memory unit arrays. The zoom-in image shows the structure of a 1T-1C dynamic memory circuit, whose schematic diagram is shown in **l**. **m,** Write and read operations in the 1T-1C unit. **n,** Estimated charge stored in the capacitor as a function of holding time for 5 different devices. **o,** Schematic diagram of an MoS_2 phototransistor with a 10-nm-thick Au top gate, and **p** shows transfer characteristics with and without illumination at V_{DS} = 0.5 V. **q,** Photocurrent mapping for a 9×9 MoS_2 FET array. The photocurrent is produced by scanning the array using a microscope-focused white beam.

Figure 4

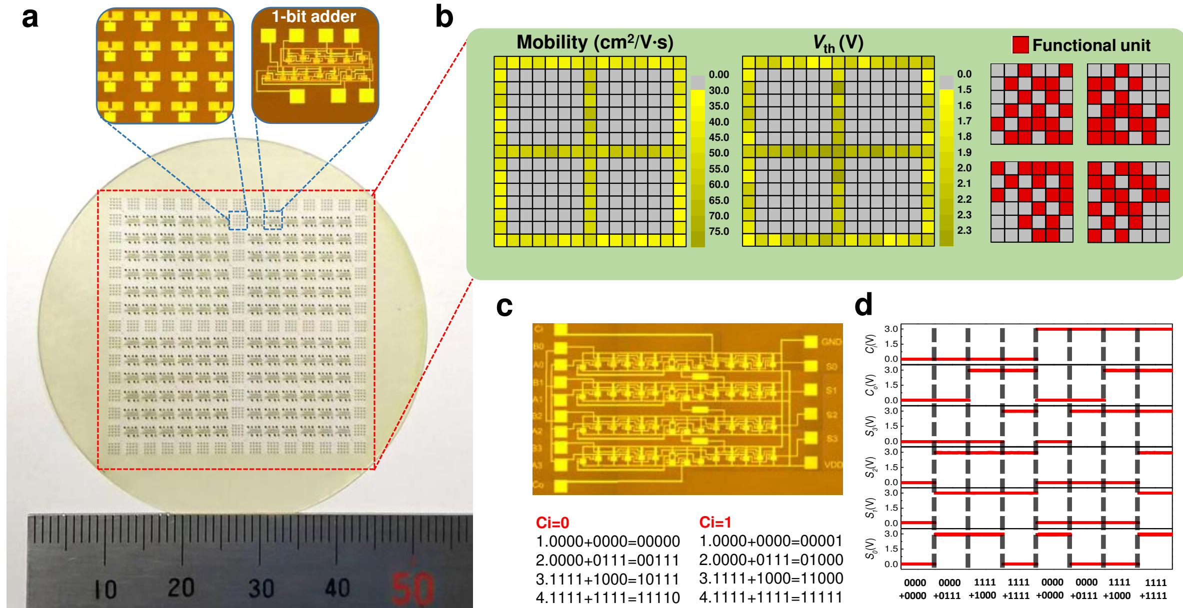
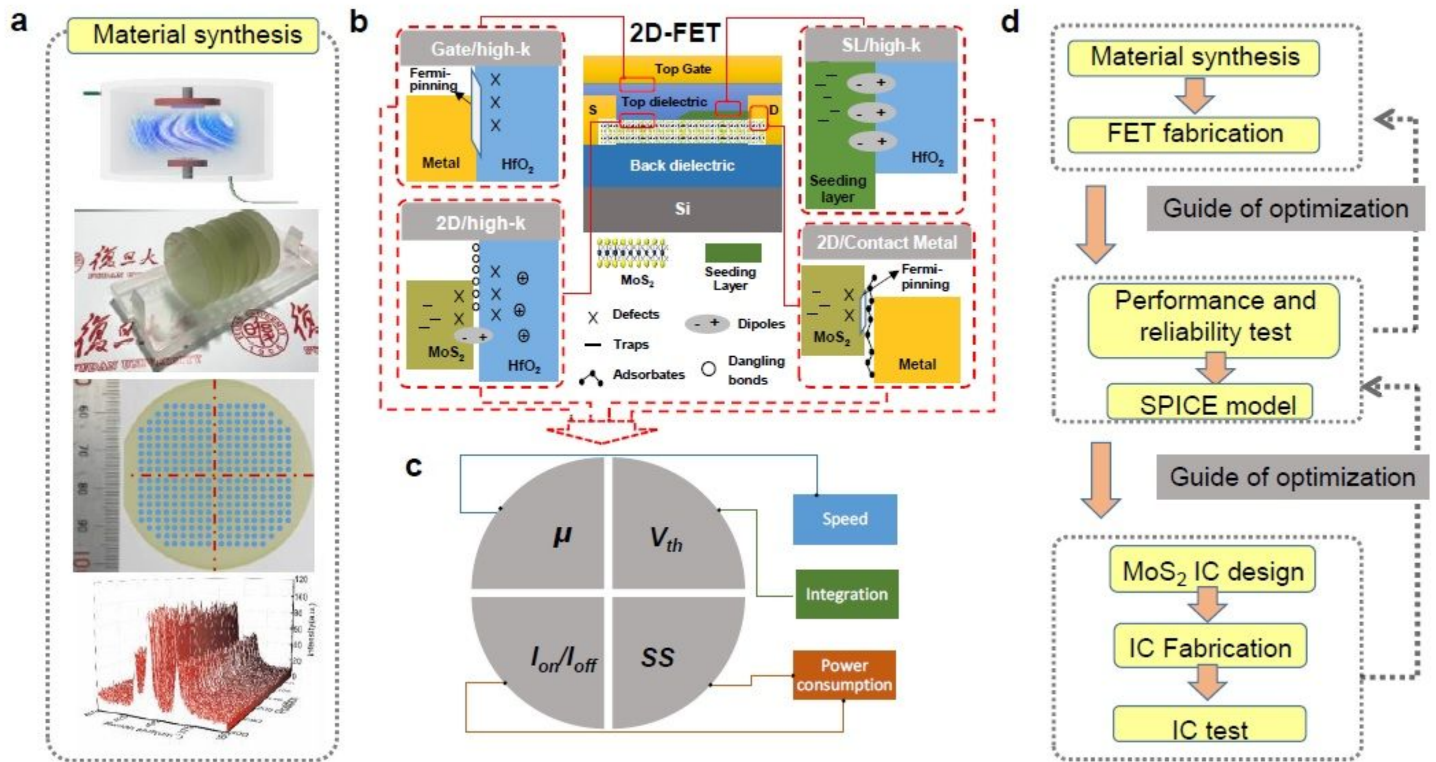


Fig. 4. Wafer-scale integrated circuits built from MoS_2 FETs. a, Photograph of a 2-inch MoS_2 wafer with 1-bit full-adder arrays as functional circuits in the center, and MoS_2 TG-FET arrays used as monitoring devices locating in the surrounding regions. **b,** Wafer maps of mobility (left) and V_T statistics (center) extracted from devices in the surrounding regions. The yellow scale bars show mobility and V_T values. Each block's color scale represents a value averaged from 16 FETs, and the entire wafer has 81 blocks. The right graph illustrates the yield of 1-bit full-adder circuit arrays. The red and gray squares represent the proportion of working and non-working circuits, respectively. **c,** Photograph of a 4-bit full-adder under which is the truth table for logical combinations. **d,** Functional measurements of the 4-bit full-adder with V_{DD} = 3 V. The 4-bit full-adder was tested using a series of input combinations (A, B) in the following order: (0000+0000, 0000+0111, 1111+1000, 1111+1111) with Ci = 0 and Ci = 1.

Figures



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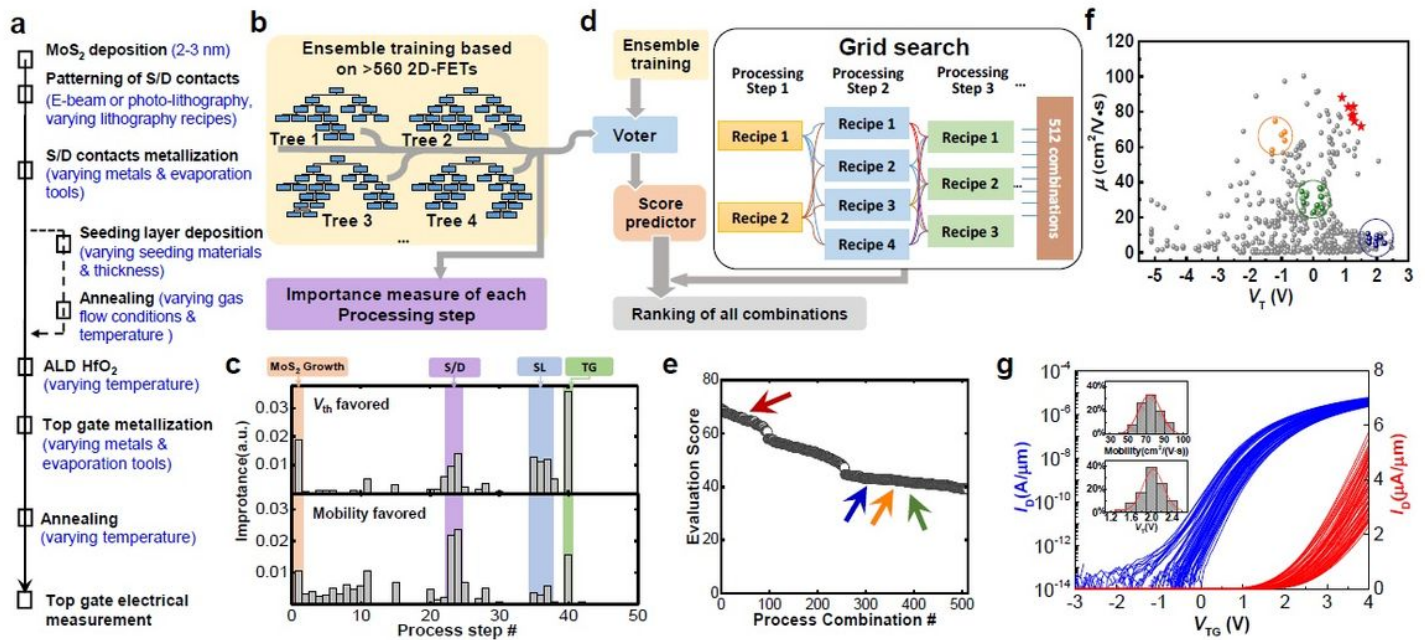

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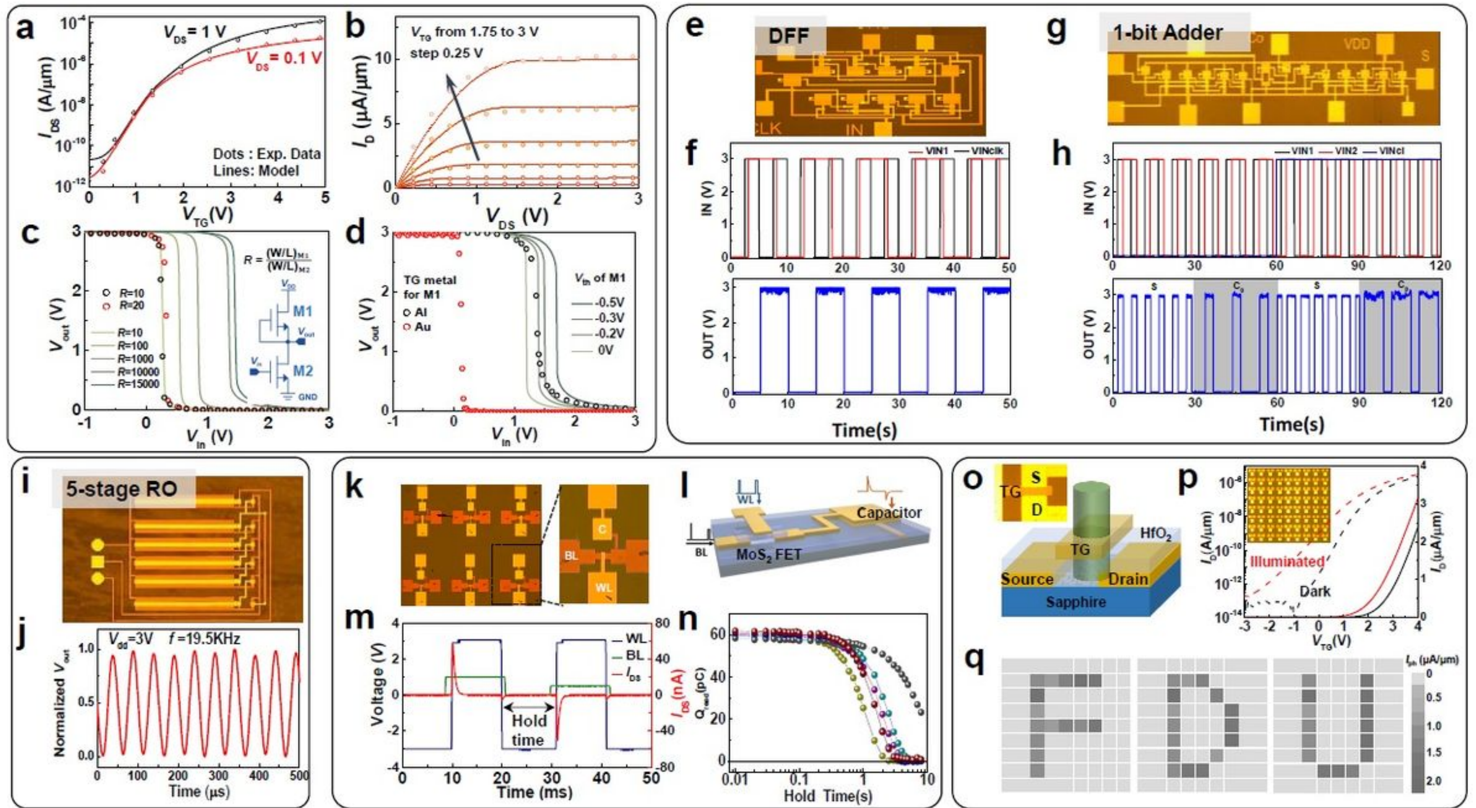

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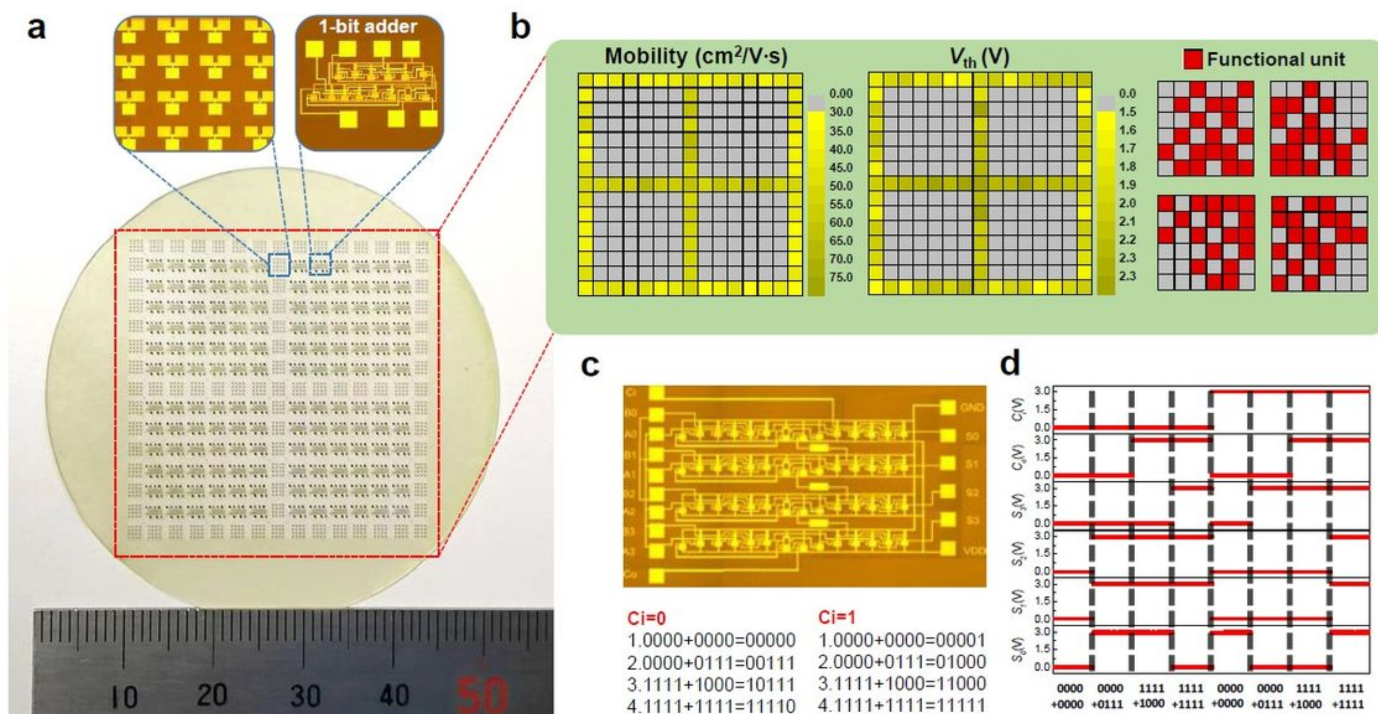

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