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Wavelet Based Fault Analysis in HVDC System

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Abstract—HVDC system has become practically mature over the years but it is still met with some protection issues which should be discussed, for example, the circuit breaker (CB) should be selective to not trip if the transient is temporary, such as overcurrent due to load change. This paper addresses the problem with identifying the type of faults in a HVDC system using wavelet transform (WT). The wavelet transform is proven to be able to capture the distinctive feature of the fault pattern, specifically fault current rising time and oscillation pattern, which are helpful to form a basis for the tripping decision. Three phase-to-ground fault and DC fault are of concern in this paper as their effects are the most detrimental to the system. The point-to-point HVDC system is simulated using PSCAD, and the simulation result is subsequently processed in MATLAB to perform the wavelet transform.

Keywords—AC fault; DC fault; Fault currents; Load change; VSC-HVDC; Rise time; Time-frequency analysis; Wavelet transforms; PSCAD; MATLAB

I. INTRODUCTION

The advancement of power electronic in recent years has paved the way for the practical implementation of HVDC system, in particular voltage source converter (VSC) based HVDC. As people are more conscious of the importance of the distributed energy resources (DERs), multi-terminal HVDC system has to come into play as it facilitates efficient integration of DERs into the grid. Hence, the interest in making the HVDC as future power transmission in addition to the existing AC transmission is fairly promising. However, before we reach that mark, the current HVDC system is still facing several dire protection issues that need to be resolved. Because of that, the HVDC system nowadays can be only restricted to point-to-point link.

This paper aims to investigate pattern of the overcurrent due to different cases, for instance, fault and load change. The understanding of such pattern will be useful in designing a protection strategy, such that the circuit breaker (CB) rightfully trips only should the overcurrent be caused by the fault. The transient caused by the load change is temporary in nature most of the time. In this case it should not send the tripping signal to the CB. The effectiveness of wavelet transform (WT) in identifying and locating the fault has been discussed in detail in these literatures [2, 3]. Thus, the contribution of this work is to extend the application of this powerful signal processing technique to track certain signatures that can differentiate both overcurrent cases.

A HVDC model is constructed and the fault is simulated in PSCAD [4], the results will be subsequently imported to MATLAB [5] for post-processing purpose. As a starting point, a simple model like point-to-point HVDC system (see Fig. 1), which is of interest in this paper, serves as a medium to develop the knowledge on the nature of fault and load change. Gaining concrete understanding on the fault analysis, this work will be extended to multi-terminal HVDC system in future.

The rest of the paper is organized as follows. In Section II, the state-of-the-art of HVDC system is presented, followed by brief introduction of the wavelet analysis in Section III. The HVDC model and fault simulation in this paper are described in Section IV and V respectively. Section VI covers the post-processed result using wavelet analysis in MATLAB. Discussions on the model, result and future work are described in Section VII, and finally conclusion in Section VIII.

II. STATE-OF-THE-ART

DC CB shares the same function as the AC CB but it is commercially known as more expensive equipment. A method has been proposed to avoid using DC CB in a way that the DC fault is fed to the AC side to let the AC CB handle the fault clearance. This method is called the ‘Handshaking method’ [6]. However, as time is one of the critical criteria to be considered in designing a protection strategy, AC CB takes long fault clearing time because of its rigid mechanical restriction.

The relatively low impedance in the HVDC grids is a challenge during a short circuit fault. The fault penetration is much faster and deeper. Fast CBs prevent the collapse of the common HVDC grid voltage. In HVDC, it is required to maintain a reasonable level of voltage for the converter station to operate normally. To protect the converter stations in an optimal manner, it is necessary to clear the fault within a few milliseconds [7].

Some literatures have shown that wavelet-based protection strategy is effectively fast to detect the fault. De Kerf et al. [3] managed to obtain fault detection time as quick as 50 μ s approximately, depending on the fault location. The superiority of wavelet analysis is also highlighted in Murthy’s dissertation [2], whereby the author compared three types of signal processing techniques, including Fast Fourier Transform (FFT), Artificial Neural Network (ANN) and WT. The result proved that WT stands out to be one of the most precise techniques as it is able to detect the location closest to

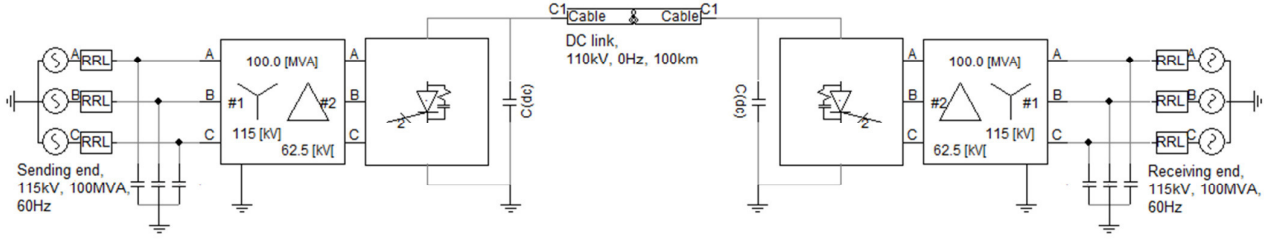


Fig. 1. Two-terminal HVDC system [1].

the exact fault point. Furthermore, Ukil and Zivanovic [8, 9] also discussed the application of abrupt change detection, which is essentially built on WT, in signal segmentation technique in power system, providing automatic disturbance recognition. The work pointed out the advantage of WT that we can utilize in this paper to differentiate the fault and load change.

Wavelet transform allows us to gain the insight into how the signal changes over time and how it can be decomposed into each frequency band over a range of frequencies at the same time. However, the level of precision is subjected to the uncertainty principle; the more precisely the time information is determined, the less precisely its frequency information can be known, and vice versa.

III. WAVELET ANALYSIS

The wavelet transform is a mathematical tool, like Fourier transform for signal analysis. The WT breaks up a signal into the shifted and the scaled versions of the original (or mother) wavelet, allowing for simultaneous time and frequency analysis. In comparison, the Fourier transform uses sinusoids as the basis function, allowing only frequency analysis.

The continuous wavelet transform (CWT) [10] is defined as the sum over all time of the signal multiplied by the scaled and shifted versions of the wavelet function

$$CWT(a, b) = \int_{-\infty}^{\infty} x(t) \psi_{a,b}^*(t) dt \quad (1)$$

$$\psi_{a,b}^* = |a|^{-\frac{1}{2}} \psi\left(\frac{t-b}{a}\right) \quad (2)$$

$\Psi(t)$ is the mother wavelet, the asterisk in (1) denotes a complex conjugate, and $a, b \in \mathbb{R}, a \neq 0$ (\mathbb{R} is a real continuous number system) are the scaling and shifting parameters, respectively. The discrete wavelet transform (DWT) is given by choosing $a = a_0^m$, $b = na_0^m b_0$, $t = kT$ in (1) and (2), where $T=1.0$ and $k, m, n \in \mathbb{Z}$ (\mathbb{Z} is the set of positive integers)

$$DWT(m, n) = a_0^{-\frac{m}{2}} \left(\sum x[k] \psi^* \left[\frac{k - na_0^m b_0}{a_0^m} \right] \right) \quad (3)$$

The multiresolution signal decomposition (MSD) [11, 12] technique decomposes a given signal into its detailed and smoothed versions. Let $x[n]$ be a discrete-time signal, then the

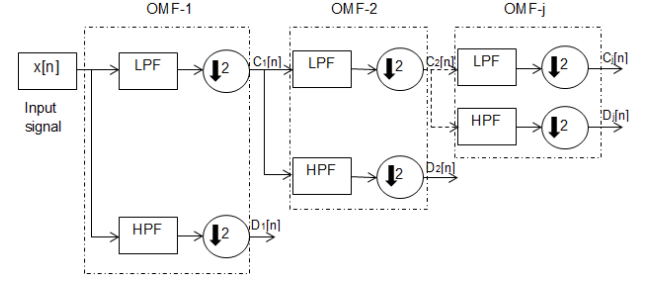


Fig. 2. Multiresolution signal decomposition.

MSD technique decomposes the signal in the form of WT coefficients at scale 1 into $c1[n]$, the smoothed (time-domain view) and $d1[n]$ the detailed (frequency-domain view) coefficients.

The decomposition process can be iterated, with successive approximations being decomposed in turn, so that the original signal is broken down into many lower resolution components. This is called the wavelet decomposition tree [11, 12], shown in Fig. 2. MSD technique can be realized with the cascaded quadrature mirror filter (QMF) [13, 14] banks.

So, for example, using 4-scale decomposition, the original signal s can be represented as

$$s = c_4 + d_4 + d_3 + d_2 + d_1 \quad (4)$$

IV. HVDC MODEL

A. Model Description

Table I. MODEL SPECIFICATION OF SIMULATED POINT-TO-POINT HVDC SYSTEM

Parameter	Value
Steady state frequency	60.0Hz
Rated capacity	100.0MVA
Rated AC voltage (L-L rms)	115.0kV
Rated DC voltage	110.0kV
Sending end transformer ratio (Y/Δ)	115.0kV/62.5kV
Receiving end transformer ratio (Y/Δ)	62.5kV/115.0kV
Switching frequency	33f _o =1980Hz
Cable length	100km
DC capacitor	500μF

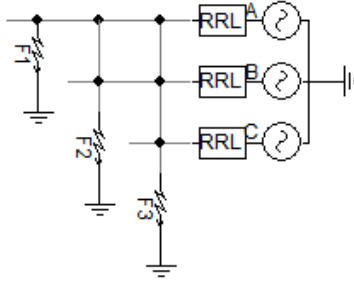


Fig. 3. Three phase-to-ground fault.

A HVDC system rated at 100MVA as shown in Fig. 1 is modeled to transmit 100MW across the DC link from the sending end (rectifier) to receiving end (inverter) using PSCAD. The AC utility is represented as an ideal three-phase AC source behind LR impedance of $26.45e^{j80^\circ}\Omega$. Because of the rectifier action, harmonics in the AC utility requires the implementation of the passive filter. With the pulse width moderation (PWM) technique, in which the odd harmonics are pushed to the edge of high order, the design of filter becomes simple, represented as capacitor in Fig. 1. Moving down the model, the Y/ Δ transformer steps down the voltage to a level suitable for the rectifier. The rectifier and the inverter bridge are the 6-pulse converter made up of gated turn-off thyristors (GTOs), which can be freely turned on and off, based on the cue of firing pulse triggered by control circuit. The role of the large capacitor ($500\mu\text{F}$) across the converter is to eliminate the voltage ripple, ensuring a constant DC voltage (110kV) across the DC link. Since the main concern of this paper is just to observe and understand the response of the system to the different overcurrent cases, the AC CB is absent in this model. The understanding of the overcurrent pattern will be useful in designing the protection logic in future, with that the AC CB will be considered.

B. AC Fault, DC Fault & Load Change

The AC fault case at the receiving end side is shown in Fig. 3. During normal operation, the fault impedance is so large ($100\text{M}\Omega$) that it can be considered as open-circuit. The fault is triggered at 2.1s, lasting for 0.05s, with the fault impedance of 0.01Ω [3]. The only AC fault case discussed in this paper is three phase-to-ground fault. The DC fault is modeled by short circuiting the cable to the ground through fault impedance of 0.01Ω . Likewise, the time of fault is controlled by the block “Timed Fault Logic”, as shown in Fig. 4.

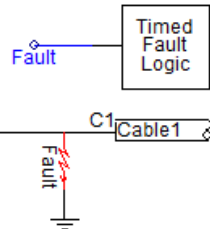


Fig. 4. DC fault.

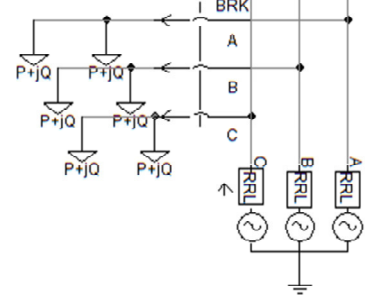


Fig. 5. Load change.

As for load change simulation, it is done by closing the breaker (BRK) at 2.1s, connecting the three-phase loads ($P+jQ$) to the system, as shown in Fig. 5. The size of load is adjusted in such a way that the current rises to the same level as that of AC fault. The reason of doing this way is to allow us to draw a clear comparison of the two seemingly alike overcurrent scenarios, in terms of their rising time and oscillation pattern.

C. Converter Control Strategy

The control strategy is employed differently in the rectifier and the inverter.

1) Rectifier control

The rectifier is controlled to maintain the AC voltage at certain level by changing the modulation index. Firing pulse is generated by comparing the triangular signal ($33f_0$) and the reference signal as determined by the modulation index. The direction and magnitude of the real power can be controlled by varying the phase angle of converter voltage with respect to AC system voltage [1].

2) Inverter control

The inverter is used to control the magnitude and frequency of the AC voltage. Similarly, the modulation index decides the change in the AC voltage of inverter. It is also possible to keep the frequency of AC voltage at fixed level with this controller.

V. HVDC FAULT SIMULATION

The main purpose of this paper is to evaluate the feasibility of wavelet analysis to distinguish the overcurrent cases due to fault and load change. For simplicity, a monopolar two-terminal HVDC transmission system is simulated to observe the distinctive characteristics of the different fault conditions, specifically, the rise time and oscillation pattern, etc. This is of particular interest because in real world, the system should uneventfully maintain continuous service under certain circumstances that might be mistaken for fault, such as load change. As selectivity is one of the vital properties of protection system, without appropriate fault identification, the relay will flag a false alarm to the DC CB, which is highly undesirable in a reliable power system. In our simulation the converter is intentionally made not to block in the event of

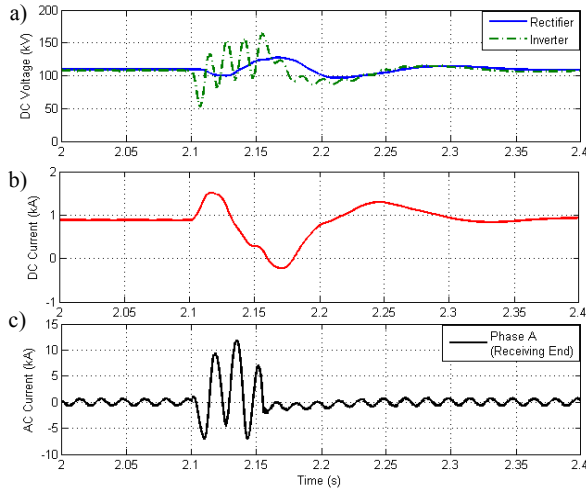


Fig. 6. Simulation result during AC three phase-to-ground fault ($t=2.1s$).

overcurrent, because the main intention is to examine the system response to fault without protection.

PSCAD has limitation in doing the wavelet analysis, therefore, the simulation result obtained will be post-processed using MATLAB [5]. The wavelet transform will provide the ‘smoothed’ (time-domain view) and the ‘detailed’ (frequency-domain view) coefficients [4].

A. Three phase-to-ground Fault

Fig. 6 shows the waveforms of the simulated three phase-to-ground fault at the receiving end. It is clearly observed that the fault inception at 2.1s causes the momentary disturbance to the system. High potential difference between the DC capacitor and fault point leads to increase in DC current, from approximately 0.88kA to 1.5kA in Fig. 6(b), accompanied by drastic decrease in inverter DC voltage, as seen in dotted line in Fig. 6(a). The DC current crosses zero at a point of oscillation before restoring to normal level. It is understandably noted that the inverter DC voltage suffers more profound effect whereas the rectifier DC voltage decreases at rather slower rate. Because the inverter is closer to the fault point, the DC voltage level of the rectifier maintains in a steady manner while the DC voltage of the inverter oscillates significantly. Moreover, the phase A AC current in Fig. 6(c) sees some oscillation as soon as the fault happens. Without proper protection, the current reaches a level, in this case as high as 11.9kA, that can be detrimental to the system. Nearby devices like transformer and converter might be likely to get damaged at this magnitude of current. As this paper mainly concerns on understanding the phenomena of fault in HVDC system, the protection will not be discussed. Since the fault is temporary, the system is seen to recover by itself shortly after the fault is cleared.

Three phase-to-ground fault is commonly recognized as the worst scenario that can ever happen at the AC side of

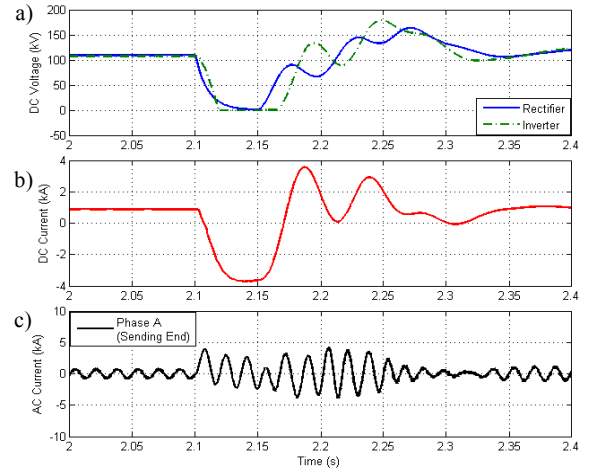


Fig. 7. Simulation result during DC line-to-ground fault ($t=2.1s$).

HVDC system. Most of the time this type of fault, which is likely to cause catastrophic harm, is highly undesirable in real world. Hence, the detection of, particularly, the three phase-to-ground fault has to be fast and precise, which will be discussed in the future work.

B. DC Line-to-Ground Fault

This type of DC fault is applied by short circuiting the cable to ground. The fault lasts for 0.05s and the result is shown in Fig. 7.

It is observed that the DC fault causes the instantaneous DC voltage collapse, and consequently, the power transfer comes to a halt because of the absence of the voltage. During recovery, the DC voltage increases to a level higher than the rated value at a point of oscillation before returning to normal level. The resulting fault current flows in the direction opposite to that of conventional current, which is from rectifier to inverter, and its magnitude increases to about 3.8kA. The impact of DC fault results in a completely different response, apparently even more severe compared with the previous case.

C. Load Change

The size of load is selected so that the DC peak current appears to be the same for both events: fault and load change. Fig. 8 demonstrates the comparison of current changes due to three phase-to-ground fault and load change. A load of power factor 0.97 is needed to achieve the same peak current. One can see that the rate of DC current rising to roughly 1.5kA, in Fig. 8(a), is different for both events; under fault circumstance the peak current rises to the peak 17ms after the fault, whereas the load change takes longer time to reach the same peak. The waveform in Fig. 8(b) also points out that the AC current phase angle is almost constant before fault and begins to change instantly at the fault inception. The phase angle change is observed in the event of load change, but barely noticeable.

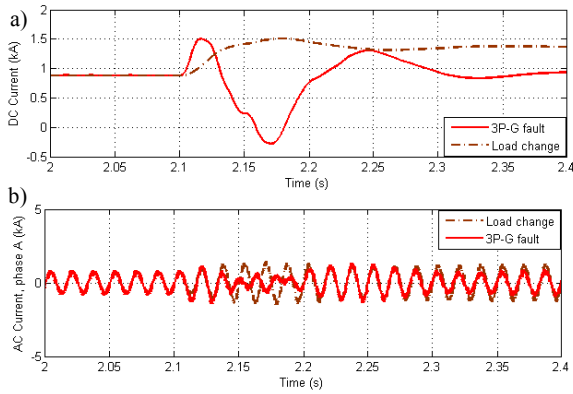


Fig. 8. Simulation result during single phase to ground fault and load change ($t=2.1s$).

This observation is confirmed in literature [14, 15].

Having said that, it becomes clear that the rising time and phase angle can be the indicator to determine the cause of overcurrent. This will be further discussed in following section where the wavelet analysis provides clearer picture - in the time and frequency domain.

VI. FAULT IDENTIFICATION USING WAVELET ANALYSIS

The simulation results obtained from the previous sections are post-processed using the WT algorithm in the environment of MATLAB, as shown in Fig. 9 & 10. The WT generates wavelet coefficient for two cases, three phase-to-ground fault and load change, which allows us to see the change in rising time in clearer manner. Experimenting the wavelet scales ranging from 1 to 7, it is found that decomposition at scale 4 offers adequately fine result.

Fig. 9(a) depicts that the pre-fault wavelet coefficient is almost close to zero, and then several spikes are noticeable between sample number 60 and 130, indicating the occurrence of fault for that duration, and eventually the wavelet coefficient falls back to zero as soon as the fault is cleared. On the other hand, the load change waveform experiences less turbulent change in rising time, which can be explained by the stable trend of wavelet coefficient shown in Fig. 9 (b). Although the change in rising time is inevitable when the current increases, the wavelet coefficient is sufficiently low that it leads us to say that the phenomenon is load change.

Similarly, the DC line-to-ground fault is also investigated using wavelet analysis, as shown in Fig. 10. Under normal operation, the wavelet coefficients are aligned along the x-axis. In other words, the current remains in steady state, therefore the wavelet coefficient is near to zero. A very high wavelet coefficient appears indicating the onset of DC fault. The capability of wavelet coefficient as the solid indicator to detect the abrupt change caused by either fault or load change is proven again.

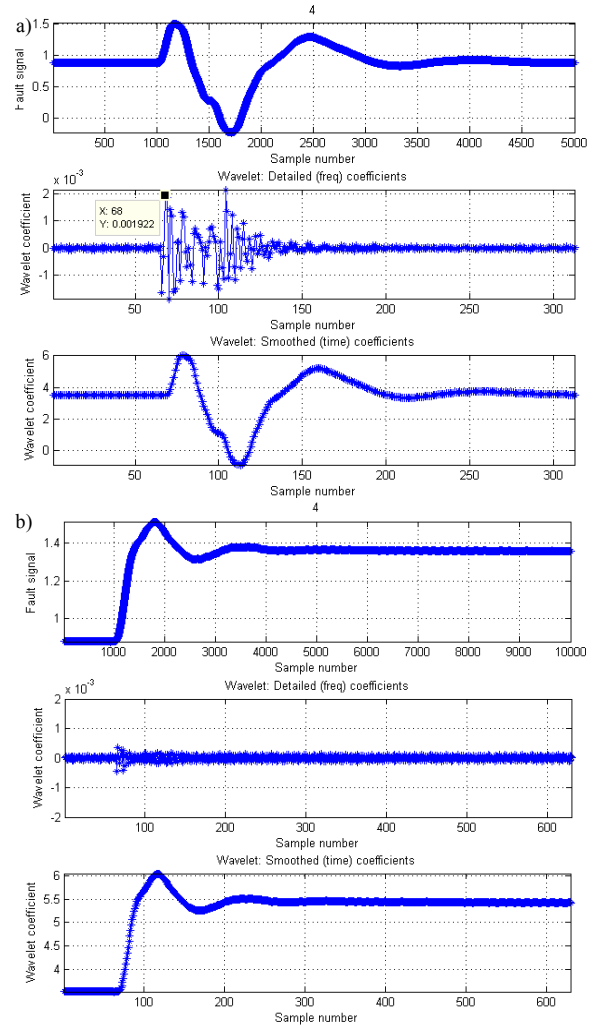


Fig. 9. (a) Wavelet coefficient of DC current (three phase-to-ground fault) and (b) corresponding load change.

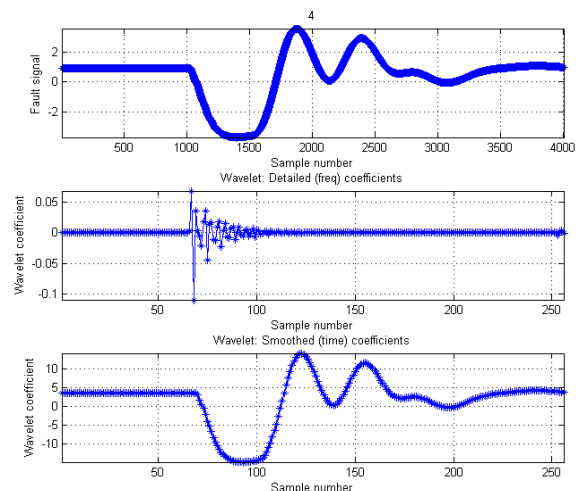


Fig. 10. Wavelet coefficient of DC current (DC line-to-ground fault).

Table II summarizes the observation from Figs. 9 and 10. As much as fault detection time is concerned, the first increase in wavelet coefficient is critical to interpret the type of fault, followed by proper protective action. Considering that the fault happens at 2.1s, simple subtraction from the time where the first wave coefficient peak arises will give the real fault detection time about 4.5ms. From Table II, it can be inferred to say that, as long as the wavelet coefficient is lower than 1×10^{-3} , the overshoot of current is merely caused by the load change and temporary. Hence, it should not be mistaken for fault. Basically fault current experiences rapid rising and hence high wavelet coefficient. However, the threshold value determination for the fault case is not clear-cut. De Keft et al. [3] suggested that multiple simulations are needed to find an appropriate threshold value, in which the worst case situation should form the basis. Having determined the threshold value, we can interpret the fault occurrence when the wavelet coefficient exceeds the threshold at any instant.

Table II. WAVELET COEFFICIENT OF CURRENT

Case	First wavelet coefficient peak ($\times 10^{-3}$)	Time (s)
3P-G Fault (Fig. 9(a))	-1.62	2.1045
Load Change (Fig. 9(b))	-0.4561	2.1046
DC Fault (Fig. 10)	67.550	2.1046

VII. DISCUSSION

In this paper, we have looked into the application of wavelet analysis to establish the distinction between fault and load change. The two-terminal HVDC system used in this paper is the starting point for this study. This research can be further extended for other purposes.

The following comments are cited on the result:

- As Tang and Ooi pointed out in their paper [16], DC fault should produce the fault current with very high rising time than AC fault, because of the huge voltage difference between the DC capacitor and voltage at fault location. This statement is evidently proven by high wavelet coefficient recorded in Table II. The power system should deliver proper protective action to mitigate the AC fault and DC fault in different manner. In former case, there might be a need to involve the tripping of AC CB to eliminate the fault. However, DC fault should be treated differently, given that the operation of AC circuit breaker takes long time, an innovative measure to clear the fault immediately should be introduced. Thus, as much as it is undesirable to confuse AC fault

for load change, it should not happen for DC fault as well.

- This application of wavelet analysis can be further extended to studying the fault in multi-terminal DC (MTDC) system. With multiple sources coming into play, the fault analysis, which becomes increasingly complicated with larger scale meshed HVDC grid, can harness the significant advantages of the proposed approach in this paper. The wavelet analysis should be helpful in understanding how the effect of fault propagates in the DC network so as to decide what appropriate action needed to be taken.
- The wavelet analysis might not be accurate in the presence of harmonics. In this paper, the GTOs are employed for the purpose of AC to DC conversion and vice versa, using the PWM technique. Therefore, the harmonics generated, which are of higher order, can be easily removed by filter. The presence of the harmonics can contaminate the signal if the HVDC system uses line commutated converter (LCC), for instance, the thyristor.
- Fast detection remains the most vital criterion in a protection system. The initial change in the wavelet coefficient that sees the overcurrent is the significant key signature to make decision whether it is fault or load change. In this regard, faults see dramatic increase in the wavelet coefficient whereas the load change has rather stable wavelet coefficient trend. This will be tested in various network configurations in future.
- The threshold value is coupled to the wavelet scale; the smaller the wavelet scale, the lower the threshold value. While the shorter fault detection time can be achieved by using smaller wavelet scale, it has to pay the penalty for low precision because the wavelet spectrum has gotten smoothed out and the appearance of spike (Fig. 9 & 10) will be less sharp. A balance between the detection time and precision should be considered.
- The choice of threshold value is a challenging task. The fault impedance is hardly predictable in practice. With different fault impedance, the DC capacitor sees the voltage difference and therefore, discharges at different rate. In this simulation, the fault impedance is assumed to be constant at 0.05Ω in every fault case. To correctly determine the threshold value, the first-order approximation of the “universal threshold” of Donoho and Johnstone [17] can be applied. Multiple simulations are required to confirm the validity of the threshold value.

VIII. CONCLUSION

We have observed the characteristic of the worst type of AC fault (three phase-to-ground), DC fault and the load change. The simulation results show that the rising time of current can be a key signature that determines the cause of overcurrent. In general, the fault results in steep increase in

current within short rising time. Under load change condition, the current experiences temporary transient, climbing to the peak with relatively longer rising time. This difference can form the logic to duly deliver appropriate protective action. The relay should be sensitive in a sense that it is able to correctly recognize the cause of overcurrent before sending the tripping command to AC CB. The overshoot of current due to load change might be mistaken for fault. In this case it is undesirable to break the circuit.

In this paper, the feasibility of wavelet analysis as a tool to identify the fault is investigated. The fault current is processed with wavelet transform to study its time and frequency component simultaneously. High wavelet coefficient is observed at the time coinciding with the fault inception, which describes the sign of frequency change in fault current; DC fault has highest wavelet coefficient for that matter. In comparison, the load change has rather stable pattern of wavelet coefficient of current, in spite of some barely noticeable variation during the transient period. This investigation will be helpful in developing sensitive and robust protection logic for MTDC system.

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