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Wavy channel transistor for area efficient high performance operation

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We report a wavy channel FinFET like transistor where the channel is wavy to increase its width without any area penalty and thereby increasing its drive current. Through simulation and experiments, we show the effectiveness of such device architecture is capable of high performance operation compared to conventional FinFETs with comparatively higher area efficiency and lower chip latency as well as lower power consumption. © *2013 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4800234]

To enhance the scaling trend of CMOS technology, it is evident that multiple gates and ultra-thin body (UTB) devices are critical technology enabler. Semiconductor giant, Intel Corporation's decision to introduce tri-gate FET for 22 nm node and beyond supports this assertion.[1] Owing to the multiple gates, devices such as the tri-gate (Fin)FET experience a stronger degree of carrier confinement effects leading to mitigated short channel effects—low leakage current (I_{off}), low sub-threshold swings (SS), and drain induced barrier lowering (DIBL).[2–6] This ensures superior operation in the low power regime. At the same time, the drive current is enhanced by the three sides of the FinFET. However, to achieve high performance operation, several fins need to be arrayed with high aspect ratio features. But this solution comes at the expense of increased chip area consumption. This can be alleviated by an extremely tight pitch control, increasing the process complexity and statistical CD variation.[7–13]

To provide an alternate perspective, we report a wavy continuous channel FinFET-like transistor that combines a 2D UTB planar and a 3D fin non-planar architecture of device on an SOI platform. Through simulations and experimental results, we show that compared to conventional FinFETs, the wavy channel transistor is capable of providing an enhanced drive current capability while consuming a lower chip area and providing a relaxed fin-fin pitch. It is to be noted that its most direct use can be in thin film transistor application where we can achieve higher output current without compromising area. Since the performance enhancement comes from device architecture, it is nearly material independent—applicable for both thin film and organic transistors.

Figure 1 depicts the differences in architecture between a wavy channel transistor and a conventional FinFET. Both the devices are on an SOI platform. The advantage of the wavy channel transistor comes from the ultra-thin silicon body between the pitch-area of two consecutive fins. The advantages of the effect of multiple-gates on the 3D fins are still present but now with the addition of several UTB SOI FETs. In the conventional tri-gate FinFET (Figure 1), the total available width for current flow is $W_{FinFET} = n(2W_1 + W_2)$, where n = number of fins. But in the case of the wavy channel transistor, the addition of several ultra-thin bodies translates to an increased width for current flow. Based on Figure 1, the total width is $W_{WCFET} = n(2W_1 + W_2) + (n + 1)W_2$. Consequently, there is a ~1.3× drive current enhancement in the wavy channel transistor over the FinFET as indicated by the equation in Fig. 1 (assume a long-channel device and $W_1 = 4\,W$, $W_2 = W$, $W_3 = 2\,W$). In addition to this, in the wavy channel transistor architecture, the ultra-thin bodies exist within the defined pitch-areas of the fins. As a result, the current enhancement in the wavy channel transistor comes at no-expense to increase in chip area.

In order to understand the benefits of the wavy channel fin architecture, device simulations are carried out using SYNOPSYS TCAD for both device topologies in Figure 1. 3D devices were modeled on an SOI platform with a top silicon thickness of 30 nm and an oxide thickness of 100 nm. The silicon fins have a width of 10 nm. The UTB devices in the wavy channel transistor have a silicon thickness of 5 nm. Both the tri-gate FET and wavy channel transistor utilize a 0.5 nm effective oxide thickness (EOT) hafnium oxide (HfO_2) high-κ gate dielectric with a mid-band gap work function gate metal. Both devices are ⟨100⟩ oriented and have a sharp Gaussian doping profile with a peak concentration of $5 \times 10^{19}\,cm^{-3}$ (Arsenic). The channel is left un-doped in both cases. Carrier transport is handled by the default drift-diffusion model. ***Phillips Unified Mobility Models*** is used in conjunction with a Lombardi model to account for high-k induced carrier mobility degradation. Both devices have a 30 nm gate length (L_g). Quantum confinement effects are handled through the density-gradient based quantization models.[5] Figure 2 compares the simulated non-normalized I_d-V_g performance between the wavy channel transistor and the tri-gate FET. As expected, there is a significant current enhancement (roughly **1.53×**) in the wavy channel transistor. However, this does come at the expense of relatively higher leakage currents and sub-threshold swings. The same ultra-thin silicon bodies responsible for the current enhancement are also responsible for this relative degradation in the leakage characteristics. These thin bodies of silicon are under planar single-gate action at a low L_g. Nonetheless, the wavy channel transistor manages a large on-off current ratio ($>10^5$) and a SS of 76 mV/dec. A larger current enhancement is possible if high aspect ratio fins are utilized in the wavy channel transistor.

From Figure 1, it was emphasized in the previous paragraph that the wavy channel architecture provides the current

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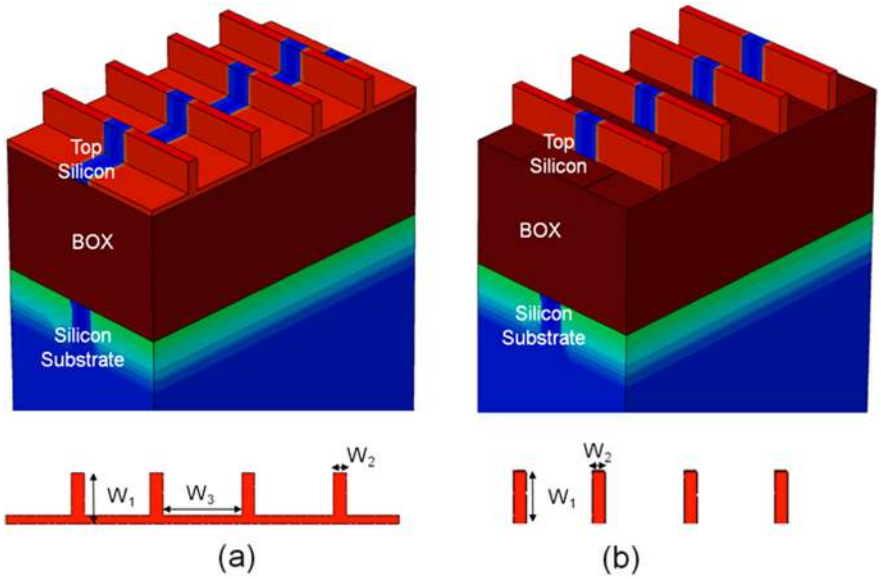

FIG. 1. Schematics of wavy channel transistor (a) and standard FinFET (b).

$$\frac{I_{WCFET}}{I_{FinFET}} = \left(\frac{\mu C \left(\frac{W_{WCFET}}{2L} \right) (V_g - V_t)^2}{\mu C \left(\frac{W_{FinFET}}{2L} \right) (V_g - V_t)^2} \right) \sim 1.3$$

enhancement without additional chip-area consumption. This is because the ultra-thin bodies that contribute to the width enhancement are defined in the existing pitch areas between the fins. To put it in a different perspective, if we consider Figure 2, the non-normalized output drive current (I_{FinFET}) from the conventional FinFET with 4 fins is approximately 0.12 mA. For the wavy channel FET with 4 fins and 5 UTBs (3 within the pitch areas and 2 at ends), the non-normalized output drive current (I_{WCFET}) is ~0.2 mA giving it ~1.6× improvement in drive current. A simple analysis shows that in the FinFET device the drive current per fin is 30 mA. So to have the same current output as the wavy channel transistor, we need an additional 7 fins (0.2 mA/30 μA). In Figure 3, where "p" and "L" denote the fin-fin pitch and the combined source, drain, and channel length, respectively, the total chip-area consumed by the wavy channel transistor is $A_{WCFET} \sim 5p \times L$. To achieve the same current enhancement as the wavy channel transistor, the FinFET has to accommodate an additional 7 fins. So the effective chip-area consumed by the FinFET is: $A_{FinFET} \sim 12p \times L$. Taking the ratio of the two areas (A_{WCFET}/A_{FinFET}) indicates that the wavy channel FET occupies just 40% of the larger 7 fin conventional FinFET. So, if a conventional FinFET was to operate at a performance level similar to the wavy channel transistor, it would require a larger array of fins translating to an increased chip area. This results in increased RC delays and power consumption. Using the equations, in Figure 3, a 4 fin wavy channel transistor will be 4× faster than a 7 fin tri-gate FinFET. The simple equations relating area and power consumption (P) indicates that the smaller and faster 4 fin wavy channel transistor will use just 25% of the power consumed by that of the larger 7-fin tri-gate device. One might argue that the area for the larger FinFET could be controlled by a tighter pitch control of the fins. But this comes at the expense of increased process complexity and higher statistical CD variation of the fins. In addition to this, arraying has an additive effect on the off-state leakage current as well as increase in SS and other short channel effects.

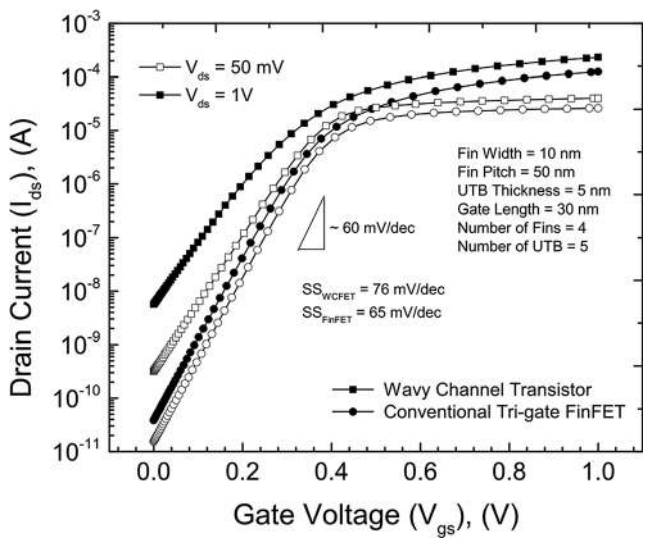

FIG. 2. Simulated transfer plot (I_d-V_g) for performance comparison between wavy channel transistor and conventional FinFET.

In order to verify the practical implication of the wavy channel transistor for thin film transistor application, polycrystalline silicon based wavy channel transistor and FinFETs were fabricated. Figure 4(a) shows the process involved in fabricating these devices. The difference in the FinFET process step is the exclusion of the second step. The wavy channel transistor and FinFET devices have fin heights of 50 nm and 70 nm, respectively. The wavy channel transistor has UTB thicknesses of ~15 nm. In both devices, the fins have a width of 2 μm with a gate length of 100 μm. All thickness measurements were confirmed by spectroscopic ellipsometry and atomic force microscopic (AFM) scans.

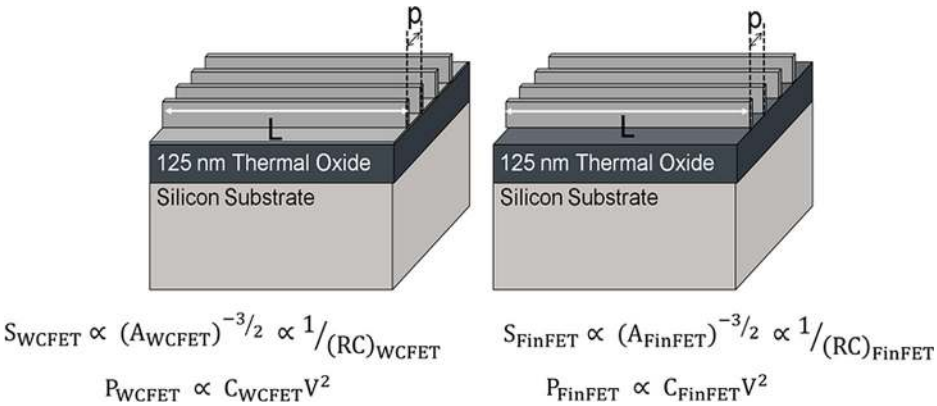

FIG. 3. Chip area efficiency, speed, and power comparison between wavy channel transistor (left) and FinFET (right).

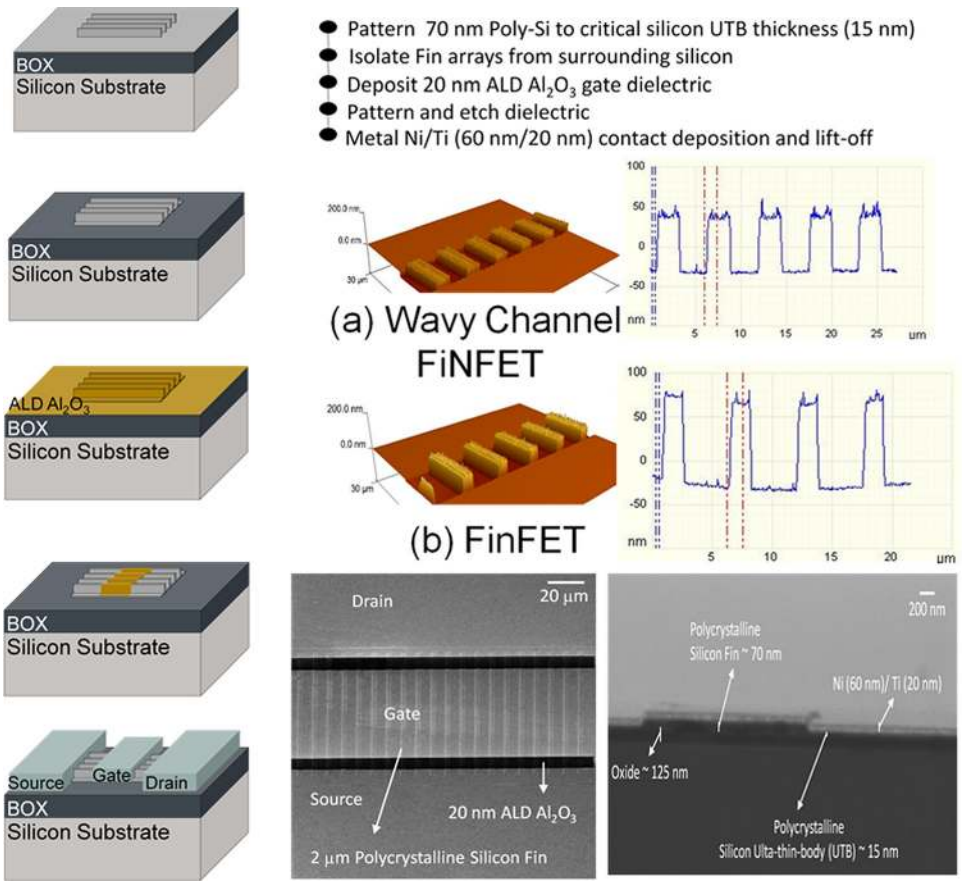

FIG. 4. (a) Process flow for wavy channel transistor. It is to be noted that standard FinFET fabrication process will avoid the second step (isolating fins from surrounding silicon); (b) scanning electron microscopic (SEM) and AFM images of fabricated wavy channel transistor.

These relaxed conditions were utilized to observe benefits of a higher drive current due to the additional UTBs in the wavy channel transistor. Both devices have an array of equal number of fins with a pitch (UTB width) of 2 μm. Figure 4(b) depicts top down scanning electron microscope images and an AFM scan of the wavy channel transistor. No-doping was incorporated in either device. Schottky barrier contacts were utilized in both cases. Figure 5(a) shows the rudimentary I_d-V_g performance of the FinFET and wavy channel transistor, respectively. Nonetheless, several observations can be made based on Figure 5(b). For a drain voltage (V_d) of 5 V, it can be observed that an almost **4×** higher output current is observed in the wavy channel transistor compared to the FinFET for a 2-5 V gate voltage (V_g) sweep. This shows the competitive advantage of having the wavy fin architecture.

It is to be noted that thinner fin widths (<20 nm) in the wavy channel FinFET enable stronger gate control, resulting in lower off-state leakage (higher on-off current ratio), short channel effects (DIBL, V_t roll-off), and SS. Thinner ultra-body thicknesses within the fin-pitches lead to lower off-state leakage, SS, and short channel effects. Increasing the pitch width (UTB width) will provide higher output current. A unique feature of the wavy channel FinFET is the multi-V_t switching capability to allow on-demand switching between low power and high performance. This can be achieved by varying the pitch widths as required to achieve desired V_t (see Supplementary Figure S1).[14]

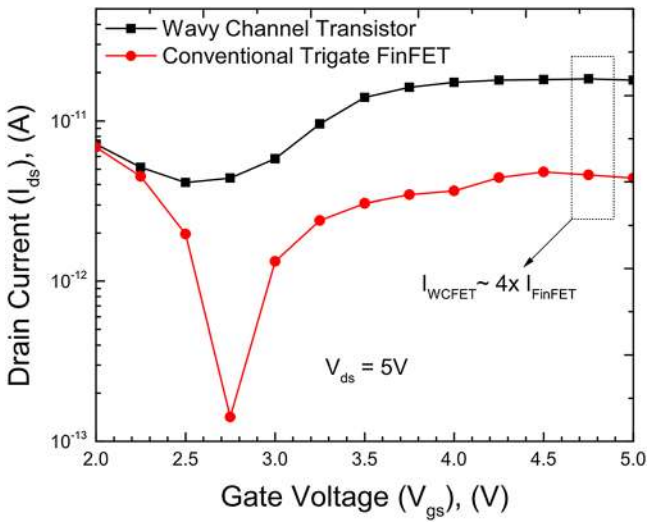

FIG. 5. Experimental I_d-V_g performance comparison between 100 μm gate length wavy channel transistor and conventional FinFET. Wavy channel transistor has 15 nm thin polycrystalline silicon ultra-thin-body (UTB) lateral channel portion in between vertical channel portions. Fin width and pitch are both 2 μm. Low I_{on}/I_{off} ratios are mainly because of poor gate control in ultra-wide fins as well as the lack of source/channel and drain/channel junctions.

We have reported the concept of a wavy channel transistor. Through simulations and experimental results, we have demonstrated that this architecture utilizes otherwise wasted pitch-areas in SOI based FinFET devices to achieve relatively higher performance compared to traditional FinFET devices while achieving high-chip area efficiency, higher chip-speed, and lower power consumption. Its advantage can be used for thin film transistor based applications where often large area electronics are integrated with both thin film and organic materials.

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[14]See supplementary material at http://dx.doi.org/10.1063/1.4800234 for the pictorial depiction of the impact of fin width versus the thickness of the body at the base on the device performance.