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Wear-out Condition Monitoring of IGBT and MOSFET Power Modules in Inverter Operation

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***Abstract*— In this paper, a condition monitoring system for the degradation assessment of power semiconductor modules under switching conditions is presented. The proposed monitoring system is based on the online measurement of two damage indicators: the on-state voltage of the semiconductor and the voltage drop in the bond wires. The on-state voltage of a semiconductor can be employed for temperature estimation, in order to anticipate failures in the solder joints that increase the thermal resistance of the cooling path. Moreover, by measuring the voltage drop in the bond wires, the degradation of the bond wires can be detected. The described monitoring system has been implemented in an inverter prototype, and tests have been performed in different scenarios to verify its capabilities in healthy and degraded states. Furthermore, a monitoring routine has been proposed in order to perform the required measurements in high switching frequency applications.**

***Index Terms*—Condition Monitoring, Fault diagnosis, Bond wire fatigue, Solder Fatigue, Switch Power Modules, Semiconductor device reliability**

I. Introduction

In the last decade, a huge effort has been made by the semiconductor industry to improve the performance of wide-bandgap (WBG) semiconductor devices in order to make them commercially available. This is due to the potential benefits that these materials have over regular silicon (Si) devices, resulting in smaller converters while maintaining high efficiency [1], [2]. However, in those applications in which lifetime is a design constraint and high reliability is required, designers still tend to choose Si rather than WBG devices. The reason is the lack of information about the ageing process of WBG modules under long-term operating conditions.

In order to deal with the wear-out process of the modules and the uncertainties of WBG semiconductors, condition monitoring of these devices plays a major role [3], [4]. The monitoring of the degradation enables the implementation of different solutions, such as condition-based maintenance [5] or degradation rate reduction by means of active thermal control [6]–[8], in order to avoid the failure to extend to other parts of the converter.

In medium-power operation, semiconductor chips are packaged in modules in order to increase their power density and improve their thermal behaviour. Experience from IGBT modules supports that failures related to the package, usually associated with wear-out processes, are the limiting factor for long-term reliability [9].

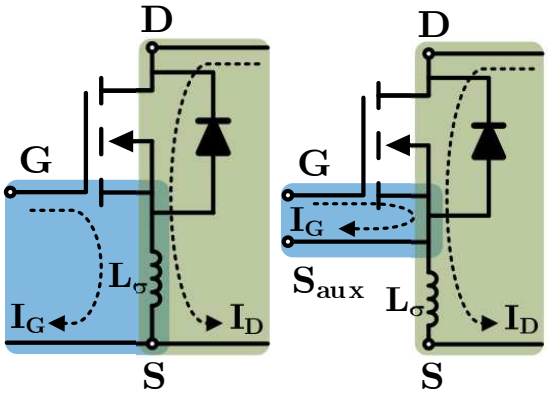


Fig. 1: Accesible terminals in MOSFET switches (Blue – Control loop and Green – Power loop). (a) Control and power loops coupled through the common source inductance. (b) Decoupled control and power loops.

The current trend in modules for switching devices is to decouple power and control loops by separating their external connections. In the case of MOSFETs, this is done separating the available source connections: one for the current that flows across the drain and to the load/DC-Link, known as the power source, and an extra source terminal for the control loop, referred to as auxiliary source, employed for the gate driver and protection circuits. The same principle can be applied to IGBTs, separating the emitter connection in auxiliary and power emitters. A comparison of the available solutions is shown in Fig. 1, where it can be seen that the parasitic source inductance L_σ caused by the package is not shared between control and power loops when the auxiliary source connection is available. By doing this, the driving voltage is not influenced by the voltage drop in the parasitic inductance, hence improving the switching and reducing the losses [10]. Moreover, it can reduce the appearance of parasitic turn-on events [11]. These improvements are specially relevant in WBG devices due to their faster switching capability and

consequently higher $\mathrm{d}i/\mathrm{d}t$ and $\mathrm{d}v/\mathrm{d}t$.

Since the early stages of the condition monitoring of semiconductor devices, the V_{DS} (or V_{CE} in the case of IGBTs) at certain load current has been widely employed as a damage indicator [12]–[14]. The reason is that, between the power connections of each switch, not only the on-state forward voltage of the device under test (DUT) chip is embraced, but also the voltage drop in the bond wires caused by the circulating current [12], as shown in Fig. 1(a). Hence, a failure in the bond wires is reflected in the V_{DS} as a sudden increase, as shown in the results of [13]. However, the on-state saturation voltage of the switches is not only current-dependent, but also temperature dependent, and hence it is influenced by other possible failure mechanisms such as solder joints degradation [15]. This complicates its use as a damage indicator for condition monitoring. By contrast, in those modules in which a separated auxiliary source connection is available [as in Fig. 1(b)], it is possible to decouple the measurement by monitoring both $V_{\mathrm{DS_{aux}}}$ and $V_{\mathrm{S_{aux}S}}$. This way, the failure effects of the main failure mechanisms can be separated and hence monitored independently. Although the possibilities of this novel monitoring system have recently been studied as a proof-of-concept in [16], its performance must be validated under switching operation in order to be employed widely.

In this paper, a complete monitoring system conceived for single-chip power modules with an auxiliary-source conexion available operated under switching conditions is presented. Here, the monitoring principle is studied for a 1200-V SiC MOSFET power module operated as an inverter, and the sensitivity of the measurement parameters against failures is analyzed.

First, in Section II, the common failure mechanisms of SiC power modules are described along with their effects. After that, the test platform is introduced and the proposed condition monitoring system is presented in Section III. With the described platform, tests have been performed in three different scenarios in order to prove its accuracy and aptitude to detect the degradation of the module. The results are shown in Section IV, along with the measurement routine employed to perform measurements in devices switching at high frequency. At the end, previous sections are summarized in the form of conclusions in Section V.

II. SiC Power Module Failures

A. Dominant Failure Mechanisms

In order to develop a condition monitoring system, the first step is to identify the most relevant wear-out failure mechanisms of the device under study. Unlike catastrophic failures, which are caused by single-events, wear-out failures occur in a degradation process that can be anticipated. In this paper, the DUT is a wire bonded SiC MOSFET power module, specifically the CCS020M12CM2 from Wolfspeed, rated at 1.2-kV/20-A. This module consists on three half-bridge branches, each composed by two MOSFETs and two antiparallel diodes, packaged in a 45-mm wire-bonded module, with the layout shown in Fig. 2(a).

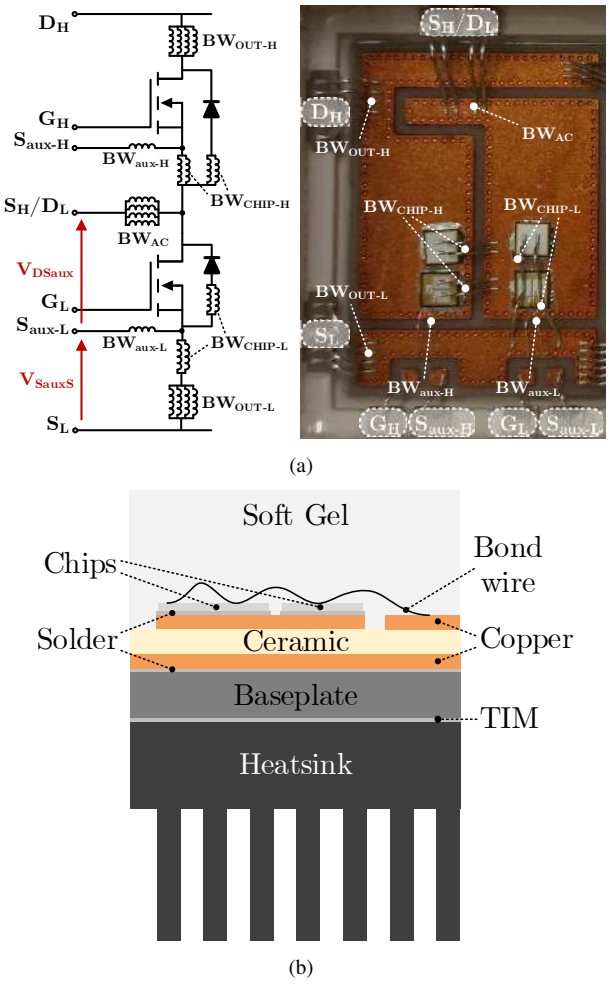


Fig. 2: Packaging structure of the DUT: (a) Internal layout of the monitored module. (b) Cross-sectional view of wire-bonded semiconductor module.

In [17], bond wire liftoff and solder fatigue are identified as the dominant failure mechanisms for wire-bonded IGBT modules. Since the packaging of SiC MOSFET and Si IGBT wire-bonded power modules is the same, similar failure mechanisms can be expected. The typical cross-sectional view of a wire-bonded power module, is illustrated in Fig. 2(b).

As described in [18], bond wire liftoff occurs as a fatigue process in the interfaces between bond-wire and chips. The power losses and the unequal Coefficient of Thermal Expansion (CTE) of the chip and the bond wires induce thermomechanical stress that ends up with the lift-off of the bond wire. Given the layout shown in Fig. 2(a), this results in a sudden increase of the resistance of the bond wires $\mathrm{BW_{CHIP_L}}$, which is reflected in a higher voltage drop between auxiliary source and power source connections $V_{\mathrm{S_{aux}S}}$ when there is a circulating current through the DUT.

Regarding solder fatigue, a similar process takes place in the interfaces chip-copper and copper-baseplate. In this case, the degradation causes cracks in the materials that degrade the

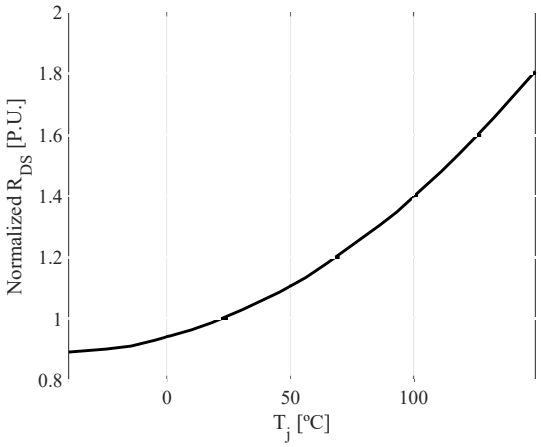


Fig. 3: Dependence of $R_{\mathrm{DS,on}}$ with T_{j} at V_{GS} = 20 V and I_{D} = 20 A [21].

heat cooling path, increasing its thermal resistance [19]. The thermal resistance of a module can be determined as:

$$R_{th_{j-a}} = \frac{\Delta T_{j-a}}{P_{Loss}} \tag{1}$$

This way, for the same power losses P_{Loss}, the temperature difference between junction and ambient $\Delta T_{\mathrm{j-a}}$ is expected to be higher after solder fatigue.

For SiC MOSFETs, a higher junction temperature is reflected in an increase of the on-state resistance R_{DS} [20]. This is confirmed by the device datasheet [21], shown in Fig. 3, in which the normalized variation of R_{DS} with the junction temperature is plotted. This makes it a suitable Temperature Sensitive Electrical Parameter (TSEP) for junction temperature estimation. In order to accurately estimate the junction temperature, a calibration of the $R_{\mathrm{DS_{aux}}} - T_{\mathrm{j}}$ would be required. This could be carried out by externally heating the module to certain temperature, such as in [22], while monitoring $R_{\mathrm{DS_{aux}}}$.

Besides these package-related failures, several investigations have studied device specific failure mechanisms of SiC MOSFETs like gate oxide degradation [23]. This failure mechanism is caused by the high defect density in these devices [24], and is accelerated by temperature and bias voltage. In [25], results of Accelerated Life Test High Temperature Reverse Bias (ALT-HTRB) from WolfSpeed are reported for a 1200 V SiC MOSFET at 150 °C. The predicted lifetimes resulted on over 10^7 hours at 960 V drain stress and over 10^8 hours at 800 V, and the identified failure mechanism was occurring in the gate oxide. Although these figures vary for different device breakdown voltages, this reflects that technology advancements have reduced the influence of gate oxide degradation.Hence, the monitoring system proposed in this paper is only intended to detect package-related failures, which are common to IGBT and MOSFET power modules.

B. Failure detection decoupling

In the module layout presented in Fig. 2(a), the two available source connections S and S_{aux} of each active switch can be distinguished. From this, the classical condition monitoring signal V_{DS} for the low side switch can be expressed as

$$V_{DS}\left(I_D, T_j, R_{BW}\right) = V_{DS_{aux}}\left(I_D, T_j\right) + V_{S_{aux}S}\left(I_D, R_{BW}\right) \tag{2}$$

where I_{D} refers to the drain current, T_{j} to the junction temperature of the chip and R_{BW} to the bond wire resistance.

As introduced before, if V_{DS} is employed as a damage indicator, a drift in the measurement could be rather the consequence of a bond wire lift-off or a temperature increase due to solder fatigue. However, when an auxiliary source connection is available, the measurement of $V_{\mathrm{DS_{aux}}}$ and $V_{\mathrm{S_{aux}S}}$ could be done independently. This way, the measurement of $V_{\mathrm{DS_{aux}}}$ can be defined as

$$\begin{aligned} V_{DS_{aux}}\left(I_D, T_j\right) = V_{DS_{CHIP}}\left(I_D, T_j\right) + I_D\, R_{BW_{AC}}(T_{BW}) \\ + I_G\left(R_{BW_{AC}}(T_{BW}) + R_{BW_{aux_L}}(T_{BW})\right) \end{aligned} \tag{3}$$

where I_{G} refers to the current coming from the gate driver, T_{BW} refers to the temperature of the corresponding bond-wire and the monitoring system and the bond wire resistances are named as in Fig. 2(a).

Concerning $V_{\mathrm{S_{aux}S}}$, it depends on the circulating current and the state-of-health of the bond wires, which is translated to its electrical resistance. Then, it could be expressed as:

$$\begin{aligned} V_{S_{aux}S}\left(I_D, R_{BW}(T_{BW})\right) = I_G\, R_{BW_{aux_L}}(T_{BW}) \\ + \left(I_D + I_G\right)\left(R_{BW_{CHIP_L}}(T_{BW}) + R_{BW_{OUT_L}}(T_{BW})\right) \end{aligned} \tag{4}$$

Indeed, the current I_{G} in a MOS device can be considered as zero after the switching has been completed. Therefore, (3) can be rewritten as

$$V_{DS_{aux}}\left(I_D, T_j\right) = V_{DS_{CHIP}}\left(I_D, T_j\right) + I_D\, R_{BW_{AC}}(T_{BW}) \tag{5}$$

and $R_{\mathrm{DS_{aux}}}$ results in:

$$R_{DS_{aux}}\left(T_j\right) = R_{DS_{CHIP}}\left(T_j\right) + R_{BW_{AC}}(T_{BW}) \tag{6}$$

been $R_{\mathrm{DS_{aux}}}$ only dependent on the junction temperature of the DUT and independent of the bond wires.

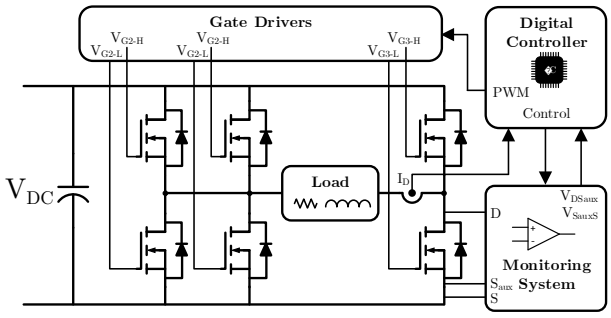
On its behalf, (4) is rewritten as

$$V_{S_{aux}S}\left(I_D, R_{BW}\right) = I_D\,\left(R_{BW_{CHIP-L}} + R_{BW_{OUT-L}}(T_{BW})\right) \tag{7}$$

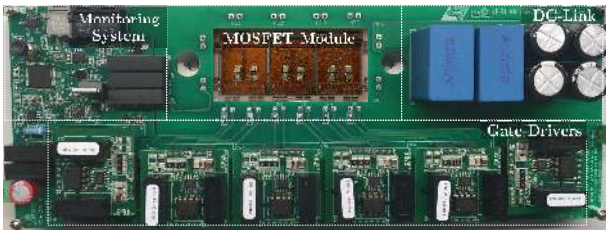
depending only on the circulating current and on the state-of-health of the bond wires. Regarding T_{BW}, resistance increases below 20% have been reported in [26]. However, a higher resistance increase is expected after a bond wire collapse, and hence its effect on the failure detection is reduced.

III. Test Platform

In this Section, a description of the platform employed to validate the monitoring system will be performed. This includes the specifications of the prototype employed and the characteristics of the monitoring system. Moreover, the procedure to emulate the failures to verify the capabilities



(a)



(b)

Fig. 4: Overview of the designed prototype. (a) Functional diagram. (b) Detailed picture.

of the system in both healthy and degraded states will be presented.

A. Inverter Setup

In order to validate the performance of the monitoring system in realistic switching conditions, the module presented above has been employed to develop an inverter [27]. Fig. 4(a) shows the implemented setup: a full bridge inverter with two paralleled legs, with the DUT located in the third leg.

A digital controller (DSP TMS320F28335 from TI) has been employed to generate the driving signals for the switches and to implement the monitoring system for collecting the measurements. Commercial gate drivers, a DC-Link capacitor and an air-cooled heatsink were selected to meet the desired performance. A picture of the designed prototype is presented in Fig. 4(b), and its specifications are collected in Table I.

B. Monitoring System

The monitored voltages are sampled by a 16-bit ADC with a ± 5 V range, resulting in a resolution of 0.15 mV. In order to avoid noises and errors in the measurements, special attention has been paid to the placement and routing of the monitoring circuits, with the S_{aux} connection as the ground of the monitoring system. The captured data are transmitted through fibre optics to the digital controller of the system. Finally, the data are forwarded to a CPU via RS-232. In addition, an external current transducer is employed to measure the circulating current. A schematic of the monitoring system is given in Fig. 5, where the measurement circuits for $V_{\mathrm{DS_{aux}}}$ and $V_{\mathrm{S_{aux}S}}$ are shown.

TABLE I:
PROTOTYPE SPECIFICATIONS [27].

Full Bridge Inverter	
DC-Link Voltage	600 V
DC-Link Capacitance	49 μF
Maximum Output Power	4 kW
Power Factor	0.99
Output Frequency	50 Hz
Modulation Strategy	Sinusoidal Bipolar PWM
Cooling System	Forced-Air Cooled Heatsink

The measurements are synchronized with the PWM signals generated in the digital controller. This way, measurements are triggered after the turn-on of the DUT. At that time, the start of conversion signal is sent to the ADC, and the output voltage of the current transducer is captured. The employed ADC acquires the monitored voltages through track-and-hold amplifiers, which sample the input voltage at the rising edge of a start of conversion signal. Hence, the monitored voltage is the instantaneous voltage when the start of conversion signal is received.

1) $V_{\mathrm{DS_{aux}}}$ measurement circuit:

The $V_{\mathrm{DS_{aux}}}$ measurement circuit, shown in Fig. 5, is based on the online V_{CE} measurement method presented in [28]. This circuit, based on the desaturation protection circuit of power semiconductors, consists of two diodes placed in series and forward biased with a current source and an analog circuit with unitary gain. In order to reduce measurement errors, the use of thermally coupled diodes when possible is suggested. Otherwise, it is recommended to employ discrete diodes from the same batch and similar characteristics. While during the on-state of the DUT, the current flows through the diodes and the power semiconductor, during the off-state the diodes block the DC-Link voltage and protect the rest of the system. Nevertheless, the complexity of this circuit limits the measurement speed of the system, since it takes a while for the current source to set the output current, forward bias the diodes and for the amplification circuit to have an stable output. Hence, a minimum settling time has to be ensured which might constraint the maximum switching frequency of the DUT.

2) $V_{\mathrm{S_{aux}S}}$ measurement circuit:

Regarding the measurement circuit of $V_{\mathrm{S_{aux}S}}$, it is connected between the auxiliary source S_{aux} and the power source S of the DUT. In this case, as presented by (7), this voltage is the voltage drop across the bond wires, hence there is no need for blocking high voltages when the device is in the off-state. Therefore, this voltage can be measured with an instrumentation precision amplifier. The simplicity of this measurement circuit implies that it requires less time to have an stable measurement.

C. Failure emulation

In order to verify that the system is able to detect the degradation of both failure mechanisms, its performance must be tested in both healthy and degraded states. Hence, the

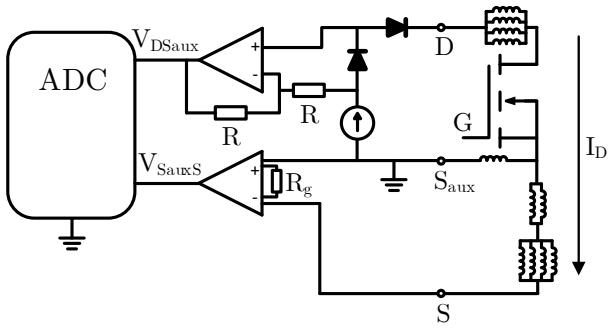


Fig. 5: Circuit implementation of the monitoring system.

effects of the described failure mechanisms must be replicated, which should be reflected in the monitored voltages.

When bond wire fatigue takes place, the failure effect is a loose of the electrical contact of one of the bond wires attached to the chips surface. In this paper, this is emulated by cutting off one of the bond wires attached to the source terminal of the DUT. Tests are performed over a brand new module and, after forcing the degradation, the same tests are repeated over the degraded module. This way, differences between measurements acquired in healthy and degraded conditions can be compared, certifying the performance of $V_{\mathrm{S_{aux}S}}$ as the damage indicator for bond wire degradation.

On its behalf, the effect of solder joints degradation is an increase of the thermal resistance of the module. As stated before, this is reflected in a higher $\Delta T_{\mathrm{j-amb}}$, or in a higher T_{j} if the same ambient temperature is assumed.

To emulate this behaviour, the prototype will be tested in three different scenarios: 1) Scenario I: Constant current operation; 2) Scenario II: Inverter switching at 5 kHz; and 3) Scenario III: Inverter switching at 50 kHz. The purpose of these three different scenarios is to generate different power losses and, hence, to reach different steady state junction temperatures when the same current flows through the DUT. The different junction temperatures are translated in different measured $R_{\mathrm{DS_{aux}}}$, proving its sensitivity to junction temperature variations.

In order to ensure that these scenarios truly lead to different junction temperatures, a model of the prototype has been created and the power losses in the different scenarios have been calculated. The model, based on the datasheet information of the elements on the system, is developed in Simulink/PLECS. While in Scenario I only conduction losses have to be taken into account, Scenarios II and III involve both conduction and switching losses. A comparison of the power losses in the three scenarios is shown in Fig. 6, in which for Scenarios II and III the x-axes refers to the circulating peak current and the y-axes reflects the average power losses during a fundamental period of the output current. If, as shown, the power losses are different in the different scenarios, a different junction temperature in the steady state can be expected.

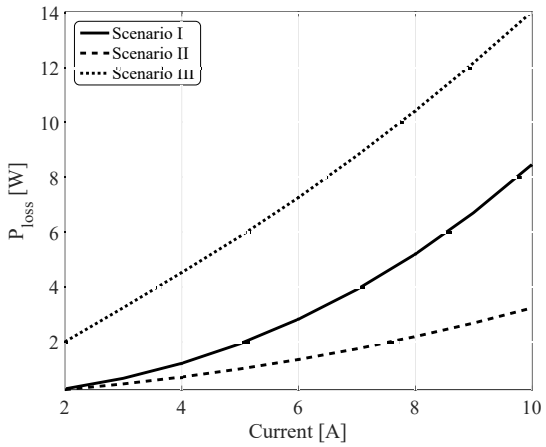


Fig. 6: Comparison of power losses in the three scenarios.

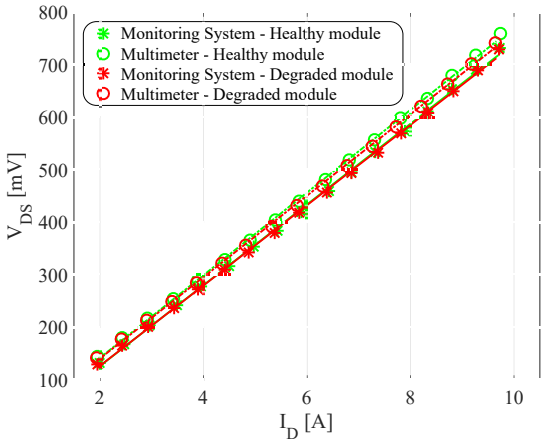
IV. Experimental Results

Over the described platform, tests have been carried out in order to validate its performance, the accuracy of the measurements and its capability to detect the degradation of the bond wires and the temperature variations of the chips. The tests were performed for a range of circulating currents. This way, the monitoring concept is independent of the operating point. Moreover, in all the tests, care has been taken in order to ensure that the DUT has reached thermal steady state in order to reduce the influence of temperature transients in the measurements.

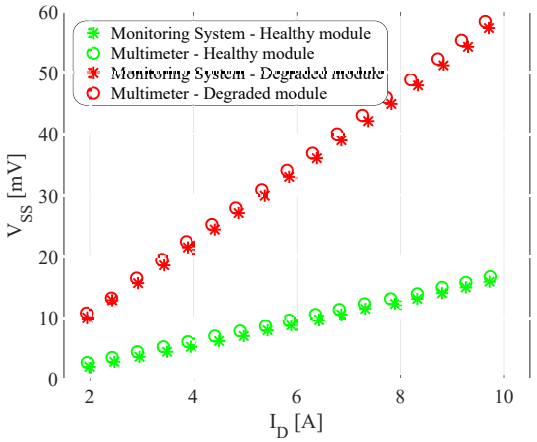
A. Scenario I: Constant current operation

The first scenario consisted in forcing a constant current through the DUT in order to verify the accuracy of the proposed system. To do this, measurements captured with the condition monitoring system are compared with those from a digital multimeter. The obtained measurements, taken in both healthy and degraded conditions, are recorded in Fig. 7. From this figure, the high precision of the monitoring system is confirmed. on the one side, considering the measurement of $V_{\mathrm{DS_{aux}}}$ in Fig. 7(a), the maximum deviation between the measurements performed with the monitoring system and with the multimeter is below 15 mV with and without the forced degradation of the bond wire. Moreover, as expected, the results show very little impact of the cut of the bond wire on the measurement.

On the other side, Fig. 7(b) shows the measurements of $V_{\mathrm{S_{aux}S}}$ at different currents. It is shown how cutting a bond wire results in a high increase in $V_{\mathrm{S_{aux}S}}$, making the effectiveness of the bond wire damage indicator indisputable. The failure could be detected online by comparing the measurements with the measurements in the healthy state, without need for calibration. Concretely, a voltage trip of 37.7 mV for a circulating current of 9 A is obtained. Comparing the measurements of the monitoring system and the multimeter, a maximum deviation of 1 mV between the tests was observed.



(a)



(b)

Fig. 7: Measurement results in Scenario I. (a) $V_{\mathrm{DS_{aux}}}$ measurements. (b) $V_{\mathrm{S_{aux}S}}$ measurements.

B. Scenario II: Inverter operation at $f_{\mathrm{sw}} = 5\,kHz$:

Once the accuracy of the measurements has been confirmed in the static test, the next step is to validate its performance with the prototype operating as an inverter. As commented above, the maximum allowable switching frequency to obtain accurate results is limited by the complexity of the $V_{\mathrm{DS_{aux}}}$ measurement circuit. The reason of this is the time it takes to the current source to set its output current after the turn-on of the power device, and the resulting time to stabilize the output voltage of the analog circuit. This is illustrated in Fig. 8, where it is shown how the $V_{\mathrm{DS_{aux}}}$ measurement error increases with the switching frequency, leading to errors higher than 1500% when the switching frequency reaches 15 kHz.

From this, it can be concluded that the maximum allowable switching frequency to measure accurately is around 5 kHz, which corresponds to a minimum settling time of 200 μs. Fig. 9 shows the measurement results obtained from the device switching at this maximum frequency, which again evidence the accuracy of the monitoring system.

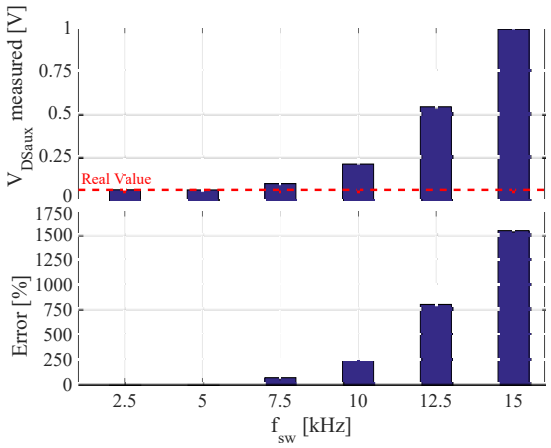


Fig. 8: Influence of the switching frequency on the $V_{\mathrm{DS_{aux}}}$ measurement with 1 A of circulating current.

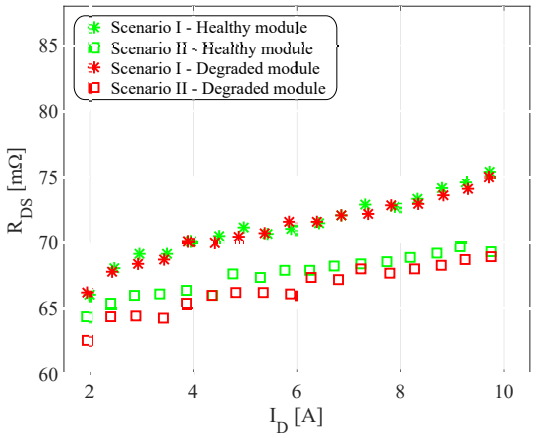
From the obtained measurements, the on-state resistance $R_{\mathrm{DS_{aux}}}$ is extracted. The results are shown in Fig. 9(a), together with the obtained $R_{\mathrm{DS_{aux}}}$ from Scenario I. It is shown how, due to the lower power losses compared with Scenario I, the resulting junction temperature is lower and, hence, the on-state resistance is also lower than in the previous case. Indeed, comparing with Scenario I, the trend shows that higher deviations are obtained at higher currents, since the power losses difference is higher (see Fig. 6). This is in agreement with the sensibility that T_{j} has over $R_{\mathrm{DS_{aux}}}$, making it a valid damage indicator for solder fatigue wear-out. Moreover, there is a slight difference of 2.1 mΩ in the resulting $R_{\mathrm{DS_{aux}}}$ after removing the bond wire.

Regarding the $V_{\mathrm{S_{aux}S}}$ measurements shown in Figure 9(b), it is once again evident the huge influence that the forced degradation has on this damage indicator, with a voltage drop increase of 37.1 mV at a drain current of 9 A, similar to the one obtained in the results above. Moreover, there are no signs of influence of T_{BW} on the measurements of the healthy module, since results similar to Scenario I have been obtained. On their behalf, the measurements of the degraded module reflect a small decrease of $V_{\mathrm{S_{aux}S}}$. However, this effect is far lower than the consequence of the bond wire cut-off.

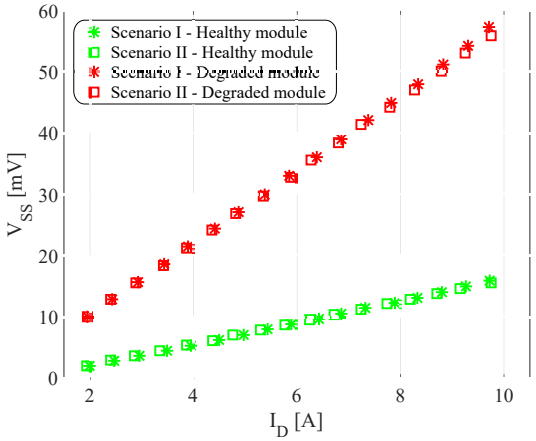
C. Scenario III: Inverter operation at $f_{\mathrm{sw}} = 50\,kHz$:

The constraint on the switching frequency imposed by the monitoring system limits its utilization on high switching frequency applications. However, the capability of reaching higher switching frequencies is one of the advantages of SiC as a power semiconductor. In order to be able to perform the monitoring in those conditions, different solutions could be implemented. However, this solution is subject to the requirements imposed by the application of the converter.

In this paper, a measurement routine consisting on maintaining the DUT in the on-state, interrupting the regular switching pattern of the sinusoidal PWM is employed. The proposed solution can be employed without high disturbances in the

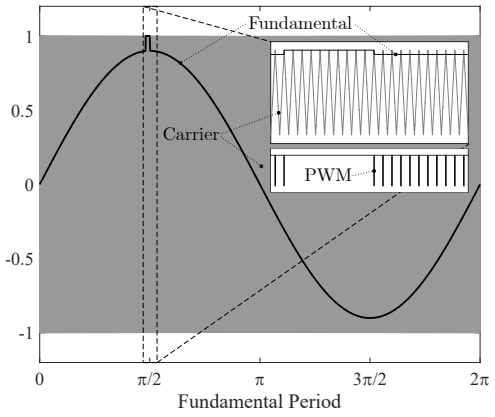


(a)

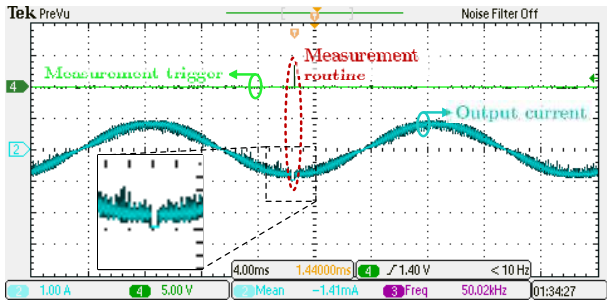


(b)

Fig. 9: Measurement results in Scenario II. (a) $R_{\mathrm{DS_{aux}}}$ measurements. (b) $V_{\mathrm{S_{aux}S}}$ measurements.



(a)



(b)

Fig. 10: Measurement routine for high switching frequency devices. (a) Modification of the PWM modulation strategy. (b) Effect of the modification on the output current of the prototype when switching at 50 kHz.

presented prototype when operated at high modulation indexes and resistive loads. This way, the current keeps circulating through the DUT and there is enough time available for the measurement to be settled. The duration of the routine is imposed by the monitoring system.

Figure 10 illustrates the modification of the switching pattern, and its effect on the output current of the inverter. As shown in Fig. 10(a), for a DUT switching at 50 kHz and a required settling time of 200 μs, the switching is altered during 10 switching periods. The effect of this modification on the output current of the inverter can be seen in Fig. 10(b) for a switching frequency of the DUT of 50 kHz and a maximum circulating current of 1 A. Despite the alteration of the switching pattern, the effect on the current is negligible. Moreover, this routine has been implemented in the model of the prototype, and the Total Harmonic Distortion of the output current $\mathrm{THD_i}$ has been calculated. The results are compared with the ones from employing the regular modulation in Table II for a maximum circulating current of 9 A. They confirm the little influence that the routine has in the harmonic content of the output current.

TABLE II:
CURRENT TOTAL HARMONIC DISTORTION.

	Normal Modulation	Measurement Routine
$\mathrm{THD_i}$	0.0968	0.0998

The presented routine has been employed to obtain the measurements in Fig. 11. In Fig. 11(a), the resulting $R_{\mathrm{DS_{aux}}}$ in this scenario are shown, which again are compared with the results of Scenario I. It can be seen that, unlike in the previous scenario, the on-resistance is higher, indicating a higher junction temperature consequence of the higher losses. Moreover, there is a shift of 1.5 mΩ after removing the bond wire.

The results in Fig. 11(b) prove newly the effectiveness of the bond wire collapse identification through $V_{\mathrm{S_{aux}S}}$, with a voltage trip of 37.56 mV at 9 A of drain current. Again, the results for the healthy module are the same than in Scenario I, while a little increase in the bond wire resistance can be appreciated in the results of the degraded module.

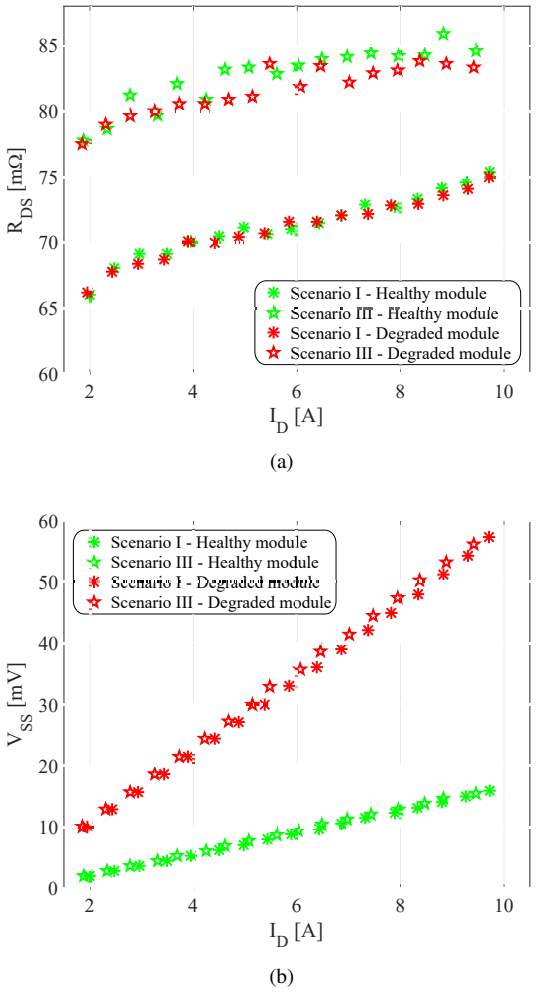


Fig. 11: Measurement results in Scenario III. (a) $R_{\mathrm{DS_{aux}}}$ measurements. (b) $V_{\mathrm{S_{aux}S}}$ measurements.

V. Conclusions

In this paper, a monitoring system for the failure identification of power semiconductor modules is presented. Through the measurement of $V_{\mathrm{DS_{aux}}}$ and $V_{\mathrm{S_{aux}S}}$, the two most relevant failure mechanisms can be identified independently: solder joints degradation and bond wire fatigue, respectively. On the one side, the degradation of the solder joints, which affects the heat cooling path, is reflected in a higher junction temperature, which could be recognized employing $R_{\mathrm{DS_{aux}}}$ as a TSEP. On the other side, the collapse of a bond wire is acknowledged through the monitoring of the source-to-auxiliary source voltage, caused by the current circulating through them.

The proposed monitoring system has been implemented in a prototype with a SiC MOSFET module and has been tested in different scenarios to validate its performance. The prototype showed its capability to measure accurately both in static tests and operating as an inverter. However, it showed a practical limitation of 5 kHz in the switching frequency. Therefore, in order to be able to perform the monitoring when the DUT switches at higher switching frequencies, a measurement routine lasting 200 μs is proposed. Although this measurement routing alters the regular switching pattern, it extends the measurement capability of the condition monitoring system. This routine has been employed to monitor the DUT switching at 50 kHz, showing accurate results again. The effects of the main failure mechanisms were emulated, and the monitoring system proved its capability to identify them independently.

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