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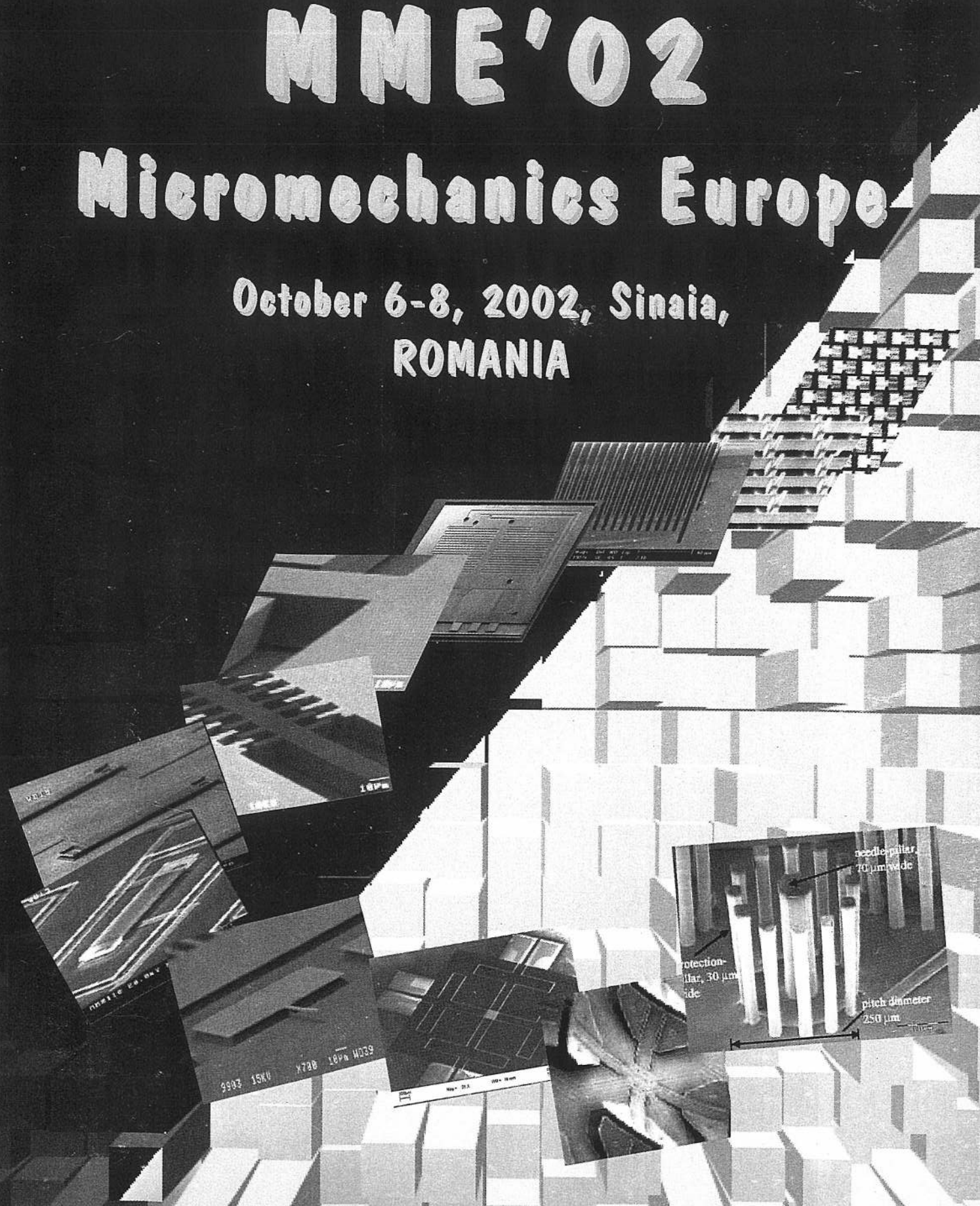

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WET ANISOTROPIC ETCHING FOR FLUIDIC 1D NANOCHANNELS

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Abstract

In this paper a method is proposed to fabricate channels for fluidic applications with a depth in the nanometer range. The channels with smooth and straight sidewalls are constructed with the help of micromachining technology by etching shallow trenches into <110> silicon using native oxide as a mask material and OPD resist developer as the etchant. Sub-50 nm deep fluidic channels are formed after bonding the nanopatterned wafers with silicon or borofloat-glass wafers.

The nanofabrication process is largely simplified by using native oxide as the main mask material. The etch depth of the nanochannels is limited by the thickness of the native oxide layer, and by the selectivity of the oxide/silicon etch rate (estimated to be at least 250 for <110> silicon at room temperature).

Key Words: *native oxide mask, TMAH, OPD 4262 developer, silicon <110>, anisotropic etching, nanotechnology, fluidic nanochannel, fluidic devices.*

I. INTRODUCTION

The fabrication of one-dimensional (1D) nanometer-sized channels and tubes has gained considerable attention in the past decade because of their potential use in chemical and DNA analysis and synthesis. The channels are used as connection ports, fluidic delivery systems (including "outlet" inkjet printing heads), fluidic particle separation and filtering obstructions, biochemical reaction chambers, fluidic pumps, or as micro heat pipes for cooling computer chips. An artist impression of such a typical 1D nanochannel is found in figure 1.

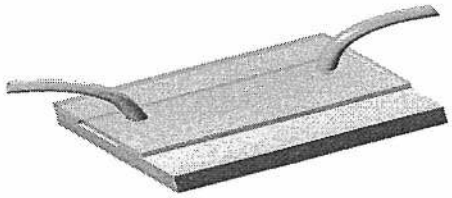

Fig. 1. Nanochannel in silicon with glass cover.

The continuously growing interest in artificial nanostructures has stimulated the search for novel nanofabrication techniques. Two different strategies can be distinguished to construct 1D nanochannels: surface and bulk nanomachining. An overview of fabrication techniques of channels is described by Rasmussen [1].

In bulk nanomachining, shallow sub-100 nm trenches are etched in a wafer and covered by another wafer to form 1D nanochannels; a process known as wafer bonding. Different bonding methods are found depending on the bulk material used. As an example of bulk nanomachining, Han demonstrated entropic trapping of long DNA [2]. Channels with a depth of 90 nm were made in silicon using reactive ion etching (RIE) and covered by a Pyrex-glass wafer using anodic bonding. A refractive index sensor in a nanofluidic system was developed by Kameoka [3]. A layer of 80 nm of silicon was deposited on a glass wafer and etched by RIE. The wafer was subsequently diced and anodically bonded to another glass wafer.

In surface nanomachining, a patterned and buried layer is removed/etched to form nanochannels; a process known as sacrificial layer etching. Nanochannels can be fabricated using a variety of materials, including silicon oxide/nitride, polysilicon, metals, and polymers. Single molecule detection in nanochannels is proposed by Foquet [4]. After patterning a thin film of silicon on top of a silica-glass wafer, the entire wafer is capped with a 1 micron thick silica layer. Irrigation holes are etched in the capping oxide, thus providing access to the polysilicon sacrificial layer. After removing the silicon, the access holes are closed using a conformal deposited oxide layer. In a final step, large holes are etched in the capping oxide to allow for fluid exchange. A similar process is proposed by Stern [5]. They use 1D nanochannels as small as 20 nm in height with silicon nitride walls for chemical sensing. The use of a 140 nm thin patterned polymer film for nanofluidics is proposed by Harnett [6].

All the proposed techniques to construct 1D nanochannels have some drawbacks. The surface nanomachining is rather complex and, unless special access holes are used, long etch times are needed to remove the sacrificial layer completely. The proposed bulk nanomachining techniques make use of expensive RIE equipment and special masks for pattern transfer. RIE normally creates rough surfaces and the sidewalls of the trench are tapered.

Especially when the width of the trench is in the same order of magnitude as the trench depth (i.e. sub-100 nm), the roughness and shape of the sidewall will have a major influence on the flow characteristics of the nanochannel.

To be able to etch channels with a depth of several hundreds of nanometers or less in silicon with smooth walls, a simple and straightforward process would be beneficial. The ideal situation would be to have an etchant that etches at a sufficiently low rate, so that the depth of the trench can be easily controlled, and that the etch process would leave a very smooth surface. Although they did not focus on nanofluidics, the fabrication of sub-10 nm lines in <110> Si with smooth sidewalls and surface has been demonstrated by Namatsu [7].

This paper focuses on the wet anisotropic etching of <110> silicon using native oxide as a mask to construct 1D nanochannels. Several silicon etchants have been investigated, including KOH, TMAH (Tetra Methyl-Ammonium-Hydroxide) and Olin OPD 4262 positive resist developer. OPD has a low concentration of TMAH (2.5 wt.%), as well as some surfactant additives. The use of anisotropic etching of <110> silicon gives the additional advantage of channel sidewalls that are perpendicular to the wafer surface.

II. METHODS

The basic process is depicted in figure 2:

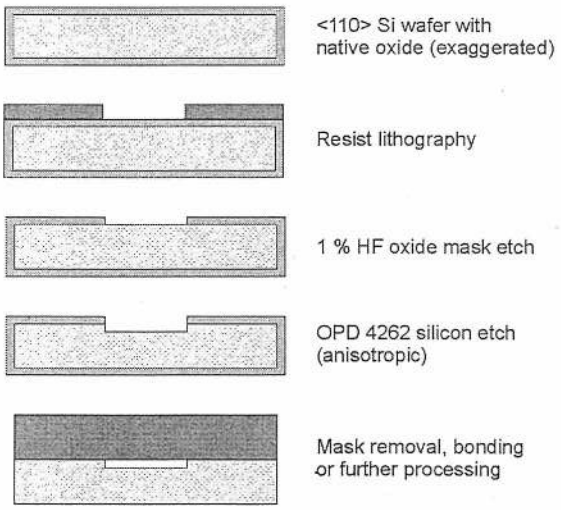

Fig. 2. Basic fabrication process of a nanochannel.

A <110> p-type silicon wafer is used in the experiments. No cleaning step is performed before the lithographic steps. Using this wafer, the following lithographic steps are performed: after a dehydratation step (>10 min at 120°C), an adhesion layer (HMDS) and photosensitive resist (Olin 907/12) are subsequently spin-coated (20 seconds at 4000 rpm). Then, after a softbake (1 min at 95°C), the resist is exposed (4 sec at 12 mW/cm^2) using an ElectroVisions 620 exposure apparatus (EVG), and a mask containing 4 μm wide lines and spacings. After this, a post exposure bake (1 min at 120°C) is performed followed by development of the exposed resist by a standard 2.5% water diluted TMAH solution (Olin, OPD 4262).

After lithography, a 1% HF dip (1 min) is done to transfer the resist pattern to the native oxide layer. Then the wafer is immersed in acetone for one minute to strip the resist, directly followed by an isopropanol (IPA) cleaning dip (1 min), after which it is blow-dried with nitrogen gas.

The pattern transfer into the native oxide is directly followed by a silicon etch at room temperature using a fresh OPD solution as the wet chemical etchant and the native oxide as the mask material. Finally, the wafer is rinsed with DI water and spin-dried.

After a surface scan with a mechanical profiler (Sloan Dektak II) to determine the depth of the silicon nanochannels, the wafer together with a cover wafer is prepared for bonding in order to seal the nanochannels.

Silicon<110>-to-silicon<110> direct bonding was done after a 1% HF dip and a Piranha step to clean the silicon surface and to grow a well controlled layer of native oxide on the silicon wafer surface.

Silicon<110>-to-borofloat direct bonding was done after cleaning the borofloat wafer by immersing it in a 25% KOH solution at 75°C for 2 minutes, then a DI water quick dump rinse, and spin-drying of the wafer (the silicon wafer underwent the same pre-treatment as described for the silicon-to-silicon bond).

The direct bonding was followed by a 2 hour anneal step at 1100°C for the silicon-to-silicon bond, and a 4 hour anneal at 400°C for the silicon-to-borofloat bond. The annealing temperature for the silicon-to-borofloat bond is kept rather low intentionally, to prevent plastic deformation of the glass (and thereby possibly closing of the nanochannels).

For nanofluidic applications, it is important that the etch depth is well controlled and the surface roughness is minimized. The etch rate of the etchant should be low enough to allow for accurate etch

depth control, but also high enough to be of practical use. After an initial test to determine the differences between the KOH/TMAH/OPD-based etchants, it was clear that the OPD 4262 developer gave a much better surface finish than any of the other candidates, probably due to the addition of surfactants to the OPD. However, the addition of surfactants does not necessarily have a positive effect, as was proven in a test with NaOH versus Clariant AZ 351B NaOH developer.

Taking all mentioned issues into account, highly controllable and smooth etching of sub-100 nm nanochannels is possible as proven in this paper.

III. RESULTS & DISCUSSION

A calibration of the etch rate of <110> silicon in OPD at room temperature was done to be able to fine-tune the depth of the etched structures. The graph of the channel depth versus the time can be found in figure 3. From this graph some important conclusions can be drawn. The first is that OPD developer etches <110> silicon with a speed of 3.7 nm/min (220 nm/hr) at room temperature.

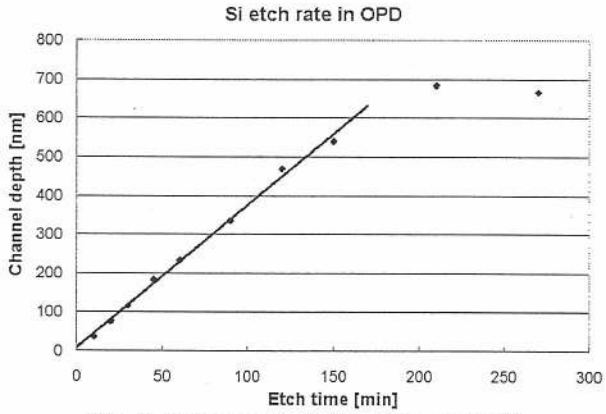

Fig. 3. Etch rate of <110> silicon in OPD.

Another observation is that channels with a depth up to at least 500 nm can be produced with this method. At long etching times (above 200 minutes) the channel depth does not increase any further. This is most likely due to the fact that the mask (the native oxide at the <110> silicon surface) has worn out at this point. The fact that the etch depth stays at a constant level at etching times over 200 minutes, can be explained by the fact that both the top and the bottom of the channels are now directionally etched at the same speed. Assuming an oxide thickness that can vary from 0.5 to 2 nm [8], this would give a selectivity of at least 250:1.

We have to bear in mind that the etch rate of the monocrystalline silicon in general depends on the crystal orientation and, furthermore, that the thickness of the native oxide layer also depends on the crystal orientation [8]. This implies that the etch rate ratio between <110> silicon and its native oxide differs from the ratio between <100> silicon and its native oxide.

The uniformity of the etch depth over a complete wafer was also shown to be good: measuring five points across a 4" wafer gave a variation of ± 1 nm at an etch depth of 50 nm. Figure 4 shows a channel with a step height of 335 nm. The surface roughness (Ra) on the trench bottom is below 0.5 nm (determined by AFM measurements).

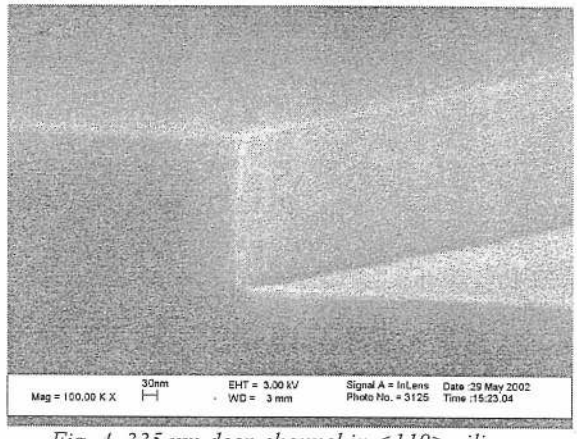

Fig. 4. 335 nm deep channel in <110> silicon.

The silicon-to-silicon direct bonding showed an instantaneous, almost perfect bond under an infrared camera. Pictures of the cross-section of the silicon-to-silicon bond can be seen in figures 5 and 6. The curved ridges on the top wafer (figure 5) are due to the breaking of the wafer, resulting from a non-perfect alignment of the two wafers during bonding. The straight etch profile can again be seen in figure 6.

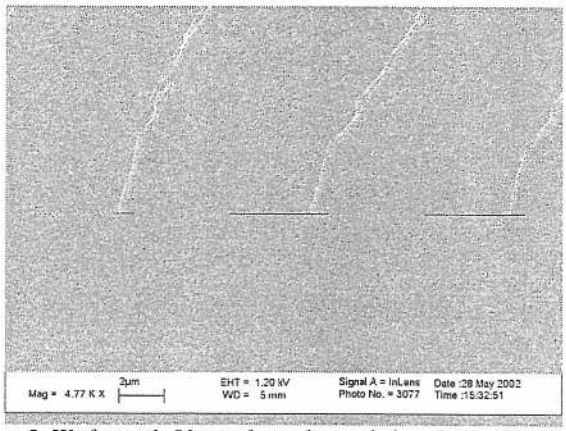

Fig. 5. Wafer with 50 nm deep channels bonded with silicon cover wafer.

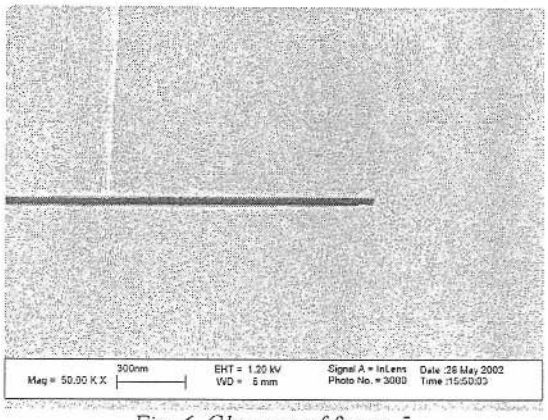

Fig. 6. Close-up of figure 5.

The silicon-to-borofloat bond proved to be a little more complicated, but an almost complete bond was formed by manually pressing the wafers together, followed by an anneal step (figure 7).

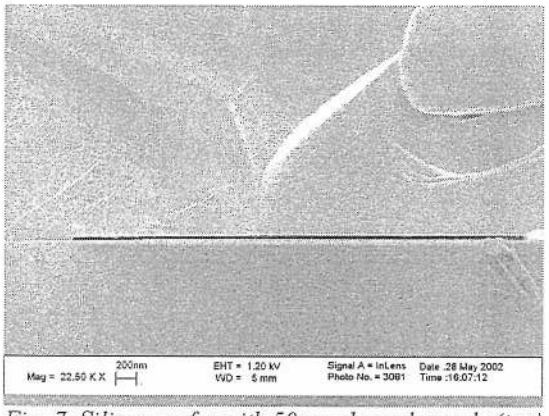

Fig. 7. Silicon wafer with 50 nm deep channels (top) bonded to a borofloat wafer (bottom).

As can be seen in figure 7 the channels are completely open and no significant bending of the wafers occurs.

IV. CONCLUSIONS

We have demonstrated a simple process to etch channels with a controlled depth up to 500 nm with an accuracy of a few percent. Etch depth uniformity across a wafer and from wafer-to-wafer are excellent. Moreover, etch roughness could not be observed with SEM, and AFM measurements indicate an Ra value below 0.5 nm.

Native oxide is a suitable mask material to fabricate these channels. Olin OPD 4262, a standard resist developer, consisting of 2.5% TMAH and surfactants is suitable as an etchant for the anisotropic etching of nanochannels in a silicon <110> wafer, having an etch rate of 3.7 nm/min at room temperature.

The etched wafers were successfully bonded to silicon and borofloat-glass wafers to seal the channels.

In the future, we plan to develop two-dimensional nanochannels by combining this technique with Laser Interference Lithography (LIL). Using LIL, sub-micron sized periodical patterns can be patterned in photoresist, bringing also the width of the channels in the nanometer range [9].

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