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Where Does the Current Flow in Two-Dimensional Layered Systems?

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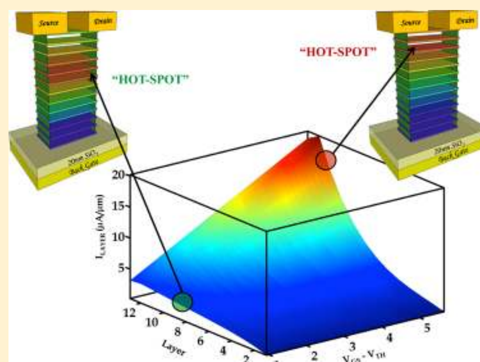
ABSTRACT: In this Letter, we map for the first time the current distribution among the individual layers of multilayer two-dimensional systems. Our findings suggest that in a multilayer MoS_2 field-effect transistor the "HOT-SPOT" of the current flow migrates dynamically between the layers as a function of the applied back gate bias and manifests itself in a rather unusual "contact resistance" that cannot be explained using the conventional models for metal-to-semiconductor contacts. To interpret this unique contact resistance, extracted from a channel length scaling study, we employed a resistor network model based on Thomas−Fermi charge screening and interlayer coupling. By modeling our experimental data we have found that the charge screening length for MoS_2 is rather large (λ_{MoS_2} = 7 nm) and translates into a current distribution in multilayer MoS_2 systems, which is distinctly different from the current distribution in multilayer graphene ($\lambda_{graphene}$ = 0.6 nm). In particular, our experimental results allow us to retrieve for the first time fundamental information about the carrier transport in two-dimensional layered systems that will likely play an important role in the implementation of future electronics components but that have not been evaluated in the past.



KEYWORDS: *MoS_2, current transport, FET, contact resistance, charge screening, 2D-materials*

Two-dimensional layered materials like graphene, h-BN, topological insulators, and more recently the family of transition metal dichalcogenides like MoS_2 and WSe_2 have started to reveal unique transport related and structural features that may become useful in future generations of nanoelectronic devices and circuits.[1−16] It is therefore important to further evaluate the true intrinsic potential of these novel low-dimensional systems by understanding their core physical properties. In one of our previous articles, we already demonstrated how to connect MoS_2 to the "outside world" using optimized three-dimensional metal contacts.[14] Critical insights into other device aspects, like the dependence of the "effective" field-effect mobility on the layer thickness, were recently published.[17] In this context, a resistor network model based on Thomas−Fermi charge screening and interlayer coupling has been successfully employed to describe various scaling aspects of multilayer MoS_2. Also, in this earlier study we noticed a remarkable difference between graphene and MoS_2, that is, that both the coupling between layers and charge screening from layer to layer is vastly different. The work presented here extends our understanding of the interlayer resistance and charge screening length through a detailed channel length and gate voltage dependent study. In particular our experimental results hint at a fundamental difference between materials like graphene where transport occurs through p_z-orbitals while d-electrons are involved in forming the relevant bands in the case of MoS_2.

In addition to the above-mentioned unique intrinsic properties, low-dimensional materials offer in general excellent electrostatic control owing to their inherently thin body. The same reason that makes Fin-FETs[18,19] and Tri-Gates[20−22] the device structures for ultimately scaled complementary metal−oxide−semiconductors (CMOS), that is, a channel that confines the electron motion without harming the respective transport properties, makes dichalcogenides potentially an ideal choice for ultrasmall FETs. Moreover, the substantial bandgap prevents direct tunneling from the source to the drain, another limiting factor when it comes to device scaling.[23,24] The final verdict about the usefulness of the dichalcogenides for high-performance applications will likely depend on whether the current drive capabilities can rival silicon devices at the end. To this extent, the work presented here elucidates how device characteristics, and in particular current through the device is distributed among the individual layers by analyzing various resistance contributions in multilayer MoS_2 FETs.

One of the most neglected aspects in the context of device applications is the so-called "contact resistance". Often it is argued that contact resistance effects can be eliminated by means of four-terminal measurements and that contacts are an extrinsic engineering problem that can be ignored for the sake of studying fundamental material properties and physical phenomena. In reality however, contact effects are limiting the current flow through the device and often impact four-terminal measurements substantially since voltage probes frequently change the potential landscape in low-dimensional systems and are thus not truly "non-invasive".[25] Moreover, when current flows nonuniformly through a layered structure (as will be discussed here), in addition to the metal to

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semiconductor interface, interlayer resistance contributions have to be considered. In this case the potential difference from a four-terminal measurement is not a valid measure of the intrinsic mobility of the material since both the carrier concentration and the mobility becomes spatially dependent; that is, they change with the respective layer number. All of those facts ultimately mask the intrinsic properties of novel layered materials like dichalcogenides and demand a fundamentally different approach to gain insight into the transport properties of this material class.

When exploring the transport in multilayer MoS_2, and here in particular the extrinsic resistance through a channel length dependent study, we uncovered a rather unusual scaling trend as a function of the applied gate bias that cannot be explained within the conventional model for Schottky barrier contacts. In fact, our experimental findings suggest that at different back gate biases the centroid of the current distribution—referred to in the following as the "HOT-SPOT"—migrates dynamically within the interlayers and as such gives rise to an unusual trend in the effective contact resistance. As will be described in more detail using a resistor network model based on Thomas–Fermi charge screening and interlayer coupling, this effective contact resistance is mainly determined by the effective interlayer resistance that comprises the various interlayer resistors involved in the current transport under the respective gate voltage conditions.

We first experimentally evaluate the current distribution in a stack of 8 nm thick MoS_2 which consists of approximately 13 monolayers. Since the current in the individual layers cannot be measured directly, we have devised an alternate route to map the current distribution—namely, a channel length scaling study which will be discussed in detail in the following. Figure 1a shows a scanning electron microscopy (SEM) image of a back gated multilayer MoS_2 FET with channel lengths ranging from 500 to 50 nm located on a 20 nm thin film of SiO_2 with highly doped Si as the substrate. Figure 1b displays the device structure schematically. A metal stack of Sc/Ni (30 nm/20 nm) was used to create the source/drain contacts employing electron beam lithography. The width of the contact bars is 300 nm. The use of scandium as the source/drain contact metal is a result of a former study by us[14] that indicated that this low work function material allows for excellent electron injection into the channel. Our earlier findings indicate in particular that the metal-to-MoS_2 contact exhibits a small Schottky barrier height of around 30 meV and therefore results in a contact resistance value of about 650 $\Omega \cdot \mu m$ for an oxide thickness of 20 nm. The contact resistance value associated with the Sc-to-MoS_2 Schottky barrier has been calculated using Wentzel–Kramers–Brillouin (WKB) approximation for a triangular Schottky barrier. The choice of a 20 nm thin SiO_2 as the back gate oxide is motivated by the fact that better carrier injection is enabled through a thinner Schottky barrier in this case. Moreover, gate electrostatics are significantly improved for thinner oxides—20 nm SiO_2 allows for more than 15 times stronger gate control of the MoS_2 channel if compared with the commonly used 300 nm SiO_2 substrate. Lastly, short channel effects are suppressed more effectively through scaling of the gate oxide.[23]

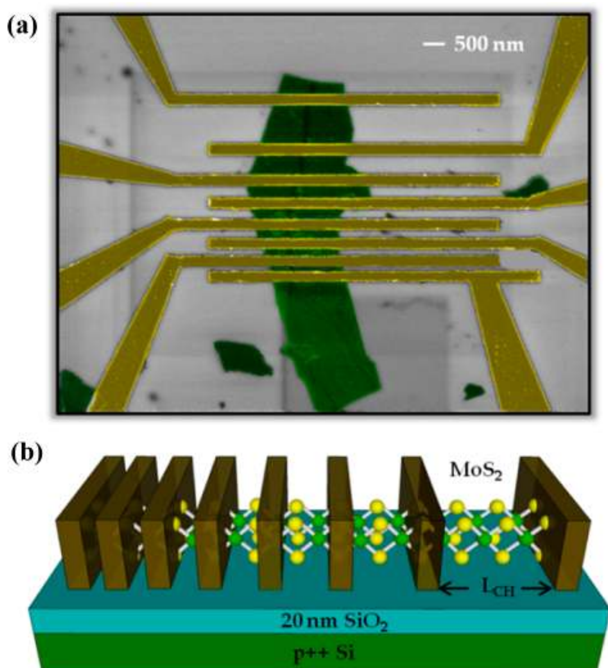

Figure 1. (a) SEM image and (b) 3-D cartoon of an 8 nm thick MoS_2 back gated FET with different channel lengths.

Figure 2a and b shows the output characteristics of 8 nm thick MoS_2 transistors with channel lengths of 500 nm and 100 nm, respectively. First, we extract the total resistance (R_{total}) of the MoS_2 stack in the linear region of the device output characteristics (from the slope of the I_{DS} versus V_{DS} at small V_{DS} values). We notice that the values of the R_{total} for a gate overdrive voltage $V_{GS} - V_{TH} = 1.0$ V (V_{GS} being the gate bias and V_{TH} being the threshold voltage which describes the onset of charge accumulation in the channel) are 82.2 $k\Omega \cdot \mu m$ and 20.4 $k\Omega \cdot \mu m$ for the 500 nm and 100 nm long devices, respectively. In the diffusive transport regime, the intrinsic channel resistance should scale linearly with the channel length in the ON state ($V_{GS} - V_{TH} > 0$) of the device operation. However, the extracted total resistance (R_{total}) numbers strongly suggest that an additional resistance contribution exists in the devices. Generally this additional resistance arises due to contact effects and here in particular Schottky barriers at the source/drain metal interface. To extract the magnitude of the total contact resistance ($R_{contact}$), we utilize the plots in Figure 2c. We define the total resistance (R_{total}) of the MoS_2 stack as the sum of the total in-plane layer resistance (R_{layer}) and the contact resistance ($R_{contact}$). Since R_{layer} scales linearly with the channel length while $R_{contact}$ is assumed to be constant as a function of the channel length, the intercept of the R_{total} versus channel length (L_{CH}) curves with the y-axis in Figure 2c can be interpreted as $R_{contact}$. The magnitude of $R_{contact}$ was found to be ~10 $k\Omega \cdot \mu m$ for $V_{GS} - V_{TH} = 1.0$ V and ~5 $k\Omega \cdot \mu m$ for $V_{GS} - V_{TH} = 4.0$ V. However, as we have argued earlier, the contact resistance value associated with the Sc-to-MoS_2 Schottky barrier is only 0.65 $k\Omega \cdot \mu m$ and as such cannot account for this additional resistance. Moreover, $R_{contact}$ shows a strong dependence on the applied gate bias. The contact resistance due to Schottky barriers on the other hand exhibits only a very weak dependence on the gate bias in the device on-state. This is due to the fact that for sufficiently large voltages beyond threshold the energy band movement in the channel of the transistor almost stops. Therefore, neither the effective Schottky barrier height nor the effective tunneling distance through the triangular Schottky barrier changes. The above argument implies that the effective contact resistance we

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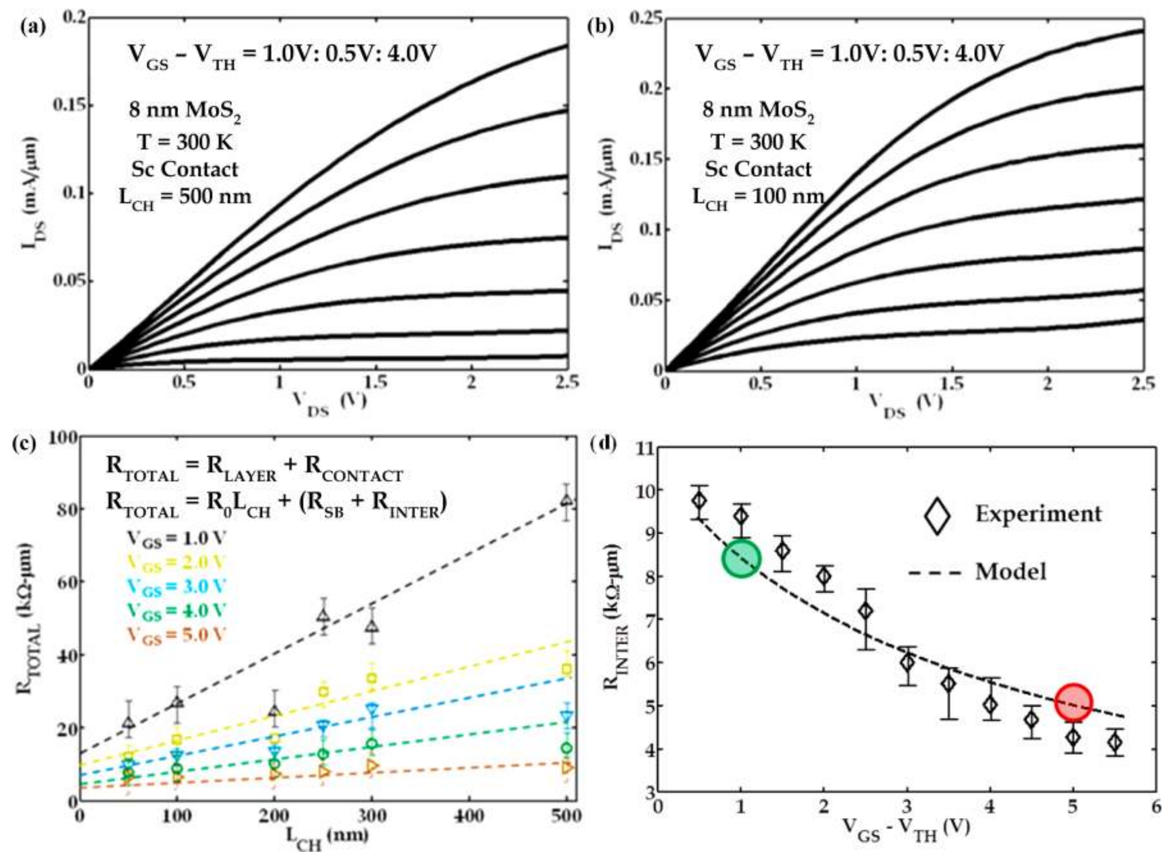

Figure 2. Output characteristic of (a) 500 nm and (b) 100 nm long and 8 nm thick MoS_2 back gated field effect transistors with scandium contacts at room temperature. (c) Total resistance of 13 monolayers of MoS_2 as a function of channel length for different gate bias conditions and (d) extracted effective interlayer resistance corresponding to different gate bias conditions. The dotted lines in c are guides to the eyes while the dotted line in d is a fit to the experimental data using resistive network model described in the text with $\lambda = 7$ nm, $R_{int} = 2400\ \Omega\cdot\mu$m, $d_{ML} = 0.6$ nm, $\mu_1 = 30$ cm^2/(V s), and $\mu_\infty = 800$ cm^2/(V s).

determined involves resistance components other than the conventional source/drain Schottky barrier resistances (R_{SB}).

Based on our study and as will be discussed in greater detail below, we propose that the additional resistance arises due to the resistive coupling between the individual layers of a multilayer two-dimensional system. This resistance is referred to as the effective interlayer resistance (R_{inter}) and comprises one or more interlayer resistors. Note that these interlayer resistors are quite different from the intralayer resistors as they define the current flow in two orthogonal directions. The intralayer resistors give rise to the true channel resistance while the interlayer resistors acts as additional access resistors for the layers which are further apart from the source and the drain contacts and give rise to the additional contact resistance. Figure 2d (diamonds) shows the R_{inter} as a function of the gate bias after subtracting the R_{SB}-value from $R_{contact}$. The strong dependence of the effective interlayer resistance on the gate bias clearly indicates that, at different gate bias conditions, different numbers of interlayer resistors are involved in the current flow and hence the current distribution among the layers must be changing.

To map the current distribution quantitatively a resistive network model including Thomas−Fermi (T-F) charge screening[26−28] and interlayer coupling as shown in Figure 3 is employed. R_1, R_2, to R_N are the intralayer resistors of each monolayer, while R_{int} captures the contribution of an interlayer resistor due to coupling between two consecutive layers. Q_i is the charge in the i-th layer, μ_i is the mobility of the i-th layer,

Figure 3. A resistor network based on T-F charge screening and interlayer coupling that describes multilayer two-dimensional systems.

d_{ML} is the distance between two consecutive layers, and N is the total number of layers. In our model, we assume that the source and the drain contacts can only inject carriers directly into the top layer while access to lower layers involves the interlayer

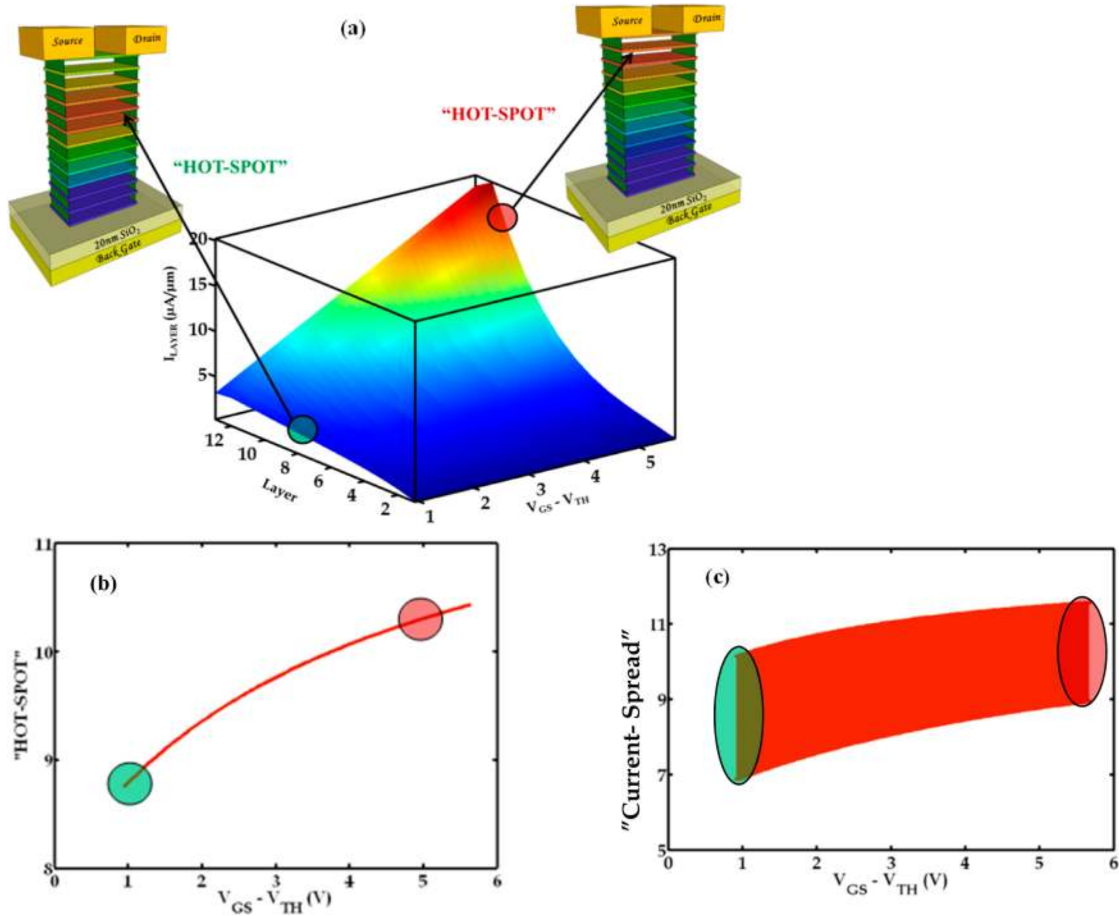

Figure 4. (a) Current distribution among the individual layers of a 13 monolayers thick MoS_2 at different gate bias conditions derived using the resistor network model. The cartoons show the location of the "HOT-SPOT" and the associated current spread schematically corresponding to two different gate bias conditions. (b) Monotonic migration of the "HOT-SPOT" toward the top layers and (c) the monotonic decrease of the current spread as a function of the applied gate bias.

resistors (R_{int}). A smaller value of R_{int} allows the current to reach lower layers more readily, while a larger value of R_{int} restricts the current to flow through the top layers. Gating on the other hand introduces the highest number of charges in the lowest layer and a decreasing number of charges in the top layers. This is a direct consequence of the T-F charge screening described by eq 1 where λ is the T-F charge screening length.

$$\frac{Q_i}{Q_{i-1}} \approx \exp\left(-\frac{d_i - d_{i-1}}{\lambda}\right) = \exp\left(-\frac{d_{ML}}{\lambda}\right) = c$$
$$\sum_{i=1}^{N} Q_i = Q_{gate} \tag{1}$$

We further assume that independent of the number of layers (N) the total charge on the gate $Q_{GATE} = C_{OX}(V_{GS} - V_{TH})$, with C_{OX} being the oxide capacitance, will be mirrored by the total induced charge in the channel region, that is, all layers involved in current transport. For both, our model and experiments we have used 20 nm thick SiO_2 as the back gate oxide which results in a gate oxide capacitance value of $C_{OX} = 1.7 \times 10^{-3}$ F/m^2. Our model also takes into account the impact of charge impurity scattering from the substrate. As observed in most (if not all) back-gated transistor geometries, charge impurity scattering is most significant in the bottom layers close to the dielectric substrate due to fixed charges in the same. The above-mentioned T-F charge screening helps to reduce carrier scattering in layers further away from the gate oxide interface by minimizing the substrate impact. The intuitive picture is that the same exponential decay that we observe for the carrier concentration in the various layers also describes the decreasing impact of the Coulomb potential from those charges at the oxide/channel interface. The mobility of the individual layers can therefore be modeled using eq 2. A detailed discussion on the resistor network model and associated assumptions can be found in our earlier articles.[14,17]

$$\mu_i = \mu_1 + (\mu_\infty - \mu_1)\left(1 - \exp\left(-\frac{(i-1)d_{ML}}{\lambda}\right)\right) \tag{2}$$

Next, we use this resistive network model to describe the current flow in the multilayer MoS_2 systems. From a previous study on the impact of layer thickness on the effective mobility we had estimated that $\lambda = 7$ nm, $R_{int} = 2400\ \Omega\cdot\mu$m, $d_{ML} = 0.6$ nm, $\mu_1 = 30$ cm^2/(V s), and $\mu_\infty = 800$ cm^2/(V s) for MoS_2 systems.[28] Here we extend this study to include the experimental findings on the gate bias and channel length dependence. Indeed we find that the identical set of parameters is able to comprehensively describe the multilayer MoS_2-system and current flow in the same. Our findings reveal in particular a unique distribution of the current flow that had not been previously noted.

Figure 4a shows the current distribution in a stack of 13 monolayers of MoS_2 at different gate bias conditions. It is interesting to note that under any given gate bias condition current flow mainly occurs through the upper layers. Consequently the layers close to the source and the drain contacts become the "HOT-SPOT" in this type of stacked resistance network as shown in the associated cartoons in Figure 4a. The explanation for this phenomenon lies in the relatively large values of λ, R_{int}, and in the significant impact of the charge impurity scattering that reduces the mobility of the bottom layers close to the substrate to a considerable extent. The top layers in a stack like this are less resistive since the mobility values for the top layers are higher and a large value of λ ensures that the top layers are populated with a considerable amount of charges. The bottom layers, on the other hand, are more resistive due to their significantly lower mobility values, in spite of higher charge population. A large value of interlayer resistance, at the same time, makes it difficult for the current to flow into the lower layers and thereby forces the current to reside in the top layers. As the gate bias is increased, the resistance of each individual layer decreases monotonically resulting in a monotonic increase in the corresponding layer current. The total current in such a system will ultimately be limited by the effective interlayer resistance. The reader should note that there exists an optimum layer number for a back gated multilayer system like this to ensure the highest performance. A monolayer device will be limited by its low mobility value while a multilayer device with too many layers will be limited by the large effective interlayer resistance and screening of charges resulting in an ever lower carrier concentration for the upper layers.

Figure 4b shows the monotonic migration of the "HOT-SPOT" toward the top layers close to the source/drain contacts, and Figure 4c shows the monotonic decrease of the current spread for the current distribution in the 8 nm (13 monolayers) thick MoS_2 stack at different gate bias conditions. The location of the "HOT-SPOT" is determined as the centroid of the current distribution by calculating the weighted average of the current in the individual layers while the current spread is determined as the standard deviation of the current in the individual layers (eq 3). As apparent from the green dots in Figure 4b,c and the associated cartoon on the left-hand side of Figure 4a, at low gate bias (V_{GS} = 1.0 V) the "HOT-SPOT" is at the ninth layer with a current spread of three layers. At this bias condition the current from the source drives into the "HOT-SPOT" region through effectively 2−3 interlayer resistors and then returns back to the drain through a similar number of interlayer resistors, giving rise to an effective interlayer resistance of around 10 kΩ·μm (green dot in Figure 2d). Note that, because of the finite value of the current spread the number of interlayer resistors to access the "HOT-SPOT" at the ninth layer is not exactly 4. Similarly, red dots in Figure 4b,c and the associated cartoon on the right-hand side of Figure 4a show that, at large gate bias (V_{GS} = 5.0 V) the "HOT-SPOT" is close to the 10th layer with a spread of two layers. At this bias condition the current from the source drives into the "HOT-SPOT" region through effectively one interlayer resistor and then returns back to the drain through the other interlayer resistor giving rise to an effective interlayer resistance of around 5 kΩ·μm (red dot in Figure 2d). The dotted line in Figure 2d is a fit to the experimental data using our resistor network model and the parameter set which was extracted based on our earlier experiments.[28] This simple resistor network model, therefore, captures the essence of current transport in a multilayer MoS_2 system to a large extent. The reader should note that the effective interlayer resistance which manifests itself in an effective contact resistance in a layered system arises from the current distribution among the individual layers and cannot be captured by any conventional model that is solely based on a metal-to-semiconductor contact. Also note that the effective contact resistance can be eliminated from the device characteristics if the source/drain contacts can be made such that direct injection into the lower layers occurs or gating is enabled from the top.

$$\text{HOT-SPOT} \quad E(i) = \frac{\sum_1^N iI_i}{\sum_{i=1}^N I_i}$$
$$\text{current spread} \quad SD(i) = \sqrt{E(i^2) - E(i)^2} \tag{3}$$

Last, to show the universal applicability of the resistor network to other layered systems, we have modeled a multilayer graphene stack. Consistent with the literature we have assumed λ = 0.65 nm, R_{int} = 100 Ω·μm, d_{ML} = 0.35 nm, μ_1 = 5000, and μ_∞ = 10 000 $cm^2/(V\ s)$.[1−6,28] Figure 5 shows the current distribution in a stack of 13 monolayers of graphene at different gate bias conditions. It is interesting to note that at any given gate bias the current predominantly flows through the bottom layers in contrast to the 13 monolayer thick MoS_2 stack that had been discussed above. As shown in the associated cartoon in Figure 5 the layers close to the substrate become the "HOT-SPOT" in this stacked resistance network. The explanation for this phenomenon lies in the low values of λ and R_{int}. A low value of λ ensures that most of the charges in the back gate are mirrored by charges in the bottom layers close to the substrate, resulting in low resistance values for these layers. The layers close to the top are almost completely depleted and hence pose a high resistance for current flow. Accordingly current flows preferably in the lower layers. The small value of the interlayer resistance further enhances this situation by making the lower layers easily accessible. As the gate bias is increased, the intralayer resistance for each individual layer is decreased and hence more layers further away from the substrate start to contribute to the current flow. The total current through the system increases accordingly before being limited by the total interlayer resistance. In this material system a single-layer device will always outperform a multilayer device because of the particular combination of strong charge screening and small

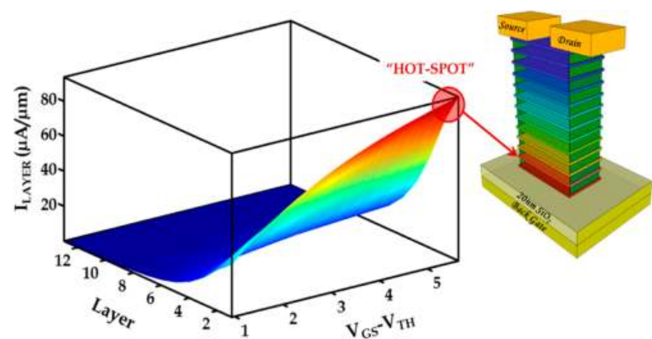

Figure 5. Current distribution among the individual layers of a 13 monolayers thick graphene stack at different gate bias conditions derived using the resistor network model. The cartoons show the location of the "HOT-SPOT" at a large gate bias condition.

interlayer resistance consistent with experimental findings on graphene.

Finally, the reader should agree that the "HOT-SPOT" for the current flow in a two-dimensional system is governed by the physical properties of the corresponding material that get manifested in the charge screening length λ and the interlayer coupling strength R_{int}. λ depends on the charge density in the channel and, therefore, can be related to the in-plane conductivity. The interlayer resistance (R_{int}), on the other hand, is inversely proportional to the out-of-plane conductivity. The position of the "HOT-SPOT" in a multilayer two-dimensional system, therefore, can be predicted from the conductivity anisotropy of the material. In realty λ and R_{int} cannot be assumed to be constant for a multilayer system and needs to be solved self-consistently for each gate bias. These are second-order effects and could potentially be introduced in a detailed analytical model with more model parameters. Our goal is to keep the model as simple as possible with minimum number of model parameters and still explain the experimental findings to a high degree of accuracy. Our assumption of constant λ and R_{int} explains the experimental results within 5% error margin (which is within acceptable limit). Moreover, our experimental data itself scatter by 10%. We, therefore, did not introduce these effects in our model.

In conclusion, we have used a unique approach of a channel length scaling study to provide first experimental insights into the current distribution among the individual layers of a multilayer MoS_2 system. We have also successfully applied a resistor network model including T-F charge screening and interlayer coupling to describe our experimental data quantitatively. Within this model, we were able to capture why the centroid of current distribution, the "HOT-SPOT", in a multilayer MoS_2 field-effect transistor migrates toward the top layers when the gate bias is increased. We have also explained how this current distribution plays a critical role in determining the effective contact resistance of this material system—a feature that cannot be explained within a conventional metal-to-semiconductor contact model. Finally, we have demonstrated that the current distribution in metal dichalcogenides is distinctly different from other two-dimensional layered systems like graphene.

■ AUTHOR INFORMATION

Notes

The authors declare no competing financial interest.

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■ REFERENCES

(1) Geim, A. K.; Novoselov, K. S. The rise of graphene. *Nat. Mater.* **2007**, *6*, 183−91.

(2) Meric, I.; Han, M. Y.; Young, A. F.; Ozyilmaz, B.; Kim, P.; Shepard, K. L. Current saturation in zero-bandgap, top-gated graphene field-effect transistors. *Nat. Nanotechnol.* **2008**, *3*, 654−9.

(3) Geim, A. K. Graphene: status and prospects. *Science* **2009**, *324*, 1530−4.

(4) Kim, K. S.; Zhao, Y.; Jang, H.; Lee, S. Y.; Kim, J. M.; Kim, K. S.; Ahn, J.-H.; Kim, P.; Choi, J.-Y.; Hong, B. H. Large-scale pattern growth of graphene films for stretchable transparent electrodes. *Nature* **2009**, *457*, 706−10.

(5) Lin, Y.; Dimitrakopoulos, C.; Jenkins, K. A.; Farmer, D. B.; Chiu, H.-Y.; Grill, A.; Avouis, Ph. 100-GHz Transistors from Wafer Scale Epitaxial Graphene. *Science* **2010**, *327*, 662.

(6) Palacios, T. Graphene electronics: thinking outside the silicon box. *Nat. Nanotechnol.* **2011**, *6*, 464−5.

(7) Dean, C. R.; Young, A. F.; Meric, I.; Lee, C.; Wang, L.; Sorgenfrei, S.; Watanabe, K.; Taniguchi, T.; Kim, P.; Shepard, K. L.; Hone, J. Boron nitride substrates for high-quality graphene electronics. *Nat. Nanotechnol.* **2010**, *5*, 722−6.

(8) Chen, Y. L.; Analytis, J. G.; Chu, J.-H.; Liu, Z. K.; Mo, S.-K.; Qi, X. L.; Zhang, H. J.; Lu, D. H.; Dai, X.; Fang, Z.; et al. Experimental realization of a three-dimensional topological insulator, Bi_2Te_3. *Science* **2009**, *325*, 178−81.

(9) Moore, J. E. The birth of topological insulators. *Nature* **2010**, *464*, 194−8.

(10) Kong, D.; Chen, Y.; Cha, J. J.; Zhang, Q.; Analytis, J. G.; Lai, K.; Liu, Z.; Hong, S. S.; Koski, K. J.; Mo, S.-K.; et al. Am-bipolar field effect in the ternary topological insulator $(Bi_xSb_{(1-x)})_2Te_3$ by composition tuning. *Nat. Nanotechnol.* **2011**, *6*, 705−9.

(11) Radisavljevic, B.; Radenovic, A.; Brivio, J.; Giacometti, V.; Kis, A. Single-layer MoS_2 transistors. *Nat. Nanotechnol.* **2011**, *6*, 147−50.

(12) Yoon, Y.; Ganapathi, K.; Salahuddin, S. How good can monolayer MoS_2 transistors be. *Nano Lett.* **2011**, *11*, 3768−73.

(13) Wang, H.; Yu, L.; Lee, Y.-H.; Shi, Y.; Hsu, A.; Chin, M. L.; Li, L.-J.; Dubey, M.; Kong, J.; Palacios, T. Integrated circuits based on bilayer MoS_2 transistors. *Nano Lett.* **2012**, *12*, 4674−80.

(14) Das, S.; Chen, H.-Y.; Penumatcha, A. V.; Appenzeller, J. High performance multilayer MoS_2 transistors with Scandium Contacts. *Nano Lett.* **2013**, *13*, 100−5.

(15) Fuhrer, M. S; Hone, J. Measurement of mobility in dual-gated MoS_2 transistors. *Nat. Nanotechnol.* **2013**, *8*, 146−7.

(16) Fang, H.; Chuang, S.; Chang, T. C.; Takei, K.; Takahashi, T.; Javey, A. High-performance single layered WSe_2 p-FETs with chemically doped contacts. *Nano Lett.* **2012**, *12*, 3788−92.

(17) Das, S.; Appenzeller, J. Screening and interlayer coupling in multilayer MoS_2. *Phys. Status Solidi Rapid Res. Lett.* **2013**, *7*, 268−273.

(18) Hisamoto, D.; Lee, W.-C.; Kedzierski, J.; Takeuchi, H.; Asano, K.; Kuo, C.; Anderson, E.; King, T.-J.; Bokor, J.; Hu, C. FinFET - A Self-Aligned Double-Gate MOSFET. *IEEE Trans. Electron Devices* **2000**, *47*, 2320−2325.

(19) Yu, B.; Chang, L.; Ahmed, S.; Wang, H.; Bell, S.; Yang, C.-Y.; Tabery, C.; Ho, C.; Xiang, X.; King, T.-J.; et al. FinFET Scaling to 10nm Gate Length. *IEDM Tech. Dig.* **2002**, 251−254.

(20) Doyle, B.; Boyanov, B.; Datta, S.; Doczy, M.; Hareland, S.; Jin, B.; Kavalieros, J.; Linton, T.; Rios, R.; Chau, R. Tri-Gate Fully-Depleted CMOS Transistors: Fabrication, Design and Layout. *Symp. VLSI Technol. Dig. Tech. Pap.* **2003**, 133−34.

(21) Doyle, B. S.; Datta, S.; Doczy, M.; Hareland, S.; Jin, B.; Kavalieros, J.; Linton, T.; Murthy, A.; Rios, R.; Chau, R. High Performance Fully-Depleted Tri-Gate CMOS Transistors. *IEEE Trans. Electron Devices* **2003**, *24*, 263−265.

(22) Sun, X.; Moroz, V.; Lu, Q.; Takeuchi, H.; Gebara, G.; Wetzel, J.; Ikeda, S.; Shin, C.; Liu, T.-J. K. Tri-Gate Bulk MOSFET Design for CMOS Scaling to the End of the Roadmap. *IEEE Electron Device Lett.* **2008**, *29*, 491−493.

(23) Lundstrom, M.; Guo, J. *Nanoscale Transistors: Device Physics, Modeling, and Simulation*; Springer Publication: New York, 2006.

(24) Ghani, T.; Mistry, K.; Packan, P.; Thompson, S.; Stettler, M.; Tyagi, S.; Bohr, M. Scaling Challenges and Device Design Requirements for High Performance Sub-50 nm Gate Length Planar CMOS Transistors. *Symp. VLSI Technol. Dig. Tech. Pap.* **2000**, 174−5.

(25) Stahl, H.; Appenzeller, J.; Martel, R.; Avouris, Ph.; Lengeler, B. Inter-tube coupling in ropes of single-wall carbon nanotubes. *Phys. Rev. Lett.* **2000**, *85*, 5186−9.

(26) Resta, R. *Phys. Rev. B* **1977**, *16*, 2717−22.

(27) Trani, F.; Ninno, D.; Cantele, G.; Iadonisi, G.; Hameeuw, K.; Degoli, E.; Ossicini, S. Screening in semiconductor Nano crystals: Ab initio results and Thomas-Fermi theory. *Phys. Rev. B* **2006**, *73*, 245430.
(28) Sui, Y.; Appenzeller, J. Screening and interlayer coupling in multilayer graphene field-effect transistors. *Nano Lett.* **2009**, *9*, 2973–7.