Which Photodiode to Use: A Comparison of CMOS-Compatible Structures

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***Abstract*—While great advances have been made in optimizing fabrication process technologies for solid state image sensors, the need remains to be able to fabricate high quality photosensors in standard CMOS processes. The quality metrics depend on both the pixel architecture and the photosensitive structure. This paper presents a comparison of three photodiode structures in terms of spectral sensitivity, noise and dark current. The three structures are n^+/p-sub, n-well$/p$-sub and p^+/n-well$/p$-sub. All structures were fabricated in a 0.5 μm 3-metal, 2-poly, n-well process and shared the same pixel and readout architectures. Two pixel structures were fabricated—the standard three transistor active pixel sensor, where the output depends on the photodiode capacitance, and one incorporating an in-pixel capacitive transimpedance amplifier where the output is dependent only on a designed feedback capacitor. The n-well$/p$-sub diode performed best in terms of sensitivity (an improvement of 3.5 $\times$ and 1.6 $\times$ over the n^+/p-sub and p^+/n-well$/p$-sub diodes, respectively) and signal-to-noise ratio (1.5 $\times$ and 1.2 $\times$ improvement over the n^+/p-sub and p^+/n-well$/p$-sub diodes, respectively) while the p^+/n-well$/p$-sub diode had the minimum (33% compared to other two structures) dark current for a given sensitivity.**

***Index Terms*—Active pixel sensors, CMOS, photodiodes.**

I. Introduction

SOLID-state image sensors have come a long way since the first CMOS [1] and CCD [2] sensors were described in the late 1960s. Since then, great advances have been made in both modalities of sensors. CCD imagers took the lead till the 1990s because CMOS fabrication technology was not sufficiently advanced to make use of the main advantage of CMOS imagers–the ability to integrate electronic circuits on the focal plane, in the same die. Advancements in CCD technology have revolved around optimizing fabrication techniques to improve the sensitivity, charge transfer efficiency, dark current, and noise performance among other specifications. By the mid 1990s, fabrication technology had improved to a point that there was a resurgence in CMOS imaging systems [3]–[5] that offered compact, single-chip, low-power devices. Innovative circuit design has led to CMOS imagers capable of imaging at several thousand frames per second [6], pixel pitches down to 1.4 μm [7], and computational imagers that can perform stereo vision [8], motion estimation [9] among others [10]. It was expected that CMOS imagers could share production lines with mainstream logic and memory fabrication, thereby delivering economies of scale. However, improving CMOS fabrication technology meant scaling down feature sizes. While this made CMOS imager fill factors comparable to CCDs, it introduced noise and nonlinear effects due to submicron features. Thus, to regain performance, CMOS fabrication technology had to be optimized for imaging, offsetting the advantages of being able to fabricate in a standard CMOS process [11]. Today high performance is available in both CMOS and CCD technologies, but with higher design complexity associated with CMOS than CCD technologies.

Clearly, the need still exists for high performance CMOS image sensors designed in standard CMOS processes. The key here is performance, which depends on the application. For example, stroboscopic imaging requires very high sensitivity while biological fluorescence imaging requires the dark current to be minimized. Since most of the parameters characterizing imagers are interdependent, application dependent tradeoffs need to be made for an optimal design. Certain applications are also wavelength specific, requiring knowledge of the spectral sensitivity of the detector.

The photodetector at the heart of most CMOS image sensors is a photodiode. While the ultimate performance of the sensor also depends on the pixel and peripheral circuitry, the photodiode plays a limiting role. Material parameters control photodiode performance and cannot be changed by a designer unless the CMOS fabrication procedure itself is modified.

Prior work comparing different photodiode structures has not been very systematic. Bhadri *et al.* simulated but did not measure spectral sensitivity and dark current for n-well$/p$-sub, n-well$/p^+$ photodiodes, and a pnp bipolar phototransistor in a 1.5 μm CMOS process [12]. Odiot *et al.* compared different photodiode geometries for a n-well$/p$-sub photodiode [13]. Li *et al.* measured the broadband sensitivity and dark response for n^+/p-sub and n-well$/p$-sub photodiodes using three and four transistor active pixel sensors in a 0.35 μm CMOS process [14]. Fowler *et al.* measured a higher response for an n-well$/p$-sub photodiode than for an n^+/p-sub using a three transistor pixel in a 0.35 μm CMOS process [15]. Tian *et al.* compared n^+/p-sub and n-well $/p$-sub photodiodes in 0.18μm CMOS process [16], where gate leakage currents on the order

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of photocurrents under normal lighting conditions require optimizing design beyond the photodiode selection, which is the focus of this work. The CMOS Minimal Array [17] developed by Janesick *et al.* presents a comprehensive comparison of pinned photodiodes, deep n-well and n-well photodiodes. Several different pixel circuits and silicon substrates were also compared.

We present a comparative study of three photodiode structures fabricated in a 0.5 μm 3-metal, 2-poly, n-well CMOS process. As elaborated in the following sections, the response of a pixel depends on the photodiode and the photodiode sense node capacitance. If not decoupled, one would measure the characteristics of the pixel rather than the photodiode. In this work, two pixel circuits were implemented, one of which allowed decoupling the photodiode capacitance from the pixel, allowing a true photodiode comparison. Section II discusses issues that control the sensitivity of a detector and describes the three structures tested. Sections III and IV detail the pixel circuits and chip architecture. Section V summarizes the results and Section VI concludes this paper.

II. Phototransduction and Photodiode Structures

Phototransduction starts with photon incidence on a detector. If the photon energy is greater than the bandgap of the material, $h\nu > E_g$, electron-hole pairs (EHPs) are generated. The quantum efficiency (QE) of a detector is defined as the percentage of photons hitting the photoreactive surface that produce an EHP. QE is only part of the measure of sensitivity of the detector. Also important is the collection efficiency which is the fraction of generated EHP that contribute to a current flow external to the detector. Considering phototransduction in a pn junction, EHP are generated all over the p and n regions that form the junction. In the bulk of the junction, these electron and holes have a high probability of recombining and are thereby lost. In the depletion region and a diffusion width on either side of it, however, due to the electric field existing across the depletion region, the electrons and holes are swept away, leading to a useful photocurrent [18]. If W, L_p, L_n denote the depletion region width, hole diffusion length, and electron diffusion length, respectively, the photocurrent I_{Op} can be written as [19]

$$I_{Op} = qg_{Op}A(W + L_n + L_p) \tag{1}$$

where g_{Op} is the light induced rate of EHP generation, q is the electronic charge and A is the total area of the junction including the bottom and sidewalls. The width of the depletion region depends on N_a and N_d, the respective doping concentrations of the p and n type materials used for the junction and on the voltage V applied across it [19]

$$W = \sqrt{\frac{2\epsilon(V_{bi} - V)}{q}\left(\frac{1}{N_a} + \frac{1}{N_d}\right)} \tag{2}$$

where ϵ is the permitivitty of silicon. V_{bi} is the built-in diode potential and is given by

$$V_{bi} = \frac{kT}{q}\ln\frac{N_a N_d}{n_i^2} \tag{3}$$

where n_i is the intrinsic carrier concentration of silicon. k, q and T denote the Boltzmann constant, electronic charge and absolute temperature, respectively. In voltage mode active pixel sensors, the photocurrent then discharges the photodiode capacitance which had been precharged to some reference level using a reset signal. The capacitance C_j of the junction is given by

$$C_j = \epsilon\frac{A}{W} \tag{4}$$

where W is defined in (2). Clearly, the output voltage signal of the photodiode will depend on the photocurrent and on the junction capacitance. From (1)–(4), these depend on the doping concentrations of the p and n type regions of the junction.

In addition to the junction characteristics, the location of the junction also contributes to spectral sensitivity. As mentioned in Section II, charge carriers can diffuse a diffusion length before they recombine and are lost. In the case of a shallow junction, a fraction of the EHP generated below the junction will start diffusing deeper into the material, away from the junction, and will not be collected. However, the EHP generated above the junction cannot diffuse away into the bulk of the material and are much more likely to get collected. Thus, a deeper junction improves the collection efficiency leading to a higher sensitivity. This effect is enhanced for long wavelength photons which penetrate more into the material and generate EHP deeper in the bulk [20]. The processing steps needed to create a highly doped region are different from those required to create a lightly doped one. Thus, the depth of a junction is indirectly related to the doping concentration of the material used to create it. Typically, low doping is achieved by diffusion which results in deeper junctions, while regions of high dopant concentration are created using ion implantation, leading to shallower junctions [21].

Apart from the sensitivity, other photodiode parameters like dark current, thermal and shot noise also depend on the diode material. Dark current is a result of random thermal EHP generation in the absence of light. EHPs are generated all over the material but the most significant contribution comes from surface states at the face of the semiconductor material [22]. If the thermal rate of EHP generation is g_{Th}, similar to (1), the dark current, I_{Dk}, can be written as [19]

$$I_{Dk} = qg_{Th}A(W + L_n + L_p) \tag{5}$$

g_{Th} depends on the absolute temperature and also on certain material properties like the defect density in the crystal structure which, in turn, depends on the photodiode material and structure. Thermal noise on the photodiode capacitance due to the thermal agitation of electrons is given by

$$v_n = \sqrt{\frac{kT}{C_j}}. \tag{6}$$

Shot noise is due to the quantized nature of the phototransduction and is related to the photocurrent

$$i_n = \sqrt{2qI_{Op}\Delta f} \tag{7}$$

where the noise is measured over a bandwidth of Δf. Since I_{Op} depends on the photodiode, so does the shot noise.

From the above discussion, it is obvious that several parameters of photosensing using pn junction diodes depend on the structure and type of the junction. In standard n-well CMOS processes, there are three ways to create a pn junction. We

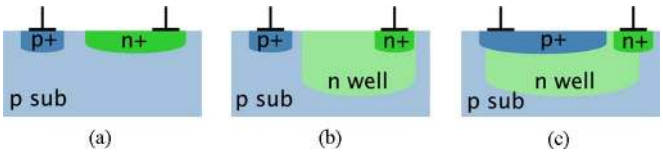

Fig. 1. Schematic drawings of the three photodiode structures—(a) n^+/p-sub, (b) n-well/p-sub, and (c) p^+/n-well/p-sub. Note the larger depletion region and the deeper junction in (b) and (c) and the pinned detector surface in (c). Fabrication design rules require larger minimum sizes and separation for n-wells. Thus, n^+/p-sub photodiodes can be more compact than the other two structures.

now briefly describe the structures and the motivation behind choosing these three.

A. n^+/p-sub

Fig. 1(a) shows the most straightforward structure used to create a photodiode. In terms of design rules, this structure is the most compact. It is formed by creating a highly doped n region in the p substrate. Due to the high doping concentration of the n^+ implant (compared to an n-well diffusion), from (2), the depletion region width W is small. This leads to a reduction in the collection efficiency. Since W is small, from (4), the junction capacitance C_j is large. This results in a low charge-to-voltage conversion. Since the n region is created by ion implantation, the junction is relatively close to the surface. This causes a further reduction in the collection efficiency, specially for longer wavelengths. We considered the n^+/p photodiode as the reference design and expect improvements over it in the other two structures.

B. n-well/p-sub

This photodiode uses the lightly doped n-well diffusion to create a pn junction in the p substrate, as shown in Fig. 1(b). The lower doping concentration of the n-well (compared to an n^+ implant) increases the depletion width W and this decreases the junction capacitance. The larger depletion region should lead to a better collection efficiency and the smaller capacitance should improve the charge-to-voltage conversion. Since the n-well diffusion is deeper than an n^+ implant, the junction is deeper and more efficient at capturing long wavelength photons compared to a n^+/p-sub junction. The increased depth also creates significant depletion regions along the sidewalls of the junction, further improving the collection efficiency. However, this increased junction area, caused by higher sidewalls due to the deeper junction, will also increase the junction capacitance C_j, offsetting some of the improvement in the charge-to-voltage conversion resulting from the smaller W. Design rules require larger minimum spacing and minimum widths for n-wells compared to n^+ regions. Thus, given a constant size, a pixel with an n-well photodiode will have a lower fill factor than one with an n^+/p-sub photodiode.

C. p^+/n-well/p-sub

This photodiode is similar to the n-well/p-sub diode above, but adds a p^+ implant covering the n-well diffusion. This "pinned" structure was first developed for CCD imagers [23] and subsequently reported for CMOS imagers as well [24]. The diode is drawn in Fig. 1(c). The implant serves two purposes. First, in the same area, there are now two pn junctions—the p^+/n-well and the n-well/p-sub. This creates an effective depletion region even larger than the n-well/p-sub diode and should lead to the highest collection efficiency among the three structures. However, depletion capacitances from the two junctions add in parallel, lowering the charge-to-voltage conversion. Second, as mentioned before, the main source of dark current is from the interface states at the surface of the junction. If the free charge carrier concentration at the interface is high, the interface states will be occupied and not contribute to EHP generation. Since the p^+ layer has a high hole concentration, we expect this photodiode to have lower dark current than the n-well/p-sub structure where the surface layer does not have a high free carrier concentration.

III. Pixel Circuits

As alluded to in Section II, the current output of a pixel depends on the QE of the photodiode that fixes the number of EHP per photon and the collection efficiency that decides the fraction of the generated EHP that contribute to the photocurrent. The subsequent voltage output of the pixel depends on the photocurrent and the photodiode capacitance. In order to compare photodiodes sensitivities *per se*, the effect of the capacitance must be removed. One of the two implemented circuits accomplishes this by unlinking the photodiode capacitance from the pixel operation. We now present the two pixel architectures that were used in this work. One is the standard three transistor active pixel sensor and the other is a pixel that includes a capacitive transimpedance amplifier within itself.

A. 3 Transistor (3T) Pixel

The circuit for the three transistor (3T) active pixel sensor [1] is shown in Fig. 2(a). The pixel is reset using transistor M_1 which charges the photodiode capacitance $C_{\rm PD}$ almost to $V_{\rm DD}$. After the reset is released, the photocurrent $I_{\rm PD}$ discharges the capacitance. The output of the pixel can be accessed through the source follower transistor M_2 and the access transistor M_3. The output $v_{\rm out}$ can be written as

$$v_{\rm out} = G_{\rm SF}\frac{1}{C_{\rm PD}}\int I_{\rm PD}dt \tag{8}$$

where $G_{\rm SF}$ is the subunity gain of the source follower. The output of the pixel depends on the photodiode capacitance $C_{\rm PD}$. Thus, this pixel, while extremely simple in design and operation, cannot be used to compare photodiodes without the knowledge of their capacitance. Junction capacitances are generally not known accurately. Since this is the oldest and most common pixel circuit, we included the 3T APS in the comparison and present this data as representative of the pixels and not of the photodiodes.

B. Capacitive Transimpedance Amplifier (CTIA) Pixel

A simplified schematic for the CTIA pixel [25], [26] is shown in Fig. 2(e). The amplifier A was realized as a single-stage cascoded common source amplifier. At a bias current of 200 nA, 1 pF capacitive load, and 3.3 V supply, simulations indicate a gain of 85 dB and a gain-bandwidth product of 675 kHz. Transistor M_1 acts as the reset switch, charging the photodiode capacitance to the inversion point of the amplifier. This sets the reverse bias across the photodiode. The capacitor $C_{\rm fb}$ acts in

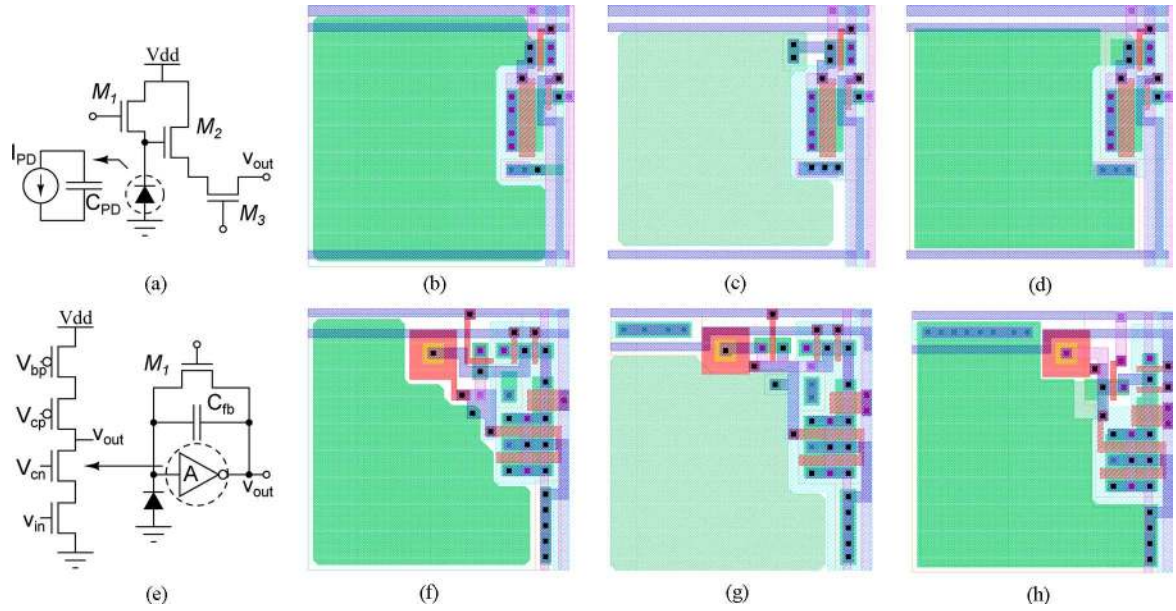

Fig. 2. Pixel circuits and layouts: (a) is the 3T APS and (b), (c), and (d) are layouts of the 3T APS with an n^+/p-sub, n-well/p-sub, and p^+/n-well/p-sub photodiode, respectively, (e) is a simplified schematic of the CTIA APS and (f), (g), and (h) are layouts of the CTIA APS with an n^+/p-sub, n-well/p-sub, and p^+/n-well/p-sub photodiode, respectively. All pixels were sized 30 μm $\times$ 30 μm. Note the different photodiode geometries due to different design rules. The differences are summarized in Table I.

negative feedback. With a sufficiently high gain amplifier and $C_{\rm fb} \ll C_{\rm PD}$, the circuit effectively pins the photodiode output node and forces the photocurrent to charge $C_{\rm fb}$. The output $v_{\rm out}$ can be written as

$$v_{\rm out} = -\frac{1}{C_{\rm fb}} \int I_{\rm PD} dt. \tag{9}$$

The circuit cancels out the effect of the photodiode capacitance and the output signal depends only on the photocurrent and a known capacitance which is a circuit design parameter. The negative sign comes from the inverting nature of the amplifier. Parasitic capacitances due to M_1 do not effect $C_{\rm fb}$ because they can be lumped into either the photodiode or the load capacitance of the circuit. Any process dependent mismatch in $C_{\rm fb}$ will manifest as gain error across pixels.

IV. Chip Architecture

In the last two sections, we described three photodiode structures and two pixel circuits. Two versions of the CTIA pixel were designed, with the feedback capacitance being 5 and 10 fF. The chip was designed in a 3 metal, 2 poly 0.5 μm n-well CMOS technology. Each of the three circuits were laid out with the three kinds of photodiodes resulting in nine pixel arrays. Fig. 2(b)–(d) shows the layouts of the three transistor APS using an n^+/p-sub, n-well/p-sub and p^+/n-well/p-sub photodiode, respectively. Fig. 2(f)–(h) shows the layout of the CTIA APS using an n^+/p-sub, n-well/p-sub and p^+/n-well/p-sub photodiode, respectively. This CTIA pixel had $C_{\rm fb} = 5$ fF. The transistor sizing within each pixel circuit was kept the same. The pixel pitch was kept constant at 30 μm across all the pixels. Due to differences in design rules and given the same pixel size, the photodiode size across all structures was not constant. Table I summarizes the photodiode geometries in all the pixels.

In order to obtain statistically significant comparisons, 7 $\times$ 7 arrays of each pixel were designed. For each array type, a two-pixel wide border was not considered in the analysis to minimize effects from the peripheral pixels that see a different surrounding environment from the central pixels. Using an analog multiplexer consisting of several transmission gates, the output of each individual pixel in the center 3 $\times$ 3 elements of each array could be connected to an output buffer. In all, 81 pixels (9 arrays of 3 $\times$ 3 pixels each) were individually interrogated.

TABLE I
Photodiode Geometries Across Pixels

Photodiode type	APS type	Area (μm^2)	Perimeter (μm)	Fill factor (%)
n^+/p-sub	3T	671.85	120.8	74.7
	CTIA 10 fF	512.86	102.5	57.0
	CTIA 5 fF	523.89	101.6	58.2
n-well/p-sub	3T	531.81	99.8	59.1
	CTIA 10 fF	513.54	96.4	57.1
	CTIA 5 fF	519.52	95.9	57.7
p^+/n-well/p-sub	3T	541.08	105.2	60.1
	CTIA 10 fF	485.10	97.5	53.9
	CTIA 5 fF	494.01	97.5	54.9

V. Results

Fig. 3(a) shows the micrograph of the 1.5 mm $\times$ 1.5 mm die with all the test structures. The chip was powered by two independently regulated 3.3 V supplies—one for all the pixel arrays and one for all the digital circuits. For characterization, a computer controlled the digital inputs to the chip, connecting a specified pixel to the output buffer. Incident light was controlled using a Fluorolog-3 spectrofluorometer (Jobin Yvon, NJ). Light intensity was measured using a model 1930 optical power meter (Newport, NY). Fig. 3(b)–(d) show the measured pixel response of the 3T APS, 10 fF CTIA APS, and the 5 fF CTIA APS, respectively, under broadband illumination. All pixels had the n-well/p-sub photodiode. The exposure time was kept constant

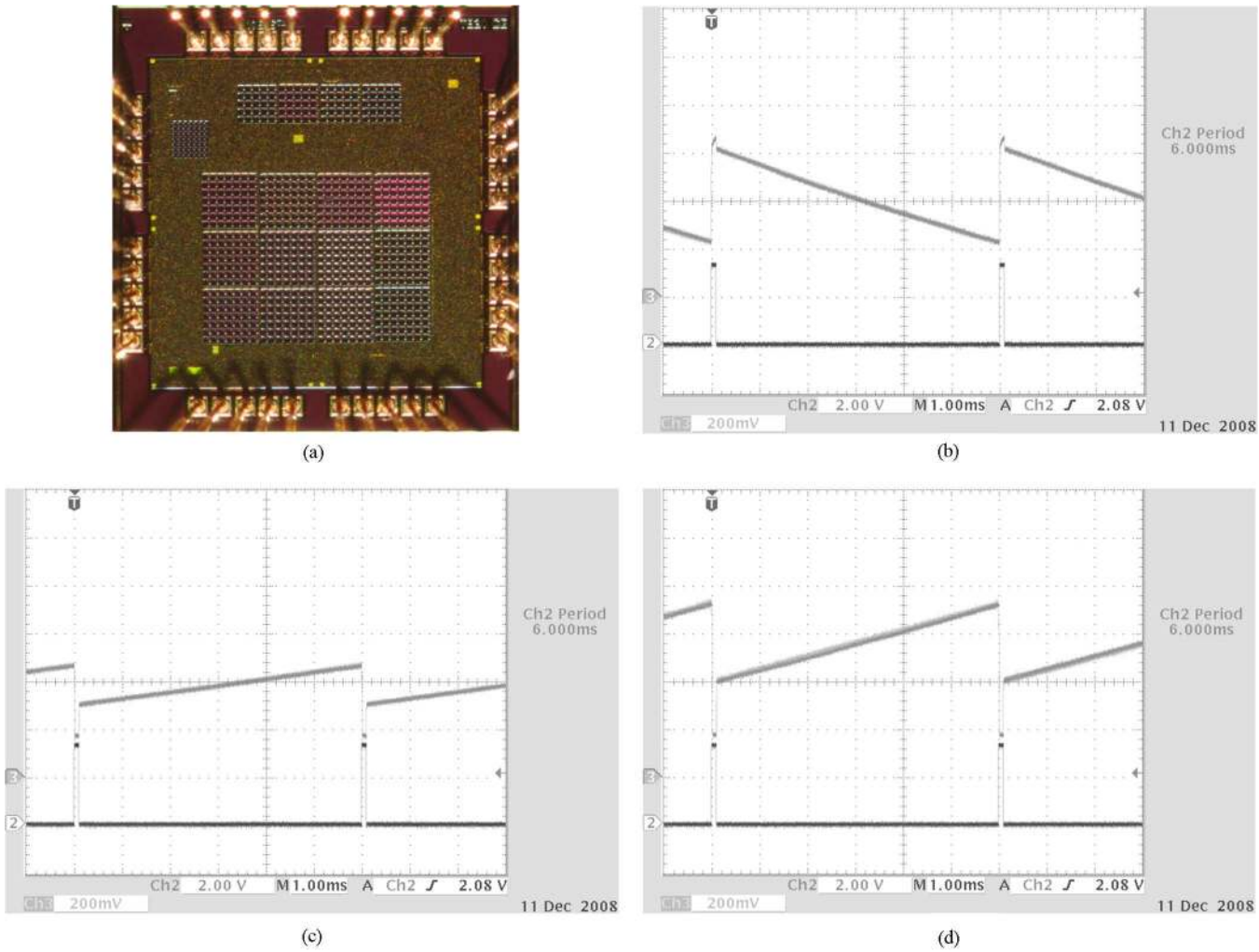

Fig. 3. (a) Micrograph of the 1.5 mm × 1.5 mm die showing arrays of the test pixels and other test structures. Panels (b), (c), and (d) show measured pixel outputs from the 3T APS, 10 fF CTIA APS, and the 5 fF CTIA APS, respectively. All APS pixels are implemented with n-well/p-sub photodiodes. The CTIA APS was covered by an OD 1.8 neutral density filter attenuating incident light by a factor of 62.5.

at 6 ms and a neutral density filter was used to attenuate the incident light by a factor of 62.5 (OD 1.8) for the CTIA APS. Note the different signs of slopes for the CTIA and 3T APS.

The analog output of the chip was digitized to 16 bits using a NI6031 data acquisition card (National Instruments, TX) and read into a computer for analysis. The slope of the voltage output of the pixel was averaged for a thousand exposures as a measure of the sensitivity. The standard deviation in the slope measurements was taken as the noise of the detector. It should be noted that this measure takes into account the electrical noise added by the readout circuitry. However, a single readout path was shared by all the 3T APS and one by all the CTIA APS. The data were collected at illumination levels leading to noise beyond the read noise floor. Thus, we expect the measurements to be representative of the inherent photodiode noise. All data were averaged across the nine pixels of each kind.

Prior to photodiode comparison, the readout paths of the pixels were characterized. While the simplified CTIA pixel shown in Fig. 2(e) is self-sufficient, the 3T APS shown in Fig. 2(a) requires a current sink to be attached to the output node for the source follower to work. Also, while the 3T APS output decreases as the photogenerated EHP are collected, the CTIA output increases due to the inverting nature of the amplifier. Due to these differences in the APS circuits, all CTIA pixels shared one readout circuit and all 3T pixels shared a different one.

In order to measure the dc gains of the two different readout paths, the output nodes of the pixels were driven by a triangular wave generated using a function generator [16]. The outputs of the pixels were acquired using the data acquisition card. For the CTIA pixels, the readout path consisted only of a large PMOS transistor configured as a common source amplifier, buffering the output. The measured gain was 0.82. The 3T APS had an NMOS transistor of the same size as a voltage buffer, but also had an in-pixel source follower that contributed additional gain (8). The measured gain was 0.64. By dividing the measured responses of the pixels by the respective gains, the photodiode outputs were calculated for subsequent analysis.

A. *Spectral Sensitivity*

The spectrofluorometer was programmed to step the wavelength of light from 400 to 860 nm in steps of 5 nm. Incident

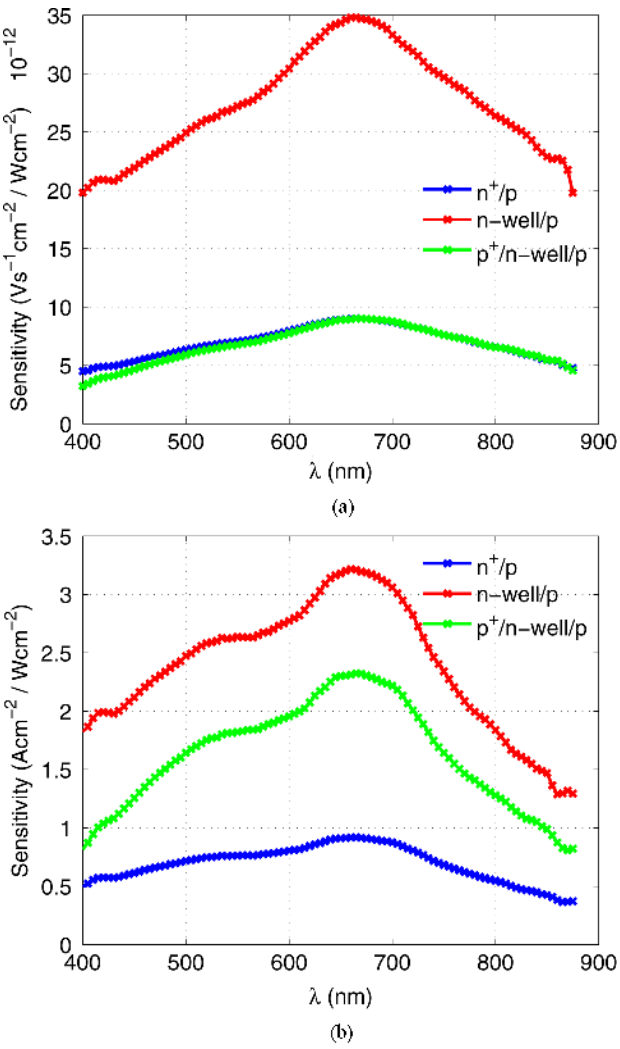

Fig. 4. Comparison of the spectral sensitivities of the three photodiodes. (a) Compares the photodiode capacitance dependent sensitivity measured from the 3T APS. (b) Compares circuit-independent sensitivities of the three photodiodes measured from the CTIA APS.

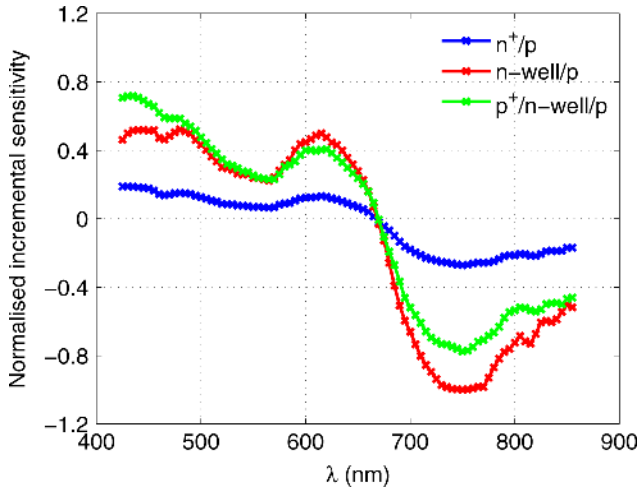

Fig. 5. Incremental sensitivity of the photodiodes calculated using the data from the CTIA APS. All data were normalized to the maximum incremental sensitivity across all photodiodes.

light irradiance was measured for each of the wavelengths. The slope of the pixel output (for the 3T APS) and the photocurrent (for the CTIA APS) was normalized by the incident irradiance (Wm^{-2}) and the photodiode area. At this point, we would like to explain the rationale behind normalizing by the irradiance and not by the radiant flux (W) on the pixel which can be obtained by multiplying the irradiance and the pixel area. Using the radiant flux assumes that none of the collected EHP were generated beyond the perimeter of the pixel. Since electron and hole diffusion lengths are larger than our pixel dimensions, each photodiode collects from an unknown area larger than itself. Thus, one cannot calculate the optical power (W) which is responsible for the current through one photodiode. While one can measure the response of a photodiode by optically confining the illumination to only one pixel, that is not the normal mode of operation of imager arrays. Therefore, we used the irradiance as a measure of the incident power.

Fig. 4(a) shows the spectral sensitivities for all three photodiodes using the three transistor APS. This data is representative of the pixels and not of the photodiodes due to the photodiode capacitance figuring in the output (8). The higher sensitivity of the n-well/p-sub diode over the n^+/p diode is due to a combination of better quantum and collection efficiencies and smaller capacitance. While the response of the p^+/n-well/p-sub diode was expected to be better than that of the n^+/p-sub diode, this is not the case, probably due to the increased photodiode capacitance. At short wavelengths, the p^+/n-well/p-sub sensitivity is actually lower, possibly due to the p^+ implant shielding some of the blue photons.

Fig. 4(b) shows the same data for the 10 fF CTIA APS. For this pixel, since the integrating capacitance is known, it is possible to calculate the photocurrent from the output. The sensitivity is calculated as the photocurrent per unit area of the photodiode for a given irradiance. A similar calculation was made for the 5 fF CTIA pixel. The data were within 5% of the 10 fF CTIA pixel for all wavelengths and are not shown. The CTIA pixels allows a true comparison of photodiode sensitivity, irrespective of the APS design. The improvement in sensitivity of the n-well/p-sub diode over the n^+/p diode is now totally due to the increase in quantum and collection efficiencies. Since the effect of the photodiode capacitance is eliminated, the p^+/n-well/p-sub diode can be seen to be more sensitive than the n^+/p-sub diode.

Another point to note from the data is the different rates of changes of the sensitivities as a function of the wavelength of the incident light for different photodiodes. Fig. 5 shows this trend by plotting the normalized "incremental" sensitivity for the three photodiodes using data from the CTIA APS. Incremental sensitivity (S^i) was defined as the derivative of the sensitivity (S) with respect to the wavelength (λ). The data were normalized as $S^i_N = [\partial S/\partial\lambda]/[\max(\mathrm{abs}(\partial S/\partial\lambda))]$ where a single maximum was calculated for the normalization across all three photodiodes.

It can be seen from the data that the dependence of the sensitivity on the wavelength is not the same across all the photodiodes. If that were the case, one would expect to see similar trends in S and S^i i.e., $|S^i_{n-\mathrm{well}/p}| > |S^i_{p^+/n-\mathrm{well}/p}| > |S^i_{n^+/p}|$ where $|\cdot|$ denotes the absolute value. Although this was generally

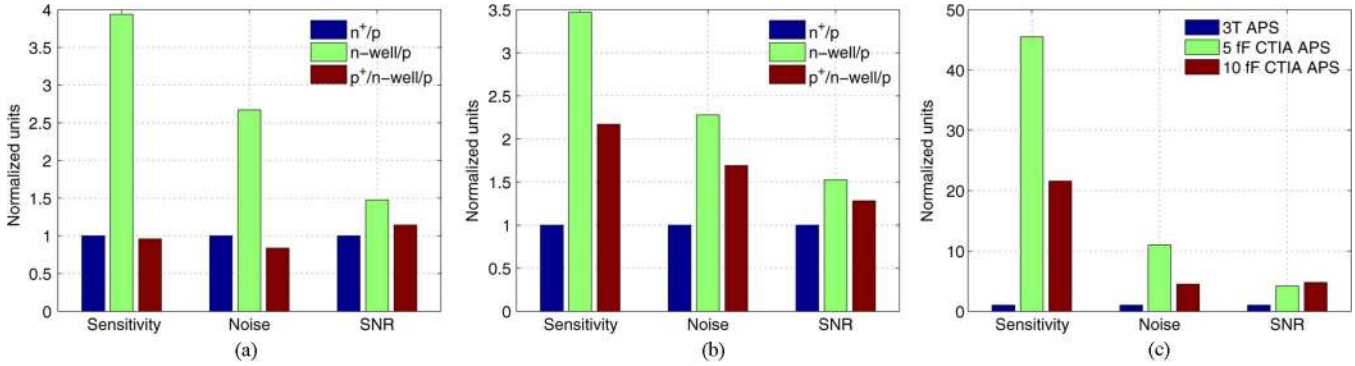

Fig. 6. Comparison of sensitivity, noise, and SNR averaged over all wavelengths for all photodiodes using data from: (a) photodiode capacitance dependent 3T APS, and (b) circuit-independent CTIA APS. Panel (c) compares the same metrics across different APS topologies using an n-well/p-sub photodiode.

true, as the light wavelength was changed from 400 to 580 nm, $|S^i_{p^+/n-\text{well}/p}| > |S^i_{n-\text{well}/p}|$. This indicates that the sensitivity of the p^+/n-well/p-sub diode is increasing faster than that of the n-well/p-sub diode. This supports our conjecture that the p^+ implant shields some of the short wavelength light incident on the pixel. As the wavelength and thereby the penetration depth increases, the structure recovers from the aforementioned disadvantage, leading to a higher rate of increase. The incremental sensitivity data from the 3T APS is not as instructive, due to the confounding factor of the photodiode capacitance and is not shown.

B. Sensitivity, Noise and Signal-to-Noise Ratio (SNR)

To obtain a relative comparison of the sensitivity, noise and signal-to-noise ratio (SNR) of the different pixels and photodiodes, the average sensitivity and noise of each structure were calculated over the entire wavelength range. Fig. 6(a) shows this data for the three transistor pixel. Sensitivity, noise, and SNR were separately normalized by the respective measurements for the n^+/p photodiode. Again, these measurements are representative of the pixel and not of the photodiode. As expected from the spectral sensitivity data, the n-well/p-sub photodiode performs the best due to higher quantum and collection efficiencies and a small capacitance. While, it also has the maximum noise, possibly due to a larger photocurrent and smaller capacitance, the SNR for the n-well/p-sub diode is still the highest. The p^+/n-well/p-sub and n^+/p perform almost similar because while the former has better collection efficiency, it also has a larger capacitance offsetting the advantage.

To perform circuit-independent photodiode comparison, data were used from the 10 fF CTIA pixel to compute the same metrics. This is shown in Fig. 6(b). While the n-well/p-sub diode still outperforms the other two, the p^+/n-well/p-sub diode is clearly more sensitive than the n^+/p. The same metrics were also calculated from the data for the 5 fF CTIA pixel. The results were within 5% of the above and are not shown.

Fig. 6(c) shows the normalized sensitivity, noise, and SNR statistics for the three different pixel structures—the 3T APS and the CTIA APS with C_{fb} set to 5 and 10 fF. Since photodiode capacitance was not known for the 3T APS, sensitivities for all APS were calculated as the slope of the voltage output. All three pixels used n-well/p-sub photodiodes. As can be seen, the effect of the photodiode capacitance plays a very important role in the pixel output. For an n-well/p-sub photodiode of the relevant geometry, $C_{\text{PD}} \gg 10$ fF. Thus, the response of the 3T APS which depends on C_{PD} is much lower than that of the CTIA APS. Between the two CTIA pixels, the ratio of the sensitivities is related to the ratio of the feedback capacitances and is approximately equal to 2. One would expect the noise of the CTIA APS to be higher since the sensitivity is higher. However, the CTIA pixels employ an active reset that attenuates the reset noise which is a major component of the total noise. An analysis of the noise [27], [28] is beyond the scope of this paper.

TABLE II
PHOTODIODE DARK CURRENT COMPARISON

Photodiode type	Dark current (nA/cm^2)	DTOP (nW/cm^2)
n^+/p-sub	96.2	0.14
n-well/p-sub	363.4	0.15
p^+/n-well/p-sub	90.3	0.05

C. Dark Current

Table II compares the dark currents for the photodiodes. Since all the parameters in (9) are known, the dark current can be calculated as current per unit area using the CTIA pixels. Dark current erodes the dynamic range and the low-light sensitivity of a detector. However, a simple analysis reveals that the ratio of the dark current to the sensitivity is a truer metric of photodiode performance. The ratio gives the minimum optical power above which the photocurrent is larger than the dark current. Ideally, this quantity should be as small as possible to allow low intensity and high dynamic range imaging. We term this ratio the dark threshold optical power (DTOP). Using photodiode sensitivity data of the CTIA pixels from Section V-B, Table II also reports the DTOP values for all the structures. Note that the argument regarding incident power measurement presented in Section V-A is applicable here as well, leading to DTOP values being measures of irradiance rather than radiant flux.

The deeper junction in the n-well/p-sub diode probably accounts for increase of dark current over the n^+/p diode because virtually all dark EHP generated above the junction are collected. As discussed in the motivation behind the p^+/n-well/p-sub diode, the p^+ protective layer leads to a reduction in the dark current over the n-well/p-sub by reducing the number of free interface states. This reduction is due to

the high free carrier concentration of the p^+ layer that causes the interface states to be occupied and thereby unavailable for EHP generation. In terms of the DTOP, the improved quantum and collection efficiencies of the p^+/n-well/p-sub diode over the n^+/p diode and its lower dark current compared to the n-well/p-sub diode give it the edge over the other two.

VI. Conclusion

We have presented a comparison of n^+/p-sub, n-well/p-sub and p^+/n-well/p-sub photodiodes fabricated in a 0.5 μm 3-metal, 2-poly, n-well CMOS process. The photodiodes were characterized using two APS designs—the three transistor APS where the measurements depend on unknown photodiode capacitances and a capacitive transimpedance amplifier APS where a designed capacitance allows the photocurrents to be inferred. The measured trends were in agreement with theoretical predictions based on the physical characteristics of the photodiodes. In terms of sensitivity, the n-well/p-sub diode performs the best, with an improvement of 3.5 and 1.6 times over the n^+/p-sub and p^+/n-well/p-sub diodes, respectively. The signal-to-noise ratio was also higher by a factor of 1.5 and 1.2, respectively. The p^+/n-well/p-sub photodiode had 67% lower dark current per unit sensitivity compared to the other two diodes.

One question not addressed in this work is the effect of scaling down the pixels. In this comparison, the pixel size was a relative large 30 μm in 0.5 μm technology. This allowed comparable fill factors for all three kinds of diodes, even though the design rules vary considerably. This might not be the case in a high density array where a small pixel size neccesitates a small photodiode. A comparison across several technologies would also be very useful.

Nevertheless, to the best of our knowledge, this is the first report of a thorough comparison of photodiodes in a standard n-well CMOS process. As outlined earlier, different measures of photodiode performance are interlinked. Often, a tradeoff needs to be made between these parameters. As an example, although the n-well/p-sub and p^+/n-well/p-sub photodiodes seem to be superior to the n^+/p-sub photodiode, design rules dictate them to occupy more area on silicon. Thus, if the application calls for very high resolution imaging and illumination is not at a premium, the n^+/p-sub photodiode is the most suitable. On the other hand, fluorescence imaging is a photon-starved process. Increasing incident light intensity is not advisable since it causes rapid photobleaching of the dyes. Thus, the photodiode of choice would be one with high sensitivity and low dark current—the p^+/n-well/p-sub photodiode. The aim of this work was to compare photodiodes in a standard CMOS process, thereby quantifying the tradeoffs in the different structures. In closing, we hope this work to be useful to CMOS image sensor designers, looking to choose the most appropriate photodiode based on the target application.

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