Wide-Range Adaptive RF-to-DC Power Converter for UHF RFIDs

Mahmoud H. Ouda, *Student Member, IEEE*, Waleed Khalil, *Senior Member, IEEE*, and Khaled N. Salama, *Senior Member, IEEE*

***Abstract*—A wide-range, differential, cross-coupled rectifier is proposed with an extended dynamic range of input RF power that enables wireless powering from varying distances. The proposed architecture mitigates the reverse-leakage problem in conventional, cross-coupled rectifiers without degrading sensitivity. A prototype is designed for UHF RFID applications, and is implemented using 0.18 μm CMOS technology. On-chip measurements demonstrate a sensitivity of −18 dBm for 1 V output over a 100 kΩ load and a peak RF-to-DC power conversion efficiency of 65%. A conventional, fully cross-coupled rectifier is fabricated alongside for comparison and the proposed rectifier shows more than 2× increase in dynamic range and a 25% boosting in output voltage than the conventional rectifier.**

***Index Terms*—AC-DC converter, adaptive, CMOS, energy harvesting, rectifiers, RFID, self-bias, UHF, wireless powering.**

I. Introduction

WIRELESS powering is the key enabler for many applications starting from RFIDs, wireless sensors, and biomedical devices to wirelessly powered electric vehicles [1]–[3]. The heart of any wireless power receiver is the rectifier which is the RF-to-DC power converter. The operating range of the wireless powering system is mainly determined by the rectifier sensitivity which is defined as the minimum input RF power required to generate a usable, output DC voltage. Also, its overall efficiency is significantly limited by the RF-to-DC power conversion efficiency (PCE) of the rectifier which is the ratio of the DC output power to the RF input power [2].

A lot of research has been conducted to improve the sensitivity and PCE of RF-to-DC power converters [2]–[5] or to increase their power handling capability [6] or to minimize their impedance sensitivity to the change of loading and power levels [7]. One of the most common architectures is the fully cross-coupled (FX) rectifier [2]. A schematic for a single-stage, FX rectifier is shown in Fig. 1. In this cross-coupled scheme, the full RF input signal swing is applied differentially to the gate-source terminals of the four rectifying transistors. This improves the rectifier sensitivity and enables it to operate at lower input RF power levels. Moreover, during the charging time, the rectifying transistors operate in linear region with low drop voltages (less than their threshold voltages as compared to diode-connected rectifiers). Therefore, they can achieve lower power dissipation and hence higher RF-to-DC power conversion efficiency.

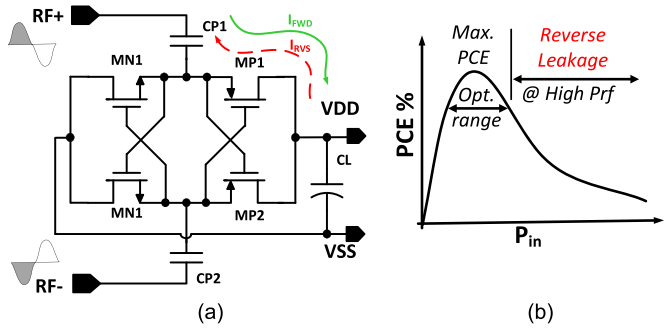

Fig. 1. (a) Schematic of single-stage, cross-coupled rectifier and (b) its power conversion efficiency versus RF input power.

Unfortunately, this cross-coupled scheme suffers from an intrinsic, reverse leakage current caused by the bidirectionality of MOS devices. The rectifying transistors MP1, 2 conduct in forward direction and charge the output DC voltage as long as the instantaneous RF input voltage is higher than the output DC voltage. However, once the RF voltage decreases below the output DC voltage, the rectifying transistors MP1, 2 conduct in reverse direction and discharge the output DC voltage during the RF switching intervals. This reverse leakage increases as the RF input power rises, resulting in large degradation in the power conversion efficiency, as shown in Fig. 1(b) [2].

In [8], an adaptive, reconfigurable rectifier stage is proposed for HF RFIDs at 13 MHz. It utilizes RF switches and active diodes, which are composed of rectifying transistors driven by fast comparators to shorten the RF switching time in order to minimize the reverse current. However, this approach is not applicable in high-frequency applications, such as UHF 900 MHz RFIDs due to the increasing losses in RF comparators and switches. A multi-stage, adaptive technique is presented in [9], [10] to reconfigure the inter-stage connectivity from parallel to series stages based on the RF power level. Whereas this extends the optimal range of the RF power, it requires the use of multiple stages with high capacitive and low resistive input impedance, further complicating the matching network.

In this letter, we propose a wide-range, differential RF-to-DC power converter stage using an adaptive, self-biasing technique. The proposed architecture extends the optimal input range at which the rectifier maintains 90% of its peak power conversion efficiency over wider input range than conventional rectifiers. This is achieved without trading off the sensitivity advantage of the cross-coupled scheme. The letter is organized as follows: Section II describes the proposed adaptive rectifier design while

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M. H. Ouda and K. N. Salama are with King Abdullah University of Science and Technology (KAUST), Thuwal 23955-6900, Saudi Arabia (e-mail: mahmoud.ouda@kaust.edu.sa; khaled.salama@kaust.edu.sa).

W. Khalil is with ElectroScience Laboratory, The Ohio State University, Columbus, OH 43212 USA (e-mail: khalil@ece.osu.edu).

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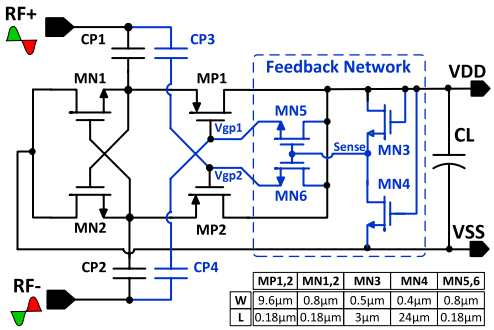

Fig. 2. Schematic of the proposed adaptive rectifier.

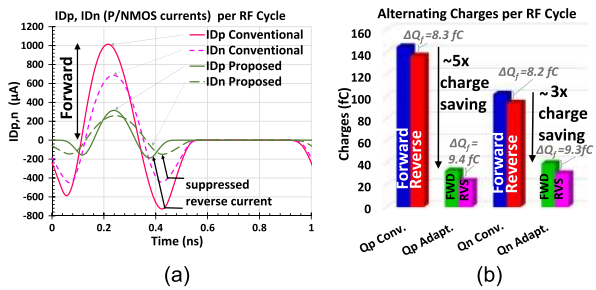

Fig. 3. (a) Simulated currents of the rectifying PMOS (solid) and NMOS (dashed) in conventional and proposed rectifiers, and (b) charges per RF cycle for 1.6 V output DC voltage.

the experimental results are presented in Section III, and finally the conclusion is drawn in Section IV.

II. Self-Adaptive Rectifier

A schematic of the proposed adaptive rectifier is shown in Fig. 2. Its operation principle is based on limiting the conduction of the rectifying devices at high input power range at which the reverse leakage becomes severe. This is achieved by raising the DC bias of the rectifying transistors (MP1, 2) gates as the input RF power increases. The proposed rectifier is comprised of four driving MOSFETs (MP1, 2 and MN1, 2) as rectifying devices that are connected in a fully, cross-coupled manner to enhance the rectifier sensitivity. However, unlike the conventional cross-coupled rectifier shown in Fig. 1, the DC voltage of the gates of the MP1, 2 are decoupled from their corresponding NMOS gates, while the AC voltages of the PMOS gates are coupled to the corresponding AC voltage of NMOS gates via two pumping capacitors CP3, 4.

To control the conduction of the rectifying devices, self DC biasing is dynamically applied to the PMOS gates only in the presence of high input RF power. While this self-biasing can be implemented in various ways, a simple yet dynamic approach is adopted by using two feedback transistors MN5, 6, as shown in Fig. 2. Here, MN5, 6 are controlled by a "Sense" signal which is derived from the output DC voltage (VDD) using a potential divider of a diode-connected transistor MN3 and a linear transistor MN4.

In the presence of high input RF power, the output DC voltage and the corresponding "Sense" signal will have high voltage levels. This high "Sense" signal switches on the biasing transistors (MN5, 6); hence, applying dynamic biasing to the gates of the PMOS rectifying devices to limit their reverse leakage, as shown in Fig. 3(a). Although the DC bias applied to the PMOS gate limits both its forward and reverse conductivity, it does not increase its conduction loss as it holds low voltage drop by operating in linear region while passing lower current than the conventional rectifier, as shown in Fig. 3(a). The rectifying PMOS and NMOS currents and alternating charges required to produce 1.6 V output DC voltage from the proposed and conventional rectifiers are plotted in Fig. 3(a) and (b), respectively. As expected, both rectifiers require the same net charges, ΔQ_f, to produce the same output voltage for equal loading. However, the magnitude of alternating charges flowing back and forth is much larger ($5\times$) in the case of the conventional rectifier compared to the proposed rectifier, demanding higher RF power for the same output voltage. Although the adaptive bias circuit is applied to the PMOS transistors, reverse leakage for NMOS is also reduced due to the reduced effective bias leading to a $3\times$ charge saving, as shown in Fig. 3(b).

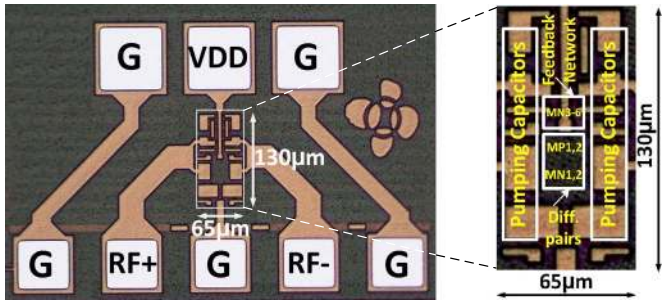

Fig. 4. (a) Microphotograph of the realized adaptive rectifier on CMOS 0.18 μm with test pads and (b) an enlarged view of the active area.

On the other hand, at low RF power, the sampled "Sense" signal is low and MN5, 6 are off. At the same time, the RF voltage is still applied differentially to the gate-source terminals of the four rectifying devices as in the conventional, cross-coupled rectifier [2]. This preserves the main sensitivity advantage of the cross-coupled scheme to the low input RF power levels. Moreover, the proposed implementation has minimal loading effects. The sensing branch (MN3, 4) is designed such that it has low quiescent current ($\sim$1.3 μA at $V_o = 1.2$ V $R_L = 100$ kΩ) by increasing the length of the diode-connected MN3 and the linear-resistive MN4, while it is OFF at $V_o < V_{\rm th}$. Also, the biasing branches (MN5, 6) have no static power consumption as they are connected to gates of MOS devices (MP1, 2) and to the decoupling capacitors

III. Experimental Results

The proposed rectifier is implemented in a 0.18 μm CMOS process technology and occupies 65 $\times$ 130 μm active area including the two additional capacitors and transistors. A microphotograph of the module including the testing pads is shown in Fig. 4. First, the input reflection coefficient is measured using Agilent's vector network analyzer (N5225A) at different input RF power levels. Then, the input RF power (Pin) is deduced from the RF source power level after the reflection and transmission losses are de-embedded. The RF measurements are carried out using a 1 GHz sinusoidal signal fed to a single-stage adaptive rectifier loaded by a 100 kΩ. All tests are repeated for a single-stage, conventional, FX rectifier fabricated on the same die using the same test setup for comparison purposes.

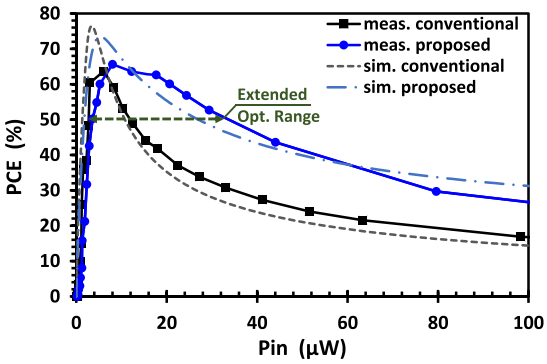

Fig. 5. Simulated (dashed) and measured (solid) power conversion efficiency versus RF input power for the proposed and conventional rectifiers.

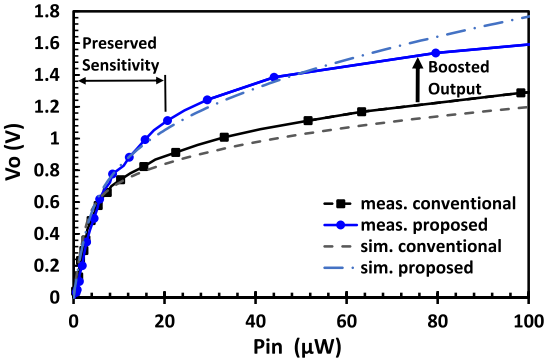

Fig. 6. Simulated (dashed) and measured (solid) output DC voltage of the proposed and conventional rectifiers versus RF input power.

The measured RF-to-DC power conversion efficiency is in well agreement with the simulation results for the proposed adaptive rectifier and the conventional FX rectifier as shown in Fig. 5. The adaptive rectifier is verified to maintain a high PCE over an extended input range of RF power (more than $2\times$ compared to the conventional FX rectifier), as shown in Fig. 5. This enables the proposed adaptive rectifier to operate at both low RF power level (i.e., long wireless power range) with superior sensitivity and also at high RF power level with extended efficiency. The measured output DC voltage of the proposed adaptive rectifier and the conventional FX rectifier are shown in Fig. 6. At the same input RF power level, the adaptive rectifier achieves a boosted output DC voltage which is 25% higher than that of the conventional rectifier under the same loading conditions. Furthermore, voltage boosting ranges from 24.5% to 29% is measured over varying load from 50 k to 500 kΩ. While the proposed rectifier achieves extended optimal range, it still maintains a high peak efficiency of 65% and sensitivity of -18 dBm for 1 V output over 100 kΩ.

A performance comparison of the adaptive rectifier with prior art is presented in Table I. The optimal range is defined as the input power range over which the rectifier maintains power conversion efficiency higher than 90% of its peak efficiency. The proposed architecture achieves a much wider optimal range compared to previously reported architectures; including the most common, fully cross-coupled rectifier [2] with 5 dB better sensitivity. More than $2\times$ improvement is achieved compared to the enhanced, 36-stage voltage doubler with floating gate devices [3]. Also, the proposed architecture provides a wide optimal range without sacrificing neither the PCE as [4] nor sensitivity as [2], [3]. Although, the reconfigurable 4-stage rectifier [10] shows comparable optimal range, it requires multi-stage re-configuration and is measured over a tracking load (regulator with external reference). It is worth mentioning that the proposed single-stage architecture can be combined with this tracking load and multi-stage techniques in [9], [10] to build a wider range, multi-stage rectifier.

TABLE I
PERFORMANCE COMPARISON

Ref	Process	Configuration	Sensitivity	Peak PCE	Opt. Range[a] P_{max}/P_{min}
This Work	$0.18\mu m$	1-stage, Proposed Adaptive[b]	-18 dBm[c] @Vo=1V	65%[c]	4.6x[c]
This Work	$0.18\mu m$	1-stage, Standard cross-coupled	-14.8 dBm[c] @Vo=1V	63%[c]	2.7x[c]
[2]	$0.18\mu m$	1-stage, Standard cross-coupled	-12.8 dBm[c] @Vo=1V	82.6%[c]	2.7x[c]
[3]	$0.25\mu m$	36-stage, floating gate doubler	-14.6dBm[d] @Vo=1V	60.7%[d]	2x[d]
[4]	$90\,nm$	5-stage, Standard cross-coupled	-20 dBm[d] @Vo=1V	40%[d]	2.4x[d]
[5]	$0.13\mu m$	12-stage,Adaptive V_{th} compensated	-17dBm[f] @Vo=1V	32%[f]	2.9x[f]
[10]	$0.13\mu m$	4-stage, Re-configurable	-21dBm[e] @Vo=2V	60%[e]	4.4x[e]

[a]Input power range of PCE$\geqslant$0.9 Peak PCE, [b]Intra-stage, [c]@100 kΩ, [d]@ 330 kΩ, [f]@ 500 kΩ, [e]@ tracking load (regulator with external ref. [10])

IV. CONCLUSION

In this letter, we propose a self-adaptive, differential, cross-coupled rectifier with an extended input RF power range without trading off the sensitivity (Pin $= -18$ dBm at Vo $= 1$ V) or the peak power conversion efficiency (peak PCE $= 65\%$). The architecture of the proposed rectifier was presented, and its performance was verified and compared with the conventional, fully cross-coupled rectifier.

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