# Wideband Balun-LNA With Simultaneous Output Balancing, Noise-Canceling and Distortion-Canceling

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*Abstract*—An inductorless low-noise amplifier (LNA) with active balun is proposed for multi-standard radio applications between 100 MHz and 6 GHz. It exploits a combination of a common-gate (CG) stage and an admittance-scaled common-source (CS) stage with replica biasing to maximize balanced operation, while simultaneously canceling the noise and distortion of the CG-stage. In this way, a noise figure (NF) close to or below 3 dB can be achieved, while good linearity is possible when the CS-stage is carefully optimized. We show that a CS-stage with deep submicron transistors can have high IIP2, because the $v_{gs} \cdot v_{ds}$ cross-term in a two-dimensional Taylor approximation of the $I_{DS}(V_{GS}, V_{DS})$ characteristic can cancel the traditionally dominant square-law term in the $I_{DS}(V_{GS})$ relation at practical gain values. Using standard 65 nm transistors at 1.2 V supply voltage, we realize a balun-LNA with 15 dB gain, NF < 3.5 dB and IIP2 > +20 dBm, while simultaneously achieving an IIP3 > 0 dBm. The best performance of the balun is achieved between 300 MHz to 3.5 GHz with gain and phase errors below 0.3 dB and ±2 degrees. The total power consumption is 21 mW, while the active area is only 0.01 mm².

*Index Terms*—CMOS integrated circuits, distortion canceling, linearity, low noise, low-noise amplifiers (LNAs), low-power electronics, noise canceling, noise cancellation, wideband LNA, wideband matching.

## I. INTRODUCTION

UPCOMING software-defined and multi-standard radio architectures may cover all major communication bands in use today up to 6 GHz [1]. This puts interesting demands on the radio and its low-noise amplifier (LNA). The wanted frequency span can be chopped into smaller bands which then can be processed by several dedicated, possibly tuned, LNA circuits. The other extreme is a single LNA, which then obviously needs to have wide bandwidth. In contrast to a multi-LNA solution, the single wideband LNA is flexible and efficient in terms of area, power and costs. Single-ended input LNAs are preferred to save I/O pins and because antennas and RF filters usually produce single ended signals. On the other hand, differential signaling in the receive chain is preferred in order to reduce second-order distortion and to reject power supply and substrate noise. Thus, at some point in the receive chain a balun is needed to convert the single-ended RF signal into a differential signal. Off-chip
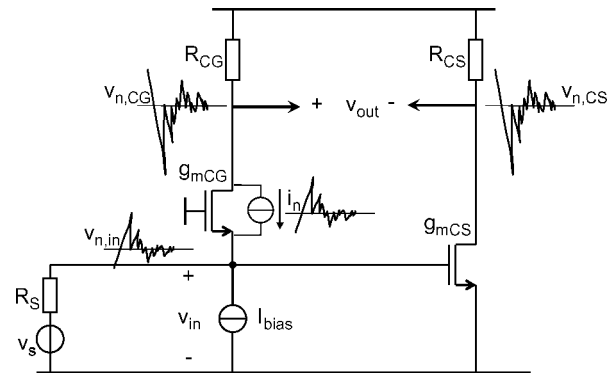
Fig. 1. The basic common-gate–common-source topology in which the noise of the CG-transistor can be canceled.

baluns with low losses are typically narrowband so that several baluns would be required in case of wideband operation. On the other hand, wideband passive baluns typically have high loss, degrading the overall NF of a receiver significantly.

Combining the balun and LNA functionality into a single integrated circuit seems an attractive option to realize a wideband low-noise receiver front-end. However, only a few CMOS wideband LNA-balun combinations with sufficient low noise figure for multiband receivers (3–4 dB) have been published [1]–[3]. These circuits all exploit the noise canceling topology published in [4, Fig. 4b], shown in Fig. 1. This is one of the noise canceling topologies discussed in [5]. Although these circuits have a single-ended input and differential output, the (im)balance of the output signal is not reported. We will show that this imbalance can be significant, e.g., about 6 dB in [1, Fig. 8a]. Next to this, the circuits in [1]–[3] all use integrated inductors. As in newer CMOS technologies the area-costs increase, area-consuming integrated inductors become increasingly expensive. Finally, we prefer to use baseline transistors at the standard supply voltage of 1.2 V instead of thick oxide transistors at 1.8 V [2] or 2.5 V supply [1]. This is challenging with respect to achieving sufficient gain and good linearity.

In this paper, we present an inductorless balun-LNA with a well-balanced output signal, and will show that it can achieve wideband amplification at low noise in a baseline 65 nm CMOS process with standard 1.2 V supply voltage, while also achieving good linearity. The measurements on this circuit were published in [6]. This paper gives an in-depth analysis of the design options, the noise behavior and distortion behavior of the used circuit topology. Furthermore, to the authors' knowledge, this is the first paper in which it is recognized that cross-terms in the $I_{DS}(V_{GS}, V_{DS})$ characteristic of modern submicron CMOS
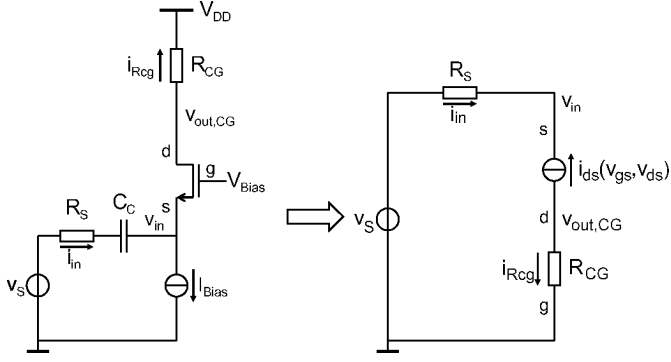
Fig. 2. Small signal equivalent of a CG-stage.

transistors can be exploited to obtain an amplifying stage with low second-order distortion.

The balun-LNA circuit topology is depicted in Fig. 1. This common-gate (CG) stage in parallel to a common-source (CS) stage is a well-known structure. Actually, there are at least 15 to 20 year old references [7], [8, Figs. 2 and 3], and possibly even older ones. Later, this structure has been used in the "micro-mixer" circuit [9] and the LNA in [1]. However, all these circuits use CG and CS devices with *identical* size and bias. As will be shown in Sections II and III, *identical devices cannot simultaneously bring the benefits of output balancing, noise canceling and distortion canceling*. This paper provides insight in circuit dimensioning trade-offs and reveals new ways to exploit the circuit to maximize performance. To this end, Section II derives conditions for simultaneous output balancing, noise canceling and distortion canceling. Section III details the noise analysis and motivates why appropriate scaling of the CS-stage is needed to exploit noise canceling most effectively and obtain a noise figure in the order of 3 dB or lower. Apart from noise, the circuit also simultaneously renders distortion canceling of the (CG-) matching-device nonlinearity [4]. However, to benefit from this, the CS-stage needs to have low distortion too. Therefore, we analyze distortion in detail in Section IV, focusing on short channel devices. The distortion generated by these devices is not only due to nonlinearity of their transconductance ($g_m$) and of their output conductance ($g_{ds}$), but also due to the dependence of $g_m$ on the drain-source bias voltage. We will show that a (cross-) term describing this dependence can be used to cancel the dominant second-order distortion due to $g_m$. Together with the distortion canceling of the CG-stage this results in a high overall IIP2. In Section V we describe the actual balun-LNA circuit design, to validate theory and set an expectation for the measurements. Section VI presents measurements and benchmarks the LNA to previous designs, while Section VII presents a summary and conclusions.

## II. SIMULTANEOUS BALANCING AND NOISE/DISTORTION CANCELING

In the sections below we will briefly derive the conditions for simultaneous balancing, noise canceling and distortion canceling. We will neglect capacitive effects for simplicity, and verify the validity of this assumption later via measurements.

A more detailed discussion on high frequency limitations and robustness for component variations can be found in [5].

### A. Balancing (Balun Operation)

The common-gate stage in Fig. 2, biased with a current source, has a straightforward relation between its voltage gain ($A_{v,CG}$) and its input impedance ($R_{in,CG}$). The signal current ($i_{Rcg}$) flowing through the load resistor $R_{CG}$ has to be equal to the signal current flowing at the input ($i_{in}$), as there is no alternative path to ground. Thus,

$$i_{in} = i_{Rcg} = \frac{v_{out,CG}}{R_{CG}} = \frac{v_{in} \cdot A_{v,CG}}{R_{CG}}. \quad (1)$$

As a result, the input impedance of the CG-stage can be expressed as

$$R_{in,CG} = \frac{v_{in}}{i_{in}} = \frac{R_{CG}}{A_{v,CG}}. \quad (2)$$

For an ideal transistor, having infinite output resistance, this is obvious. In that case the input impedance can be written as $R_{in,CG} = 1/g_m$ and the gain equals $A_{v,CG} = g_m \cdot R_{CG}$. However, (1) and (2) are equally valid when the finite output resistance and the body-effect of a real transistor are taken into account.

For an impedance match at the input, the input impedance of the CG-stage ($R_{in,CG}$) should equal the source resistance ($R_S$), thus the gain of the CG stage becomes

$$A_{v,CG} = \frac{R_{CG}}{R_{in,CG}} = \frac{R_{CG}}{R_S}. \quad (3)$$

To create a balun, the gain of the CS-stage in Fig. 1 should be equal, but have opposite sign, thus,

$$A_{v,CS} = -A_{v,CG} = -\frac{R_{CG}}{R_S}. \quad (4)$$

### B. Noise Canceling

The noise generated by the CG-transistor in Fig. 1 can be represented by a current source ($i_n$). This current generates both a voltage at the input-node ($v_{n,in} = \alpha_1 \cdot i_n \cdot R_S$) and a fully correlated anti-phase voltage at the CG-output ($v_{n,CG} = -\alpha_1 \cdot i_n \cdot R_{CG}$). The factor $\alpha_1$ equals the voltage division between the input resistance ($R_{in,CG}$) and the source resistance ($R_S$), which equals 1/2 in case of impedance matching:

$$\alpha_1 = \frac{R_{in,CG}}{R_{in,CG} + R_S}. \quad (5)$$

The noise at the CS-output equals the CG-output noise ($v_{n,CS} = v_{n,in} \cdot A_{v,CS} = v_{n,CG}$), when the CS-gain $A_{v,CS}$ satisfies (4). Thus, the noise contribution of the CG-transistor can be canceled, as it becomes a purely common-mode signal at the differential output ($v_{out}$). This proofs that simultaneously balancing of the output signal and noise canceling is obtained.

### C. Distortion Canceling

As derived in [4], not only the noise of the impedance matching device is canceled, but also its nonlinearity, assuming

it can be modeled as a current source between drain and source, controlled by the *gate-source* voltage. We will take this one step further here, by also taking into account the influence of the *drain-source* voltage on the drain current. This allows the modeling of the nonlinear output conductance and other second-order effects like Drain Induced Barrier Lowering (DIBL), which become more prominent in modern CMOS processes.

Fig. 2 shows a model of the CG-stage. Weakly nonlinear behavior is assumed, modeled by a drain-source current $i_{ds}$ which depends nonlinearly on both voltage variations $v_{gs}$ and $v_{ds}$ around their DC bias points.[1] The source signal $(v_s)$ causes a nonlinear drain-source current $(i_{ds})$ which is converted into a nonlinear voltage at the input $(v_{in})$ via the (linear) source resistor $R_S$. The nonlinear input voltage $(v_{in})$ can be written as a Taylor expansion of the signal source voltage $(v_s)$:

$$v_{in} = \alpha_1 \cdot v_s + \alpha_2 \cdot v_s^2 + \alpha_3 \cdot v_s^3 + \alpha_4 \cdot v_s^4 + \ldots = \alpha_1 \cdot v_s + v_{NL} \quad (6)$$

where the $\alpha$'s represent Taylor coefficients and $v_{NL}$ contains all unwanted nonlinear terms and the first Taylor coefficient $(\alpha_1)$ is defined in (5).

The output voltage of the CG-stage (see Fig. 2) can be written as

$$v_{out,CG} = i_{in} \cdot R_{CG} = \frac{v_s - v_{in}}{R_S} \cdot R_{CG}$$
$$= ((1 - \alpha_1) \cdot v_s - v_{NL}) \frac{R_{CG}}{R_S} \quad (7)$$

where (6) is used. The output voltage of the CS-stage can be written using (4) as

$$v_{out,CS} = -v_{in} \frac{R_{CG}}{R_S} = -(\alpha_1 \cdot v_s + v_{NL}) \frac{R_{CG}}{R_S}. \quad (8)$$

The difference in sign of the wanted signal $v_s$ and unwanted signal $v_{NL}$ in (7) and (8) can be exploited: after subtraction only the linear signal remains

$$v_{out,diff} = v_{out,CG} - v_{out,CS} = v_s \cdot \frac{R_{CG}}{R_S}. \quad (9)$$

In conclusion, all noise and distortion currents generated by the CG-transistor can be canceled, irrespective whether produced due to nonlinearity of the transconductance or nonlinearity of the output conductance. The gain required in the CS-stage to cancel the distortion products of the CG-transistor equals the gain required to obtain output balancing, leading to the conclusion that *simultaneous balancing and cancellation of unwanted noise and distortion currents of the CG transistor is possible*. As the distortion due to the CG-transistor is canceled, while $R_{CG}$ is normally quite linear, the CS-stage will determine the overall linearity of the complete LNA. The linearity of the CS-stage will be analyzed in Section IV-B. The final noise is determined by $R_{CG}$ together with the CS-stage, as will be shown in the next section.

## III. NOISE ANALYSIS

In this section, we analyze the noise figure of the basic CG-CS LNA (Fig. 1) for three different design options. To simplify

the calculation, transistors are assumed to have infinite output impedance and the bias current source of the CG-transistor is assumed to be ideal. Furthermore only the thermal noise of the resistors and of the transistors $(\overline{i_n^2}/\Delta f = 4kT\gamma g_m)$ is taken into account assuming $\gamma = 2/3$, which is known to be optimistic for short channel devices. These assumptions will overestimate the gain and underestimate the NF. However, the calculation is useful to compare the different design options and simplifies comparison to previously published results using similar assumptions. The output noise power of the circuit elements in Fig. 1 can be calculated, and divided by the noise contribution of the signal source, leading to the noise factor:

$$F = 1 + \frac{\gamma \cdot g_{mCG} \cdot (R_{CG} - R_S \cdot g_{mCS} \cdot R_{CS})^2}{R_S \cdot A_V^2}$$
$$+ \frac{\gamma \cdot g_{mCS} \cdot R_{CS}^2 \cdot (1 + g_{mCG} \cdot R_S)^2}{R_S \cdot A_V^2}$$
$$+ \frac{(R_{CG} + R_{CS}) \cdot (1 + g_{mCG} \cdot R_S)^2}{R_S \cdot A_V^2} \quad (10)$$

where the second part is the contribution from the CG-transistor, the third part from the CS-transistor and the last part from the load resistors, while the voltage gain $(A_V)$ equals

$$A_V = g_{mCG} \cdot R_{CG} + g_{mCS} \cdot R_{CS}. \quad (11)$$

Three different design options of the CG-CS circuit are now considered, as follows.

1) The transconductances of the CS and CG transistors are *equal* and the load resistors are *equal*, thus: $g_{mCS} = g_{mCG}$ and $R_{CS} = R_{CG}$ (the traditional way to implement an active balun [7], [8], using a CG-CS amplifier).
2) The transconductance of the CS transistor is $n$ times bigger than the CG-transconductance and the load resistors are equal, thus: $g_{mCS} = n \cdot g_{mCG}$ and $R_{CS} = R_{CG}$ (design option used in [1]).
3) The CS-transconductance is $n$ times bigger than the CG-transconductance and the CS-resistor is $n$ times smaller than the CG-resistor, thus: $g_{mCS} = n \cdot g_{mCG}$ and $R_{CS} = R_{CG}/n$ (characterizes the design presented in this paper).

The ratio of the voltage gain of the CS- and the CG-stage is defined as the gain imbalance:

$$\Delta A_V = 20 \cdot \log \left( \frac{A_{V,CS}}{A_{V,CG}} \right) = 20 \cdot \log \left( \frac{g_{mCS} \cdot R_{CS}}{g_{mCG} \cdot R_{CG}} \right). \quad (12)$$

The noise figure, voltage gain $(A_V)$ and gain imbalance $(\Delta A_V)$ of the three design options are plotted versus the impedance scaling factor $n$ in Fig. 3. In all three cases the CG-transconductance is assumed to be: $g_{mCG} = 1/R_S$, to have input impedance matching and $R_{CG} = 4 \cdot R_S$ to have a reasonable gain of the CG-stage.

Option 1) gives horizontal lines, as it does not depend on the factor $n$. The NF equals 3.4 dB, the voltage gain 18.1 dB ($8\times$) and the output signal is perfectly balanced $(\Delta A_V = 0$ dB). Although the noise of the CG-transistor is fully canceled, this effect is not exploited to achieve a NF below 3 dB. The noise generated by the CS-stage is significant because of its low
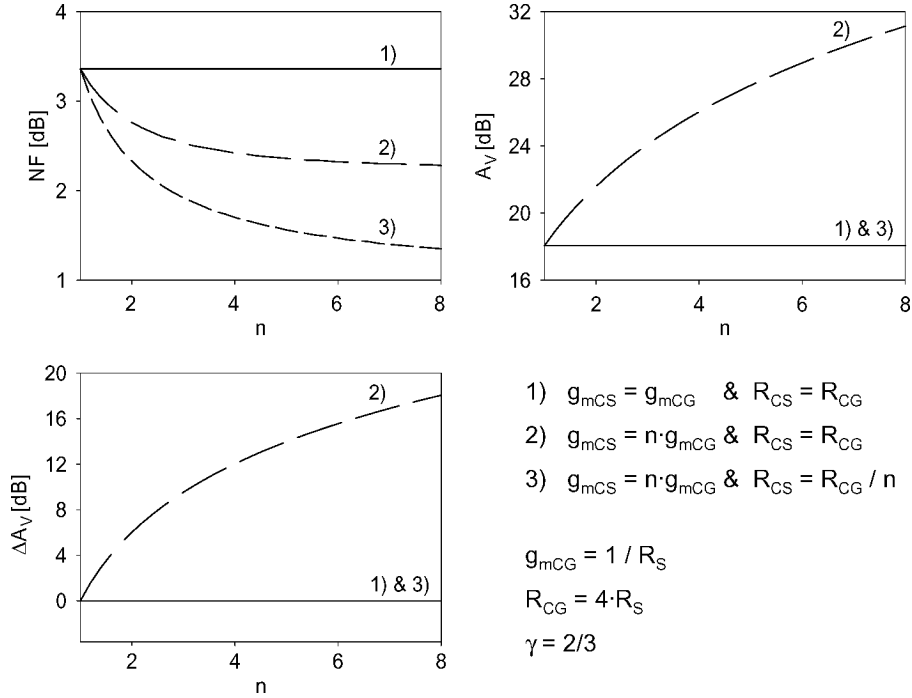
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[1]Also the body-effect can be accounted for, by observing that $v_{sb} = -v_{gs}$ for a CG-transistor with its bulk node $(b)$ connected to ground.

Fig. 3. Noise figure (NF), voltage gain ($A_V$) and gain imbalance ($\Delta A_V$) versus impedance scaling factor '$n$' for three different cases.

transconductance ($g_{mCS} = 1/R_S$) and the voltage division of 1/2 by $R_S$ and $R_{in}$ magnifies its contribution.

Option 2) shows a decreasing NF and an increase in voltage-gain with increasing $n$. These two positive effects are however countered by an increase in gain imbalance. As $n$ increases, the voltage gain of the CS-stage gain increases whereas the CG-voltage gain remains constant.

The last option, 3), shows an even faster decrease of NF than in option 2). In contrast to option 2), the noise of the CG-transistor is fully canceled. Next to this, the contribution of the CS-transistor decreases with a factor $1/n$ for increasing $n$, whereas in option 2) this contribution decreases at a rate slower than $1/n$. The voltage gain remains constant for option 3). Both the transconductance and the resistance of the CS-stage are scaled simultaneously (admittance scaling [10]). Thus the gain of the CS-stage remains constant and no gain imbalance occurs, i.e., the balun functionality is maintained for all values of $n$.

Now some more attention is given to design option 2) as published in [1]. Both in the calculation above and in [1] the load resistors have a value of $4 \cdot R_S$ ($= 200\ \Omega$). The transconductance-scaling factor in [1] is estimated to be in the range n = 2–3, using the square-law MOS-model ($g_m = \sqrt{2 \cdot \mu_n \cdot C_{ox} \cdot W/L \cdot I_D}$). This translates into a gain imbalance between CG- and CS-stage of 6–9.5 dB and (10) gives a NF between 2.8 and 2.5 dB. The remarkably low NF reported in [1, Figure 8b] of about 2.2 dB is a simulation result where $\gamma = 1/2$ is assumed (instead of $\gamma = 2/3$, or higher) [11]. In the abstract of [1] a much higher NF of 3–3.5 dB is given.

Overall, we conclude that admittance scaling of the CS-stage (option 3) is the best way to achieve low noise figure in the order of 3 dB or below, while simultaneously achieving good output balancing. It is possible to get more gain using option 2

[1], but this comes at the cost of suboptimal noise behavior and significant unbalance in the output signal.

## IV. LINEARITY ANALYSIS

In this section we will analyze the nonlinearity of the balun-LNA proposed in the previous section and see how we can exploit the distortion cancellation property. However, before we do so, we first want to introduce the IIP2 problem of wideband LNAs.

### A. Linearity Requirements for Wideband Receivers

Like a narrowband zero-IF or near zero-IF receiver, a wideband receiver is sensitive to the second-order intermodulation product generated by an AM modulated carrier via AM detection. However, a wideband receiver may also suffer from second-order intermodulation generated by interferers that have a sum or difference frequency equal to the wanted RF-input signal. The response to a modulated carrier can be suppressed by placing a high-pass filter (i.e., AC-coupling) between the LNA-output and mixer-input and by driving and designing the mixer in a well-balanced way [12]. However, the intermodulation product generated at a frequency equal to the frequency of the wanted signal cannot be separated from the signal. Especially standards that operate on large bandwidths, like DVB-H (470–862 MHz) [13] or WiMedia UWB (3.1–10.6 GHz) [14], have a high probability that a certain combination of interferers renders an in-band intermodulation product. A receiver designed for these standards should have an LNA with sufficiently high IIP2 (and IIP3) in order to handle strong interferers like WLAN (IEEE 802.11a/b/g) and the GSM standards. The required intercept points depend strongly on the assumed interferer scenario and the assumed

amount of pre-filtering of the interfering signals. For a Wi-Media UWB receiver the required IIP2 is above $+20$ dBm and IIP3 above $-9$ dBm as derived in [15, sec. II]. For a DVB-H receiver, consider a GSM interferer (1.8 GHz, $+30$ dBm at 0.2 m distance) and a WLAN interferer (2.4 GHz, $+20$ dBm at 1 m) that generate second-order intermodulation product in the DVB-H band at 600 MHz. The received interferer power levels will be $+7$ dBm (GSM) and $-20$ dBm (WLAN). For a decrease in sensitivity of 3 dB, the maximum allowable interference level in a DVB-H receiver is $-105$ dBm [13]. Without filtering the required IIP2 would become $\text{IIP2} = P_{int1} + P_{int2} - P_{IM,max} = 7 - 20 + 105 = +92 \text{ dBm}(!)$. Assuming that both (out-of-band) interferers can be filtered with 35 dB attenuation brings the required IIP2 back to a more realistic value of $+22$ dBm.

### B. Distortion of the CS-Stage

As the distortion of the CG-stage can be canceled in the parallel CG- and CS-stage amplifier (Section II-C), the distortion performance of the total amplifier is determined by the distortion behavior of the CS stage. For distortion calculations often only the nonlinearity of the transconductance of a transistor is taken into account. However, as in [16], [17], we find that the nonlinearity of the output conductance cannot be neglected anymore in modern CMOS processes. The drain current ($i_{ds}$) as function of the gate-source voltage ($v_{gs}$) and the drain-source voltage ($v_{ds}$) can be written as a two-dimensional Taylor approximation:

$$
\begin{aligned}
i_{ds}(v_{gs}, v_{ds}) = {} & g_{m1}v_{gs} + g_{ds1}v_{ds} + g_{m2}v_{gs}^2 + g_{ds2}v_{ds}^2 \\
& + x_{11}v_{gs}v_{ds} + g_{m3}v_{gs}^3 + g_{ds3}v_{ds}^3 \\
& + x_{12}v_{gs}v_{ds}^2 + x_{21}v_{gs}^2 v_{ds} + \dots
\end{aligned}
\tag{13}
$$

where the Taylor coefficients can be derived from the large signal relations between $I_{DS}$, $V_{GS}$ and $V_{DS}$:

$$
g_{mk} = \frac{1}{k!}\frac{\partial^k I_{DS}}{\partial V_{GS}^k}; \quad g_{dsk} = \frac{1}{k!}\frac{\partial^k I_{DS}}{\partial V_{DS}^k}; \quad x_{pq} = \frac{1}{p!q!}\frac{\partial^{p+q} I_{DS}}{\partial V_{GS}^p \partial V_{DS}^q}.
\tag{14}
$$

Notice that in (13) $i_{ds}$ not only depends on powers of $v_{gs}$ and $v_{ds}$ but also on cross-terms ($x_{11}$, $x_{12}$, etc.) of $v_{gs}$ and $v_{ds}$. The cross-term $x_{11}$ can be described as the dependence of the transconductance ($g_{m1}$) on the drain-source bias voltage. One of the reasons for this dependence is the drain induced barrier lowering (DIBL) effect. The terms $x_{12}$, $x_{21}$, etc. are higher order derivatives of $x_{11}$. The cross-terms will prove to be very important for the linearity in modern short-channel CMOS processes. In [18] the importance of these cross-terms was shown for MESFET transistors, which have linearity characteristics that are somewhat similar to MOSFETs. The linearity of a resistively loaded CS-transistor ($g_{mCS}$ and $R_{CS}$ in Fig. 1) is calculated. The variation of the drain source voltage ($v_{ds}$) is set by the output current of the transistor ($i_{ds}$) and the load resistor $R_{CS}$. Using this and (13) $v_{ds}$ can be expressed in a Taylor approximation of $v_{gs}$:

$$
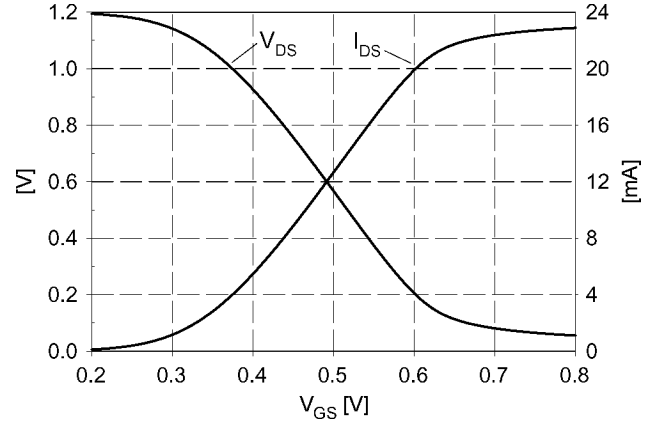v_{ds} = c_1 v_{gs} + c_2 v_{gs}^2 + c_3 v_{gs}^3 + \dots
\tag{15}
$$



Fig. 4. $V_{DS}$ and $I_{DS}$ versus $V_{GS}$ of a resistively loaded CS-stage.

with the following Taylor coefficients:

$$
\begin{aligned}
c_1 = {} & - g_{m1} \cdot (R_{CS} // (1/g_{ds1})) \\
c_2 = {} & - \left(g_{m2} + g_{ds2}c_1^2 + x_{11}c_1\right) \cdot (R_{CS} // (1/g_{ds1})) \\
c_3 = {} & - \left(g_{m3} + g_{ds3}c_1^3 + 2g_{ds2}c_1 c_2 + x_{11}c_2 + x_{12}c_1^2 + x_{21}c_1\right) \\
& \cdot (R_{CS} // (1/g_{ds1})).
\end{aligned}
\tag{16}
$$

To demonstrate the importance of the coefficients in (16), they have been derived from simulations. The circuit parameters of the simulated CS-stage are: $\text{W/L} = 300 \ \mu\text{m}/0.06 \ \mu\text{m}$ and $\text{R}_{CS} = 50 \ \Omega$. MOS model 11 [19], known for its accurate linearity modeling, is used for the transistor model. Fig. 4 shows the drain-source current ($I_{DS}$) and the drain-source voltage ($V_{DS}$) versus the gate-source bias voltage ($V_{GS}$). In the inset of Fig. 5 the linear voltage gain ($c_1$) of the CS-stage versus $V_{GS}$ is plotted. The second-order coefficient $c_2$ is proportional to the derivative of $c_1$, thus it equals 0 at the maximum gain point ($c_1 = -4$ at $V_{GS} \approx 0.5$ V). The three contributions that sum up to $c_2$ in (16) are also shown in Fig. 5. In the lower range of $V_{GS}$, where the transistor is in saturation, the second-order distortion due to the cross-term ($x_{11}$) is in the same order (but with opposite sign) as the second-order coefficient generated by the transconductance nonlinearity ($g_{m2}$). These two terms cancel each other around the maximum in gain ($V_{GS} \approx 0.5$ V). The contribution due to the output conductance ($g_{ds2}$) in this $V_{GS}$ range is small. As $V_{GS}$ increases (and $V_{DS}$ decreases) the transistor goes into linear operation, which results in lower transconductance nonlinearity ($g_{m2}$). However, the output conductance nonlinearity ($g_{ds2}$) increases significantly above $V_{GS} = 0.5$ V due to the decreasing $V_{DS}$. The contribution due to the cross-term remains relatively constant over a broad range of $V_{GS}$ values.

Fig. 6 shows the IIP2 and IIP3 versus $V_{GS}$ of the resistively loaded CS-stage. These graphs were derived from the Taylor coefficients $c_1$, $c_2$ and $c_3$ using

$$
\text{IIP2}_{\text{dBm}} = 20 \cdot \log_{10}\left(\left|\frac{c_1}{c_2}\right|\right) + 10 \text{ dB}
$$

$$
\text{IIP3}_{\text{dBm}} = 20 \cdot \log_{10}\left(\sqrt{\left|\frac{4}{3}\frac{c_1}{c_3}\right|}\right) + 10 \text{ dB}
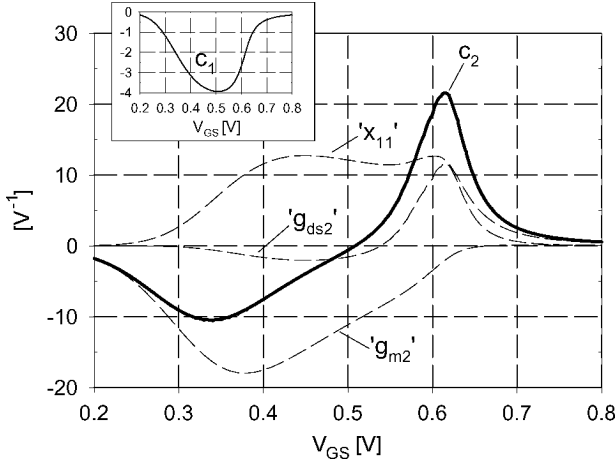\tag{17}
$$

Fig. 5. Simulated second-order nonlinearity coefficient $(c_2)$ and individual contributions due to the transistor coefficients $(g_{m2}, g_{ds2}$ and $x_{11})$. Inset: linear gain coefficient $(c_1)$ of the CS-stage.
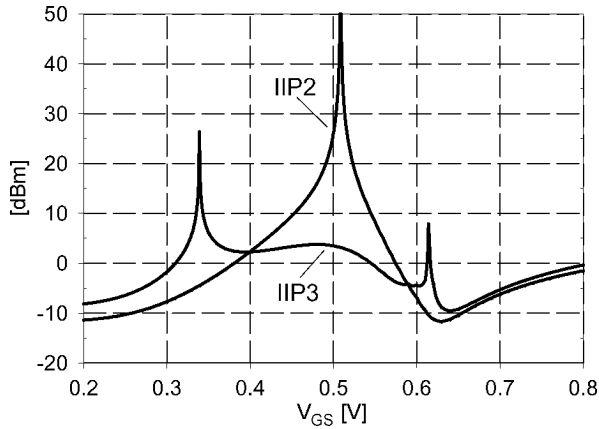


Fig. 7. Schematic of the wideband balun-LNA; the circuit within the dashed box is integrated on chip.



Fig. 6. Simulated IIP2 and IIP3 of a resistively loaded CS-stage.



Fig. 8. Die photo of the bonded wideband balun-LNA.

where the factor 10 dB accounts for the conversion from peak-voltage to power in dBm in 50 $\Omega$. This shows that the resistively loaded CS-stage is capable of achieving an IIP2 higher than +20 dBm with an IIP3 higher than +2 dBm when it is biased close to the point where it reaches a maximum in gain.

## V. CIRCUIT DESIGN

Fig. 7 shows the balun-LNA circuit, the circuit inside the dashed box is implemented on silicon. The voltage gains of the CG- and CS-paths are designed to be equal, giving the balun function. However, the CS-stage is scaled up n times by admittance scaling to achieve lower noise (see Section III). As a result the output impedance of the CG and CS-stage are not equal. To solve this, the outputs of both amplifier paths are buffered by identical source-followers, both having 50 $\Omega$ output impedance. These source-followers are currently also used as measurement buffers; in a complete receiver design they can drive a mixer, usually at a higher impedance level and reduced current. To maximize balanced operation, the DC-levels at the gates of the source followers are chosen equal. This is achieved by AC-coupling the output of the CS-stage to its source-follower and gen-
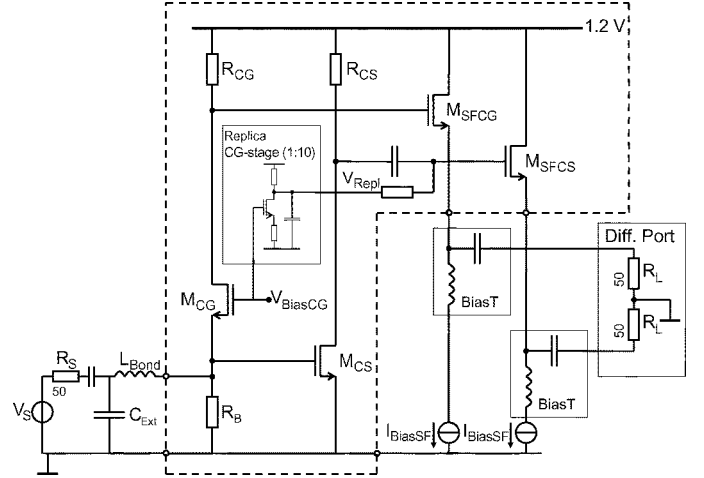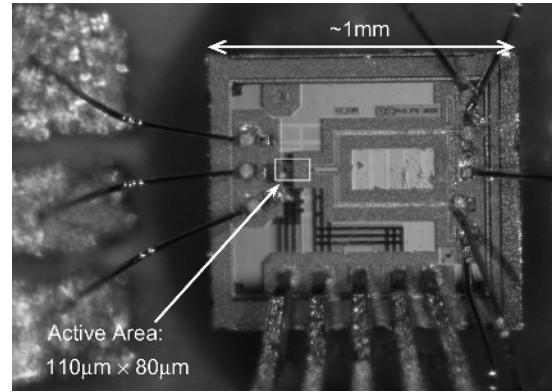
erating the DC-level $(V_{Repl})$ by a scaled replica of the CG-stage (see Fig. 7). The cut-off frequency of the AC-coupling is designed to be at 10 MHz. This is more than a decade below the intended minimum operation frequency, which keeps the error in phase difference of the two paths within a few degrees of 180°. The transconductance of $M_{CS}(g_{mCS})$ is chosen 5 times higher than $g_{mCG}$ to limit its noise contribution (see Section III). The resistor $R_B$ acts as a current source and is chosen 7 times higher than $R_S$, thereby limiting its noise contribution to about 0.3 dB.

## VI. MEASUREMENTS

The LNA, which has an active area of only 110 $\mu$m × 80 $\mu$m, has been fabricated in a baseline 65 nm CMOS process and is mounted on a PCB, see Fig. 8. For quick prototyping only the most critical connections for the RF performance, the inputs and outputs, are bonded. The supply and bias are applied using a probe. By using adequate on-chip decoupling, the effects due to inductance in the supply lines are suppressed.

### A. Gain, Input-Match and Isolation

Fig. 9 shows the measured single-ended input to differential output S-parameter gain, $S_{ds21}$. This parameter characterizes
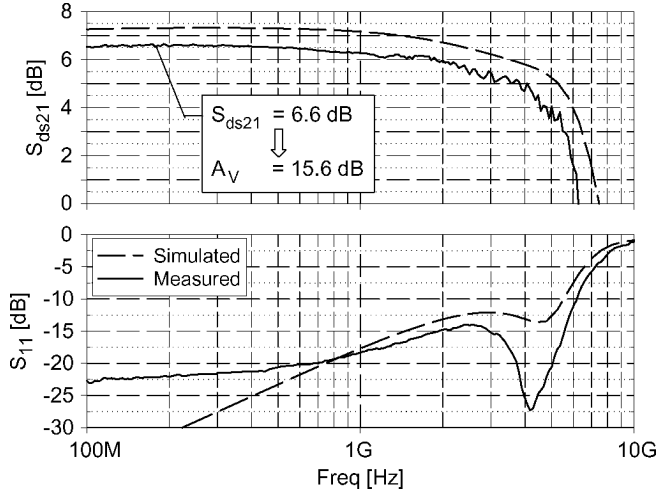
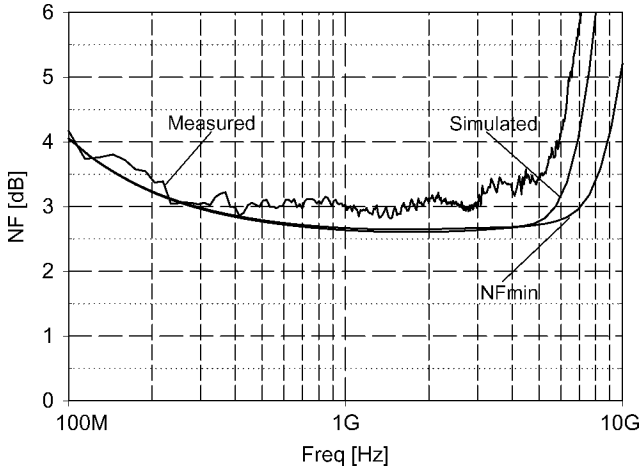Fig. 9. Simulated and measured S-parameters, $S_{ds21}$ (Gain: single-ended in, differential out) and $S_{11}$.



Fig. 10. Measured noise figure, simulated NF and $NF_{min}$ of the complete LNA.



Fig. 11. Gain imbalance, simulated and measured (20 samples).
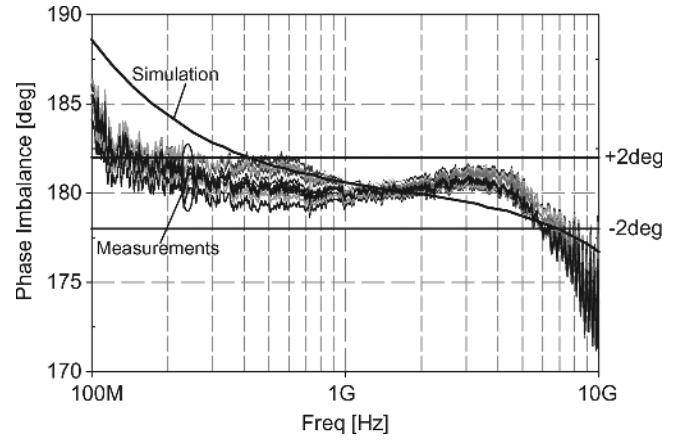


Fig. 12. Phase imbalance, simulated and measured (20 samples).

the gain of the LNA using a 50 $\Omega$ single-ended input port and a 100 $\Omega$ differential output port. In practical use, the LNA will usually be followed by an on-chip mixer with a voltage-type input, and matching to 50 $\Omega$ at the outputs is not needed. The most meaningful gain parameter is then the (unloaded) voltage gain. To convert $S_{ds21}$ into voltage gain, 6 dB needs to be added to account for the voltage-halving at the matched output, and an additional 3 dB to take the conversion from 50 $\Omega$ input to 100 $\Omega$ output into account. Thus, the voltage gain is within 15.1 dB $\pm$ 0.5 dB from 100 MHz up to 2.5 GHz. The 3 dB bandwidth is 5.2 GHz.

The $\pi$-network formed by an external capacitor (600 fF), the input bondwire inductance ($\sim$1 nH) and the input capacitance of the circuit gives a broad input match. Fig. 9 shows that $S_{11}$ is below $-10$ dB up to 6.2 GHz. The influence of the ground inductance is included in this measurement, as a Ground-Signal-Ground configuration has been used to bond the input.

The common and differential output to single-ended input isolations ($S_{sc12}$ and $S_{sd12}$, not shown) are better than $-30$ dB up to 10 GHz.
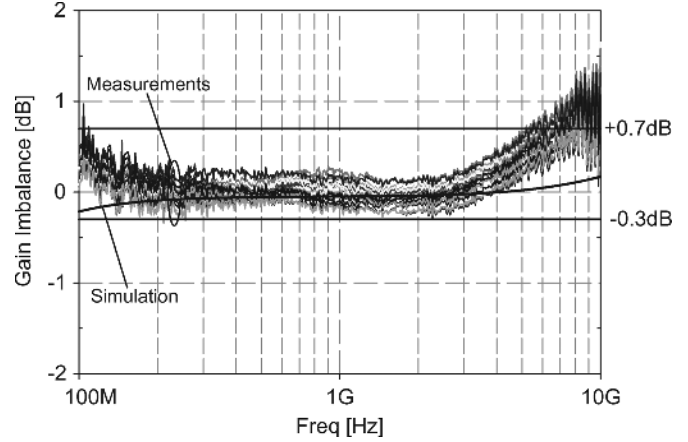
### B. Noise Figure

Fig. 10 shows that the measured noise figure (NF) is below 3.5 dB from 0.2 to 5.2 GHz and below 4 dB from 0.1 to 6 GHz. Another advantageous property of the noise canceling technique is that the power and noise matching can be obtained simultaneously [4]. Indeed, the simulated NF equals the simulated $NF_{min}$ of the complete LNA over a large bandwidth and only starts to deviate at higher frequencies due to the increasing impedance mismatch at the input. The increase of $NF_{min}$ at low frequencies is due to $1/f$ noise, and the increase at high frequencies is due to the drop in gain.

### C. Gain and Phase Imbalance

The balun performance was characterized on 20 samples at nominal bias conditions, equal to the simulation conditions. These measurements were performed using wafer-probing. The gain and phase imbalance measurements are shown in Fig. 11 and Fig. 12. The gain imbalance is within $+0.7$ to $-0.3$ dB from 100 MHz to 5.2 GHz and even within $\pm0.3$ dB in the band 180 MHz–3.5 GHz. The phase imbalance remains within $\pm2$ degrees from 250 MHz to 6 GHz. The somewhat larger spread in phase difference in the 300–800 MHz range is caused by a resonance-effect in the output cables and non-optimal

TABLE I
COMPARISON OF BALUN-LNAS, PASSIVE BALUNS AND INDUCTORLESS SINGLE-ENDED LNAS

| Ref | Freq. Band [GHz] | NF [dB] | Gain $A_V$ [dB] | IIP2 [dBm] | IIP3 [dBm] | Power (core) [mW] | Proc.[2] $V_{supply}$ | # coils area [mm$^2$] | Balun? | Gain imbal. [dB] | Phase imbal. [deg] |
|---|---|---|---|---|---|---|---|---|---|---|---|
| This Work | **0.2 – 5.2** | < 3.5 | 13 – 15.6 | **> +20** | > 0 | 21 (14) | 65nm 1.2V | – **0.009** | YES | < 0.7 < 0.3 [3] | **< 2** |
| [1] JSSC 2006 | 0.8 – 6 | < 3.5 | 18 – 20 | ? | >-3.5 | 12.5 | 90nm 2.5V | 2 ? | YES | > 6 [4] | ? |
| [2] CICC 2005 | 0.9 – 5 | < 3.5 | 18 – 19 | +4 (sim) | +1 (sim) | 12 | 0.13μm 1.8V | 4 ~0.4 | YES | ? | ? |
| [3] RFIC 2005 | 2.7 – 4.5 | < 5 | 18 – 19.6 | ? | -8 | 16.2 (12.6) | 90nm 1.2V | 1 0.2 | YES | ? | ? |
| [22] MTT-S 2005 | 0.8 – 2.5 | < 4 [1] | $S_{ds21}$ ≈ -4 | high | high | 0 passive balun | 0.18μm - | 2 0.073 | YES | < 0.4 | < 3.2 |
| [23] MTT-S 2005 | 1.5 – 3.5 | < 1 [1] | $S_{ds21}$ ≈ -1 | high | high | 0 passive balun | GaAs - | 6 0.42 | YES | < 1.3 | < 4 |
| [4] JSSC 2004 | 0.2 – 2.0 | < 2.4 | 10 – 14 | +12 | 0 | 35 | 0.25μm 2.5V | – 0.075 | NO | N/A | N/A |
| [24] ISSCC 2006 | 0.5 – 8.2 | < 2.6 | 22 – 25 | ? | -4 / -16 | 42 | 90nm 2.7V | – 0.025 | NO | N/A | N/A |

[1] Insertion Loss      [2] CMOS unless specified differently      [3] For 180 MHz ~ 3.5GHz      [4] Derived from component values in schematic
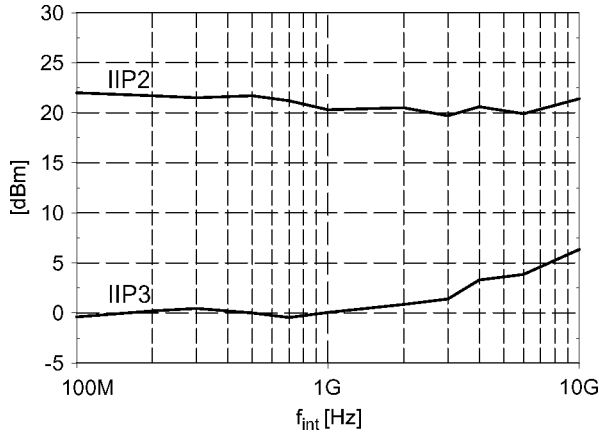


Fig. 13.   IIP2 and IIP3 versus intermodulation frequency ($f_{int}$).

probe contacting. If desired, fine tuning of the balun functionality is possible, e.g., via the bias of the CS or GS stage or via the bulk of the CG transistor.

### D. Linearity

Fig. 13 shows the second-order and third-order intercept points versus the frequency of one of the intermodulation tones. To determine the IIP2, one fixed 900 MHz tone (e.g., GSM) is used, whereas another input tone is swept in frequency from 100 MHz to 9.1 GHz. For intermodulation frequencies below 900 MHz the difference frequency is taken, for frequencies above 900 MHz the sum frequency is taken as the intermodulation frequency. An IIP2 of more than +20 dBm over the full 100 MHz–10 GHz range is achieved. This shows that using the combination of distortion canceling of the CG and the optimum

bias for the CS around the gain maximum (see Section IV-B), gives low overall second-order distortion.

The spread of IIP2 was measured on 20 samples, while keeping the biasing fixed. The worst case was found to be +18 dBm while other samples showed an IIP2 as high as +34 dBm. To improve this IIP2 value further, and guarantee it over temperature and process spread, it is beneficial to apply calibration techniques, as is more and more done in mixers [20], [21]. An effective approach is for instance to use $V_{biasCG}$ to tune the gain of the CS-stage, while using the bulk of the CG-stage to equalize the gain of the CG- and CS-stage. Simulations show a gain error <0.1 dB for all process-corners and a temperature range of −40 to +100 °C, with a worst case IIP2 = +23 dBm for fast N, fast P at −40 °C and a best case IIP2 = +33 dBm for nominal process at −40 °C (nominal case IIP2 = +27 dBm at 27 °C).

The IIP3 is determined using two closely spaced tones and is around 0 dBm. The increase in IIP3 with frequency can be explained by the increasing impedance mismatch at the input. The capacitance at the input of the chip input shunts the signal to ground at higher frequencies. Consequently, for the same input power there is less voltage swing on the input-transistors at higher frequencies than in the lower frequency range. This results in less distortion and an increased IIP3.

Overall, the results show that capacitive effects in the balun-LNA play only a minor role over most of the bandwidth.

### E. Benchmarking to Other Designs

Table I shows a comparison of the balun-LNA to three other wideband CMOS active baluns [1]–[3], two passive baluns implemented in CMOS [22] and GaAs [23] and two wideband

inductorless single-ended LNAs [4] and [24]. The proposed balun-LNA is more wideband than the passive integrated baluns [22], [23] while showing smaller gain and phase imbalances. The LNA performance of the implemented circuit is competitive to non-balun LNAs [4] and [24]. The circuit is integrated in a digital baseline 65 nm process using baseline transistors and a 1.2 V supply voltage. Still, at this low supply voltage, it achieves high linearity and the active area is small, as no integrated inductors are required. In contrast to [1] the balun-LNA presented in this work simultaneously achieves impedance matching, noise canceling and a well-balanced output.

## VII. Conclusion

In this paper we analyzed the performance of a parallel common-gate (CG) and common-source (CS) stage for operation as a wideband balun-LNA. We showed that it is possible to achieve simultaneous output balancing, noise canceling and distortion canceling. This requires admittance scaling of the CS-stage with respect to the CG-stage. Compared to a traditional balun design with equally sized CG and CS devices this circuit achieves better noise. Compared to equal load impedance designs, output balancing is achieved and a lower noise figure can be achieved. Moreover, we show that very good linearity can be achieved if the CS-stage has good linearity. In particular, it is shown that an interesting optimum IIP2 point exists in which the $v_{gs} \cdot v_{ds}$ cross-term cancels the traditionally dominant square-law term. Table I shows that this leads to a balun-LNA with very competitive performance in terms of output balancing, noise figure and linearity, while using standard 65 nm transistors at the standard 1.2 V supply voltage.

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