Wideband Coplanar Waveguide RF Probe Pad to Microstrip Transitions Without Via Holes

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***Abstract*—A novel via-less coplanar waveguide (CPW) to microstrip transition is discussed and design rules based on simulations and experimental results are presented. This transition demonstrates a maximum insertion loss of 1 dB over the frequency range from 10 GHz to 40 GHz with a value of 0.4 dB at 20 GHz. This transition could find a variety of applications due to its compatibility with RF systems-on-a chip, low loss performance, low cost and its ease of fabrication.**

***Index Terms*—CPW, microstrip, transition, via-hole.**

I. Introduction

AS THE DEMAND for high density and high performance microwave and millimeter wave circuits increases, RF devices become smaller and more highly integrated. Often these devices are fabricated with different type of transmission lines. One of the most commonly used transmission lines in RF circuit design is the microstrip due to its compact size, ease of fabrication and low cost. However, low cost, rapid characterization of microwave integrated circuits currently requires coplanar waveguide probe pads. Thus, a transition from the CPW probe pads to the microstrip line is required. In order to achieve the highest possible integration, while maintaining each circuit's effective performance, transitions are needed to reduce the mismatch and coupling between different circuit elements. One important class of transition is the coplanar waveguide (CPW) to microstrip transition. In [1]–[3], via-less transitions based on radial stubs and sections of coupled lines were developed. These transitions typically require an extensive design process and are not compact for frequencies below 30 GHz. Transitions with via holes have also been developed [4].

This paper presents for the first time design guidelines for the development of a compact, wideband transition from a coplanar waveguide (CPW) probe pad to a microstrip line that does not require any connection (vias) between the CPW ground strips and the microstrip backside ground plane and is also simple to design. The transition was designed and fabricated on silicon substrate with a center frequency of 20 GHz. The Method of Moments (MoM) was used to both verify the experimental results and optimize the design.

Manuscript received April 21, 2003; revised September 29, 2003. This work was supported by the Georgia Electronics Design Center of the State of Georgia and the NSF under Grant ECS –0218732. The review of this letter was arranged by Associate Editor Dr. Rüdiger Vahldieck.

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Digital Object Identifier 10.1109/LMWC.2003.820638

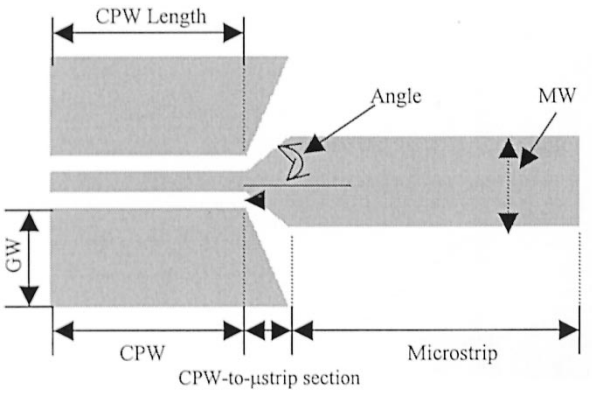

Fig. 1. Top view of the CPW to microstrip transition structure requiring no vias (bottom ground plane everywhere).

II. Transition Circuit Description

Fig. 1 shows the schematic of the CPW to microstrip transition. The complete structure consists of a CPW section, a CPW-to-microstrip transition section, and a microstrip section. In the intermediate transition section, the width of the CPW signal strip is gradually increased to match the width of the microstrip. At the same time, the gap between the ground planes and the signal line is widened to retain a 50 Ω characteristic impedance in order to match that of the microstrip line, and minimize reflections. As shown in Fig. 1, "GW" is the width of CPW ground plane width, "MW" is the width of the microstrip line which is 460 μm to obtain a 50 Ω impedance. The substrate is high resistivity silicon with $\varepsilon_r = 11.7$, $\rho > 5000\ \Omega - \mathrm{cm}$, a thickness of 400 μm and a SiO_2 layer of 1 μm. The signal line width of the CPW is 104 μm while the slot (gap) width is 80 μm. In order to better understand this transition and derive some design guidelines, the CPW section length ("CPW Length" in Fig. 1) and the angle ("Angle" in Fig. 1) of the transition between CPW and the microstrip were studied and varied. The length of the intermediate section can be calculated as long as the angle is given.

High resistivity silicon wafer was used to prevent the energy leakage through the substrate; the thickness of 400 μm of the substrate and the excitation mechanism (RF CPW probes) also contribute to the minimization of the presence of the microstrip mode in the coplanar section [5]. Furthermore, by choosing ground plane widths much smaller than $\lambda/2$, parallel plate and higher order modes can be avoided [6].

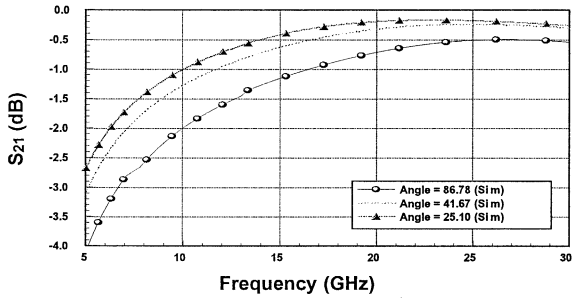

Fig. 2. Simulated insertion loss versus frequency for different transition angles.

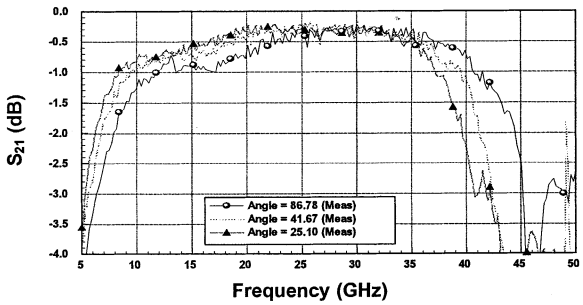

Fig. 3. Measured insertion loss versus frequency for different transition angles.

III. Simulations and Measurements

Full wave simulations for various combinations of geometrical parameters were performed with *Agilent Momentum* to reduce the insertion loss, and optimize the design in terms of size and operating bandwidth. To facilitate on-wafer measurements, each structure was fabricated as two CPW-to-microstrip transitions (back-to-back configuration). In order to compare on the same basis with the simulated results, one half of the insertion loss (dB) was deducted from the measured results and compared with the simulated results. Fabrication was done on the high resistivity silicon substrate mentioned above. The metallization layer for the transmission lines was 2 μm of plated Au. Gold was also plated everywhere on the backside of the substrate to provide the ground plane. Measurements were performed with the HP8510 Network Analyzer and calibrated with the SOLT method.

The measured and simulated results with respect to different transition angles and CPW lengths are shown in the following figures.

Fig. 2 displays the simulated loss from 5 to 30 GHz, for design angles ranging from 25.1° to 86.7°. For this experiment, the "GW" was fixed to 800 μm and the CPW length was chosen as 400 μm. The specific angles were chosen because they correspond to the intermediate section length of 10 μm, 200 μm, and 380 μm for an angle of 86.78°, 41.67° and 25.1°, respectively. As it is shown in the figure, when the angle decreases, the insertion loss gets smaller. This is expected, since as the angle decreases, the transition between the CPW to microstrip becomes smoother, and the sharp discontinuities are reduced. An angle below 40° is good enough to produce practically the optimum results.

Fig. 3 shows the measured loss from 5 to 50 GHz. This graph shows that the measured and simulated results agree very well

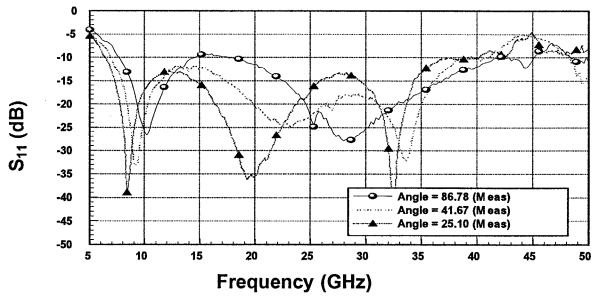

Fig. 4. Measured return loss versus frequency with different transition angle.

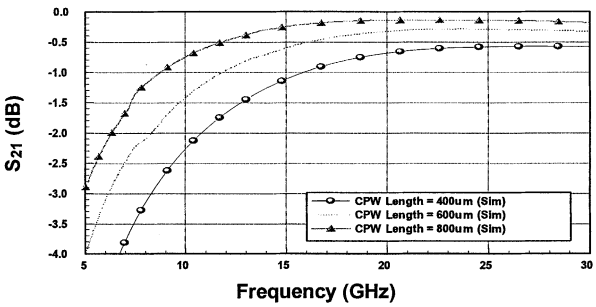

Fig. 5. Simulated insertion loss versus frequency for different CPW section lengths.

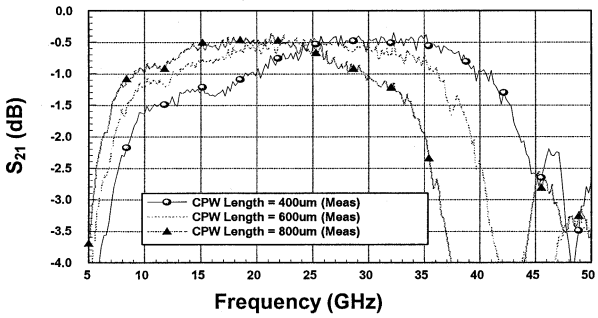

Fig. 6. Measured insertion loss versus frequency with different CPW lengths.

and that around 40° the insertion loss is optimized in terms of value and bandwidth. More specifically, for this angle the loss is below 1 dB from 10 to 40 GHz, with a value of 0.4 dB at 20 GHz. The 3-dB bandwidth is 185%. For smaller angles, the difference in loss is very small, but the bandwidth performance deteriorates. The angle of 41.67° was chosen as the nominal value for further investigation of the transition.

Fig. 4 shows the measured return loss for the different transition angles. It can be observed, that the return loss is optimized for the smallest angles, as expected and that for the 41.67° angle, the return loss is better than 12 dB from 7 to 37 GHz.

Fig. 5 shows the simulated insertion loss for different CPW lengths as defined in Fig. 1, and for a transition angle of 41.67°. The width "GW" was chosen to be 500 μm, to reduce the total size of the structure and also reveal the effect of the finite ground plane. As it can be seen, when the CPW lengths change from 400 μm to 600 μm to 800 μm, the transition exhibits a better performance.

Fig. 6 is a plot of the measured insertion loss from 5 to 50 GHz. It clearly shows that from 5 to 25 GHz, the loss decreases as the CPW section length increases and above 25 GHz the opposite effect occurs. For a length of 600 μm

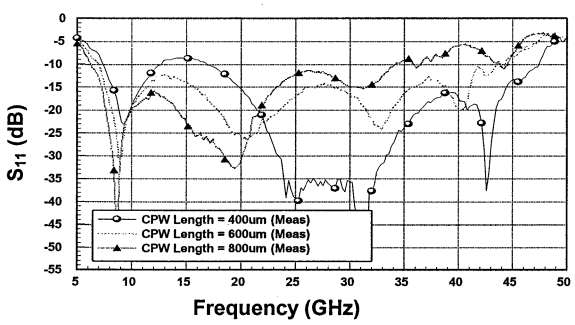

Fig. 7. Measured return loss versus frequency with different CPW lengths.

the loss is less than 1 dB from 12 to 36 GHz, with a value of 0.5 dB at 20 GHz. Taking into account the effective dielectric constant for the CPW section, it was found that 400 μm, 600 μm and 800 μm of line length corresponds to 0.067 λg, 0.1 λg and 0.133 λg at 20 GHz, respectively. This shows that in order to get an optimum insertion loss for the frequency of interest, the CPW length needs to be around 0.1 λg. The latter allows the coplanar mode to build-up and is the best compromise for optimum loss and bandwidth. Comparing Figs. 3 and 6, it can be seen that the former graph shows a slightly smaller insertion loss. This is expected since the CPW ground plane size is reduced to 500 μm from 800 μm for the latter study, which results in the smaller total capacitance from the CPW ground plane to microstrip ground plane, thus, the electrical reactance X between the probe ground and the microstrip ground increases, in other words, the impedance between the probe ground and microstrip ground increases slightly [3].

Fig. 7 shows the measured return loss for the transition with the different CPW lengths. As it is seen, the return loss is optimum (value and bandwidth) for the 600 μm length. For this length, the return loss is better than 13 dB from 7.5 to 42 GHz, and a return loss of 26 dB was measured at 20 GHz. For a longer length (800 μm), the return loss is larger than 11 dB from 7 to 34 GHz.

IV. Conclusion

In this letter, a novel CPW to microstrip transition was presented. This transition does not require any vias between the CPW ground planes and the microstrip backside ground plane; therefore it simplifies the fabrication and lowers significantly the production cost. Measurements showed that a loss of 0.4 dB can be achieved at 20 GHz, while the loss is below 1 dB from 10 to 40 GHz for an angle around 41°. In addition, the CPW length should be approximately 0.1 λg at the design frequency for the optimum result. To the authors' knowledge, this is the smallest reported loss with widest bandwidth ($\sim 185\%$) for such a compact and via-less transition. Future work in this area may involve extending the transition to different substrates and frequency ranges.

Acknowledgment

The authors would like to thank Dr. G. Ponchak for useful conversations on moding issues of coplanar lines.

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