Wideband Injection-Locked Divide-by-3 Frequency Divider Design with Regenerative Second-Harmonic Feedback Technique

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***Abstract*—This paper presents an integration of wideband injection-locked divide-by-3 frequency divider with regenerative second-harmonic feedback technique. By using the proposed feedback technique, a divider with a wide input locking range over 10% can be achieved at Ka-band, which performs near the device maximum oscillation frequency (f_{MAX}) in a CMOS 0.18-μm process. The divider can operate from 33.9 GHz to 37.7 GHz with an input injection power of 0 dBm. The measured input locking range is 3.8 GHz (10.6%). The chip area of the divider core is 0.22 mm^2. The core power consumption is 11.9 mW at a supply voltage of 0.9 V. At an offset frequency of 200 KHz, the measured output phase noise under lock is -121 dBc/Hz as the input signal with phase noise of -111.5 dBc/Hz is applied. The difference of 9.5 dB in phase noise is close to the theoretical value predicted by the theorem of division-by-3.**

Keywords-injection-locked frequency divider (ILFD), divide-by-three, wide input locking range, Ka-band.

I. INTRODUCTION

Because of the needs of wideband millimeter-wave communication systems [1] and radar applications [2], wideband phase-locked loops (PLLs) become the essential and critical blocks in microwave and millimeter-wave transceivers. In such PLLs, the first stage divider (i.e., the prescaler), which plays an important role to keep the circuit function correctly, has to directly scale down the output frequency of the voltage-controlled oscillator (VCO) that operates at the highest frequency. The injection-locked frequency divider (ILFD) is much suitable for first stage divider design due to its capability of high operation frequency with low power dissipation. However, compared to the other topology such as digital dividers, the relatively narrow input locking range of an ILFD is the challengeable issue when concerning to cover the whole tuning range of VCO under the process, voltage, and temperature (PVT) variations. Hence, how to enlarge the locking range of the first stage ILFD in a PLL is an important topic at microwave and millimeter-wave regime.

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An ILFD with a high-division-ratio is attractive since it can reduce the needed numbers of divider stages, the power dissipation, and the chip area consumption simultaneously [3]. However, when the operation frequency increases, the input locking range of high-division-ratio ILFDs is usually narrower than that of divide-by-2 ILFDs. In high-division-ratio ILFDs, the power level of high-order harmonics is naturally lower due to the serious high-frequency substrate loss in a lossy CMOS process. Hence, the input locking range will be reduced when the division-ratio increases [4]. As under the trade-off between the division-ratio and input locking range, divide-by-3 ILFDs could be the optimal solution in the first stage of a wideband PLL.

Many divide-by-3 ILFDs, which are fabricated in CMOS processes and operated at K-band and Ku-band regime, have been reported [5]-[9]. The cascode differential injection divide-by-3 ILFD incorporating with the shunt-peaking technique to enlarge the locking range has been proposed in [5]. But, when the frequency increases, the peaking level will be limited due to serious substrate loss. The divide-by-3 ILFDs using transformer and linear mixer techniques as reported in [6]-[7] can extend the input locking range. But the bonding wires adopted in [6] and [7] are difficult to be integrated and result in extra packaging cost. The direct injection by a floating source injector [8] also can be applied to the divde-by-3 ILFDs to widen the locking range. However, increasing the source impedance of the injector becomes difficult due to the substrate loss when the operation frequency increases. The transformer-feedback divide-by-3 ILFD [9] can operate with low power consumption, but on-chip transformer design will need a lot of effort to get a stable wideband operation.

In this paper, the divide-by-3 ILFD using regenerative second-harmonic feedback technique is proposed to compensate the input locking range degradation due to high frequency substrate loss and further extend the input locking range in lossy CMOS process. Therefore, wide input locking

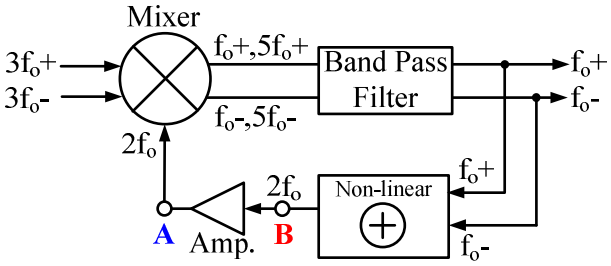


Figure 1. The block diagram of the proposed divide-by-3 ILFD.

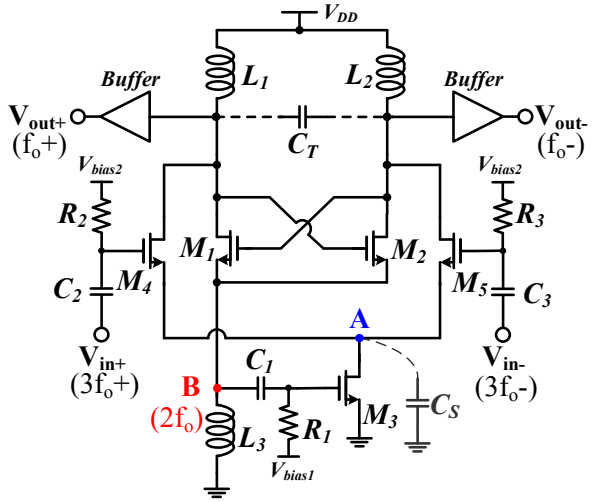


Figure 2. The circuit schematic of the proposed divide-by-3 ILFD

range divide-by-3 ILFD can be achieved in this work and it has high potential to be incorporated in wideband Ka-band PLLs.

II. CIRCUIT DESIGN

Fig. 1 illustrates the block diagram of our proposed divide-by-3 ILFD. The second-harmonic ($2f_0$) of the output signal can be obtained from a signal combiner (e.g., the common-mode node of a differential transistor pair) and fed into an amplifier for the amplification of the second-harmonic signal. Then, the regenerated and amplified second-harmonic is fed back to a mixer to mix with differential input signals for producing the two frequency terms at $3f_0 \pm 2f_0$. By this proposed technique, this mixing methodology can be accomplished with higher conversion gain. By filtering out all the unwanted signals with the band-pass filter, the desired fundamental differential signals at f_0 can be obtained at the output nodes. It is worth to note that the enlarged output signals will again enhance the second harmonics ($2f_0$) in sequence for feedback. When this loop is locked, the output frequency will exactly be equal to one-third of input frequency.

The circuit schematic of the proposed circuit is shown in Fig. 2. The free-running oscillator core of the ILFD is composed of the NMOS-only cross-coupled pair (M_1–M_2), the switching pair (M_4–M_5), and the LC tank that includes L_1, L_2, and total parasitic capacitance C_T. The cross-coupled pair (M_1–M_2) produces negative resistance for compensating the loss of

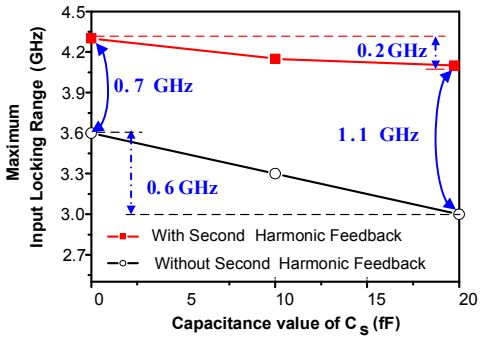


Figure 3. The simulated maximum input locking ranges versus different capacitance values of C_S, with and without second-harmonic feedback.

the LC tank. The second-harmonic ($2f_0$) can be obtained at the common node of M_1 and M_2. The inductor L_3 is employed to resonate with the AC coupled capacitor C_1 and the stray parasitic capacitance at the node B. Then, the second-harmonic can be peaked. The mixing circuit in this work is realized by a single-balanced mixer which includes the RF transconductance stage (M_3) and the input switching pair (M_4 – M_5). The peaked second-harmonic ($2f_0$) is fed into the transconductance stage to accomplish the regeneration of the second-harmonic; the differential input signals at $3f_0$ are directly injected into the switching stage and then the frequency terms of $3f_0 \pm 2f_0$ can be generated at the output ports. By utilizing the band-pass filter (i.e., the LC tank of free-running oscillator core), only the signal at f_0 can be preserved. Finally, for the measurement consideration, two buffers in a self-biased inverter topology are also integrated on chip for driving the 50Ω output loads.

The impact of conversion gain of the mixing circuit on the performance of an ILFD has been discussed in [10]. The input locking range increases with the conversion gain, since a higher conversion gain means a greater amplitude of injection signal that can be obtained to lock the free-running oscillator. Such concept also can be applied to our proposed circuit, where the conversion gain is defined as the power gain of the second-harmonic to the fundamental. Increasing the conversion gain or enhancing the amplitude of second-harmonic both can improve the input locking range. According to this reason, the regenerative second-harmonic feedback design is adopted in this work. In the feedback path, we peak the common-mode node impedance of M_1–M_2 at $2f_0$ to enhance the amplitude of second-harmonic. The transconductance stage employed in mixing circuit can increase the conversion gain, and then the input locking range can be extended significantly.

Fig. 3 shows the simulated maximum input locking ranges versus different capacitance values of C_S with and without the regenerative second-harmonic feedback technique. The input power is equal to 0 dBm. The capacitor Cs is connected at node A for modeling the high frequency substrate losses. The higher capacitance value of C_S will stand for the more substrate losses. In the case of the divide-by-3 ILFD without the regenerative second-harmonic feedback, we just remove the AC coupled capacitor (C_1) to break the second-harmonic feedback loop so that the transconductance stage is out of function consequently.

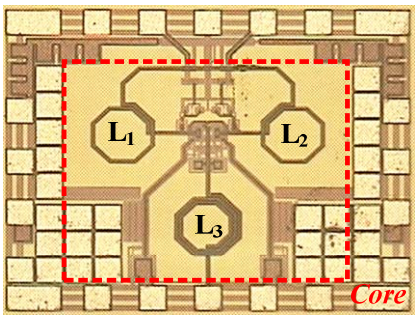
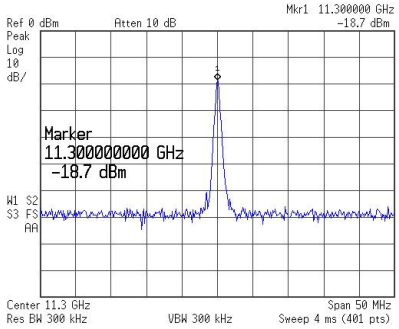
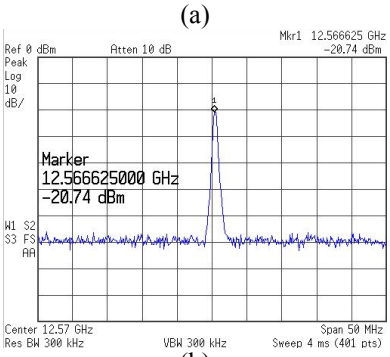


Figure 4. The chip photography of this work. Total chip size of core is 0.52 mm × 0.43 mm.



(a)



(b)

Figure 5. Measured output spectrum of the locked frequency at (a) input frequency= 33.9 GHz and (b) input frequency= 37.7 GHz.

According to the simulation results, our proposed divide-by-3 ILFD with the regenerative second-harmonic feedback technique indeed have a wider input locking range. The improvement of input locking range is 0.7 GHz in a normal condition (without added C_S). Under a serious loss condition (e.g., C_S=20 fF), the improvement is obviously increased to 1.1 GHz. If the divide-by-3 ILFD is operating without a regenerative second-harmonic feedback, it will be lack of conversion gain enhancement for the second harmonic at node A. The amplitude of the second harmonic is thus lower than that with regenerative second-harmonic feedback. As the value of C_S increases, the amplitude of second harmonic will be degraded more and more. Hence, the input locking range will also be degraded and such degradation will get worse.

From the simulation results shown in Fig. 3, it is noted that even under the serious loss condition (C_S=20 fF), the locking

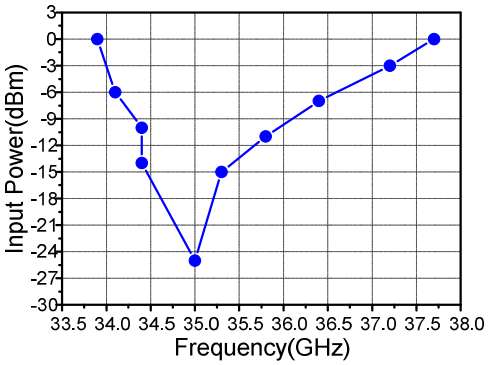


Figure 6. Measured curve of input sensitivity

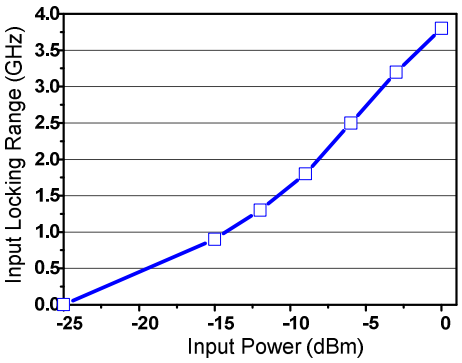


Figure 7. The measured input locking rang when the input power varies from -25 dBm to 0dBm

range degradation with the proposed second-harmonic feedback technique is only of 0.2 GHz as compared to that of 0.6 GHz without feedback. In other words, the proposed feedback technique can desensitize the loading effect of C_S. Hence, this proposed technique is very suitable for wideband PLLs operating in the millimeter wave frequency regime.

III. Measurement Results

The divide-by-3 ILFD using the regenerative second-harmonic feedback technique was fabricated in a 0.18-μm CMOS process and the chip photograph is shown in Fig.4. The chip size of core area is 0.52 mm × 0.43 mm (= 0.22 mm^2). The measured DC power consumption (P_{DC}) of the core is 11.9 mW at a supply voltage of 0.9V. The differential injection signals are generated by a signal generator with an external 180° hybrid coupler. The output performances are measured by a spectrum analyzer (Agilent E4440A). Fig. 5 shows the measured output spectrums locating at 11.3 and 12.56 GHz under locked, respectively, when the input frequencies are equal to 33.9 and 37.7 GHz. The output power over the whole operation range is around -17 dBm after the cable loss calibration at the input power of 0 dBm.

Fig. 6 shows the measured curve of input sensitivity. This work operates from 33.9 to 37.7 GHz without any tuning mechanism. The measured input locking rang is shown in Fig. 7 when the input power varies from -25 dBm to 0 dBm. The

TABLE I. The performance comparisons of our proposed divide-by-3 ILFD with other reported dividers

Ref.	Tech.	Pin (dBm)	Chip Area (mm^2)	P_{DC} (mW)	Input Operation Frequency (GHz)	Locking Range (GHz)
[5]	0.18-µm Epi-CMOS	4	0.81**	4.59	15.5~18.7	1
[7]	0.13-µm CMOS	0	0.83	2.05	12~17.1	2.6
[8]	0.18-µm CMOS	0	0.14*	8.28	21.7~24.9	3.2
[9]	0.13-µm CMOS	2	0.23	1.7	22.3~26.3	1.3
[11]	0.13-µm CMOS	5	0.68	13	58.2~60	1.8
This work	0.18-µm CMOS	0	0.22*	11.9	33.9~37.7	**3.8**

*core area only
** with on-chip balun

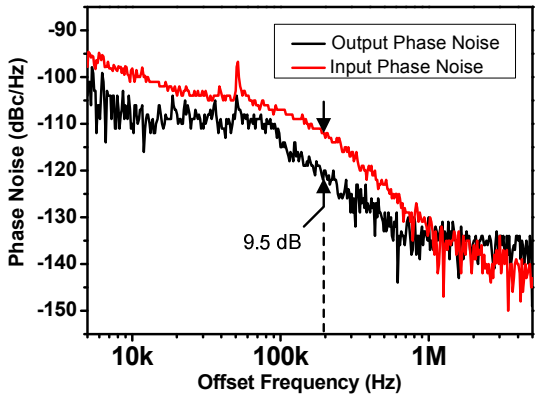


Fig. 8 The measured phase noises of input and output .

maximum input locking range is 3.8 GHz with respect to an injection-power level of 0 dBm. Fig. 8 shows that input and output phase noises are -121 and -111.5 dBc/Hz, respectively, at an offset frequency of 200 KHz. The difference of phase noise is about 9.5dB, which is close to the theoretical value.

Table. I summarizes the performance comparisons of our proposed divide-by-3 ILFD with other reported dividers [5], [7]-[9], and [11], using CMOS 0.18-µm or 0.13-µm processes. Generally, when the operation frequency increases, the input locking range of divide-by-3 ILFD becomes narrower since the high-order harmonic levels inherently become weaker in lossy CMOS process. However, among the previous works listed in Table. I, this work which utilizes the regenerative second-harmonic feedback technique can own the widest input locking range (of 3.8 GHz) at high operation frequency (from 33.9 GHz to 37.7 GHz), even just being fabricated by a CMOS 0.18-µm process.

IV. Conclusion

A wide input locking range K-band divide-by-3 ILFD has been successfully presented in a 0.18-µm RF CMOS process. This divide-by-3 ILFD uses the regenerative second-harmonic feedback technique to extend the input locking range. The measured input locking range is 3.8 GHz (from 33.9 to 37.7 GHz) with a DC power consumption of 11.9 mW. It is worth to note that the proposed regenerative second-harmonic feedback technique also can compensate the input locking range degradation when the divide-by-3 ILFD suffers from high frequency substrate losses. With the combined features of a wider input locking range and a higher tolerance to the substrate loss, the proposed regenerative second-harmonic feedback technique is very attractive to the wideband divide-by-3 ILFD design for the wideband millimeter-wave PLLs.

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