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# Wideband polarization splitter and rotator with large fabrication tolerance and simple fabrication process

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We propose and demonstrate a polarization splitter and rotator (PSR) built on a silicon-on-insulator platform. The PSR is constructed with a tapered waveguide followed by a  $2 \times 2$  multimode interferometer and can be simply fabricated in a single lithography and etching step. A low insertion loss ( $< 2.5$  dB with minimum insertion loss of 0.6 dB) and a low polarization crosstalk ( $< -12$  dB) over a wide operation bandwidth ( $\sim 100$  nm) with a large fabrication tolerance ( $> 50$  nm) are experimentally demonstrated. © 2013 Optical Society of America

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Silicon-on-insulator (SOI) microphotonic devices are very attractive thanks to their complementary metal oxide semiconductor (CMOS)-compatible fabrication technology, their high refractive index contrast, and compact size [1]. Those advantages make SOI microphotonic devices promising candidates for all-optical signal processing subsystems. However, the high refractive index contrast also introduces large polarization dependency, which becomes one of the major challenges for their practical use. In particular, if the device is to be used in a subsystem deployed over an optical fiber link, the polarization state of the optical signal at its input may change randomly over time, making standard SOI microphotonic devices no longer compatible with optical processing functionalities. To realize polarization independence, polarization diversity (Pol-D) circuits based on polarization splitter and rotator (PSR) technologies are typically used [2–4]. In this scheme, the input light contributions along the two orthogonal polarizations axes are first split by a polarization splitter [5]. After that, one of the two polarizations is rotated by  $90^\circ$  by a polarization rotator [6]. Thus, in the rest of the circuit, only one polarization needs to be processed. Many approaches have been proposed and demonstrated to realize PSRs. However, they all require a rather complex fabrication process [6–11]. To simplify the fabrication process, asymmetrical directional coupler (DC)-based PSRs have been recently proposed and demonstrated [12–14]. One of the main practical issues with many PSR designs is their limited fabrication tolerance, which makes them impractical for high-yield production. The best reported fabrication tolerance of  $\sim 14$  nm for a DC-based PSR was recently obtained using a tapered DC design [15].

In this Letter we propose and demonstrate a PSR built on the SOI platform. In this device, an adiabatically tapered waveguide first converts the  $TM_0$  to the  $TE_1$  mode, while also preserving the  $TE_0$  mode. A  $2 \times 2$  multimode interference (MMI) coupler, which is well-known for its large fabrication tolerance [16] and has been utilized for wide bandwidth polarization splitting/combining [17], is introduced afterward to effectively couple the  $TE_0$  and  $TE_1$  modes at the end of the  $TM_0$ – $TE_1$  mode converter to two distinct  $TE_0$  outputs. Simulation results show a large fabrication tolerance of 63 nm thanks to

the use of the MMI. A low insertion loss better than 2.5 dB, with minimum insertion loss of only 0.6 dB and polarization crosstalk lower than  $-12$  dB over a wide bandwidth of 100 nm, is demonstrated experimentally, together with a large fabrication tolerance better than 50 nm.

The principle of the proposed PSR is schematically depicted in Fig. 1(a). Light is first injected into a tapered waveguide and then split into two beams by a Y-splitter. Before being injected into the  $2 \times 2$  MMI, an extra phase difference of  $\pi/2$  is introduced between the two beams. In case of  $TE_0$  input, the mode will be preserved during the adiabatic taper and split into two  $TE_0$  beams with the same phase. Thus, at the MMI input, the two beams will have a  $\pi/2$  phase difference. By properly designing the MMI, light will output from arm 1 on the  $TE_0$  mode with little crosstalk in arm 2 [Fig. 1(b)]. On the other hand, in case of  $TM_0$  input, the light is converted to the  $TE_1$  mode during the adiabatic tapering [14] and split into two  $TE_0$  beams with  $\pi$  phase difference. Thus, at the MMI input, the two beams will have a  $-\pi/2$  phase difference, and light will consequently output from arm 2 on the  $TE_0$  mode

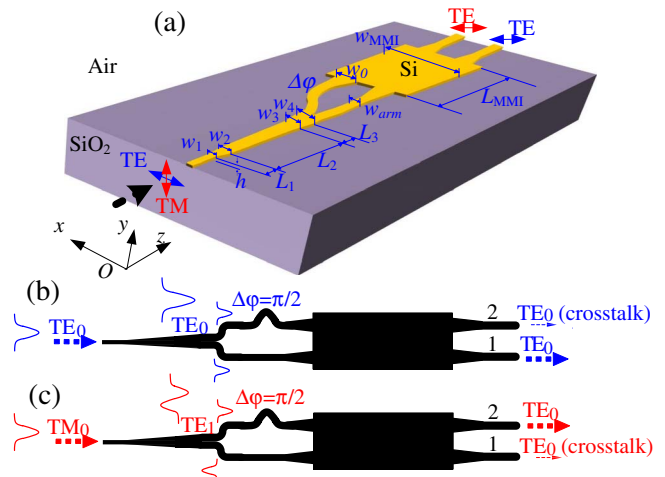


Fig. 1. (Color online) (a) Schematic structure of the proposed PSR.  $TE_0$  (b) and  $TM_0$  (c) light are input to the PSR, and output from arm 1 and 2, respectively, on the  $TE_0$  mode.

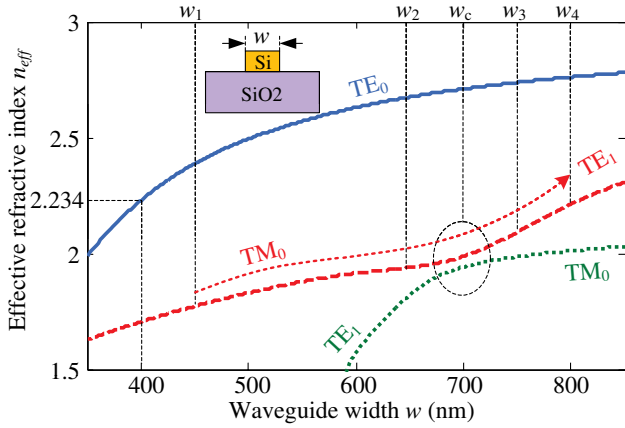


Fig. 2. (Color online) Effective indices of the  $TE_0$ ,  $TE_1$ , and  $TM_0$  modes of an air-clad SOI waveguide as a function of the waveguide width  $w$  for a waveguide height  $h = 250$  nm (simulated by FIMMWAVE [18]).

with little crosstalk in arm 1 [Fig. 1(c)]. To achieve an efficient  $TM_0$ - $TE_1$  polarization conversion, a material that is different from the buffer layer (silicon oxide) should be applied as top-cladding layer [14]. In our design, air is employed as top cladding material. To decrease the tapering length, the  $TM_0$ - $TE_1$  converter is divided into three sections, as shown in Fig. 1(a). The first section  $L_1$  is from input single mode silicon waveguide ( $w_1 = 450$  nm) to  $w_2 = 650$  nm. Since in this section there is no mode conversion, a short tapering length of  $10 \mu\text{m}$  is employed. Considering the  $TM_0$  and  $TE_1$  modes are hybridized around  $w_c = 700$  nm, as shown in Fig. 2, the second tapering section  $L_2$  is from  $w_2$  to  $w_3 = 750$  nm with a tapering length as long as  $120 \mu\text{m}$ , which can guarantee an efficient  $TM_0$ - $TE_1$  conversion, as shown in the inset of Fig. 3(a). The third section  $L_3$  is from  $w_3$  to  $w_4 = 800$  nm with tapering length of  $10 \mu\text{m}$ . The output end of the  $TM_0$ - $TE_1$  converter is then split to two arms with widths of  $400$  nm and connected to the  $2 \times 2$  MMI through tapering to  $w_0 = 700$  nm to improve the fabrication tolerance [16]. With a calculated effective index of  $2.234$ , the two arms are designed to have a length difference of  $173$  nm to introduce the required  $\pi/2$  phase difference. The  $2 \times 2$  MMI is designed to be of the symmetric type (excited at  $w_{\text{MMI}}/4$ ) with width of  $w_{\text{MMI}} = 2 \mu\text{m}$  and length of  $L_{\text{MMI}} = 13.7 \mu\text{m}$  based on three-dimensional finite difference time domain (3D FDTD) simulations. A restricted type MMI (excited at  $w_{\text{MMI}}/6$ ), which could efficiently decrease  $L_{\text{MMI}}$ , could also be used. In this case,  $w_{\text{MMI}}$  should be larger in order to sufficiently separate the two output waveguides.

In reality, a size deviation  $\Delta w_{\text{device}}$  may be introduced by the fabrication process for the whole device. Such a size deviation will influence the  $TM_0$ - $TE_1$  mode conversion in the adiabatic taper section and introduce a phase deviation from  $\pi/2$  between the two arms before the MMI, which further influences the whole performance of the device. Figure 3(a) shows the  $TM_0$ - $TE_1$  conversion efficiency for different width deviations of the adiabatic taper calculated using the eigenmode expansion method [18]. A large tolerance of  $\pm 40$  nm is expected for the adiabatic taper to guarantee a high  $TM_0$ - $TE_1$  conversion efficiency above 95%. To investigate the impact of a

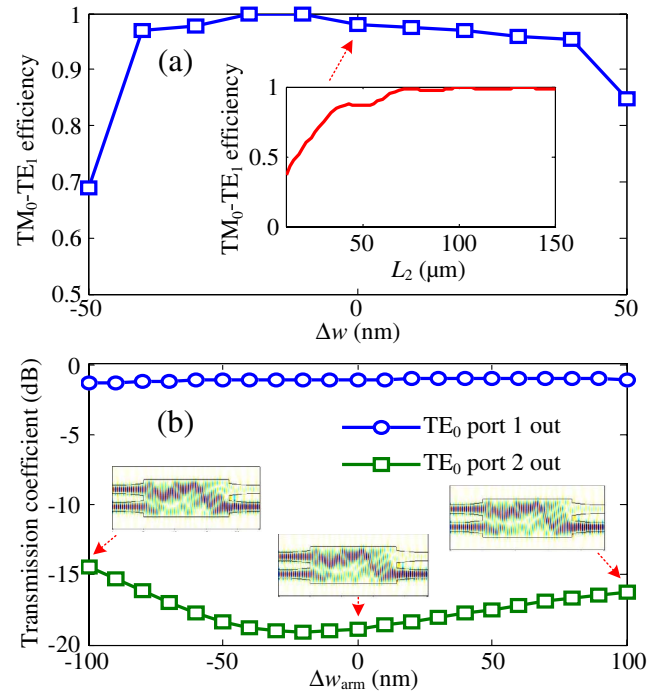


Fig. 3. (Color online) Calculated fabrication tolerance of (a) adiabatic taper based  $TM_0$ - $TE_1$  mode converter and (b)  $2 \times 2$  MMI. The inset in (a) shows the  $TM_0$ - $TE_1$  conversion efficiency as a function of  $L_2$ . The insets in (b) show the field distributions simulated by 3D FDTD.

width deviation of the two arms before the MMI, the width deviation is first converted to an effective index deviation according to Fig. 2, then to a phase deviation  $\Delta\phi$  for the two beams. 3D FDTD simulations are used to investigate the tolerance. In the simulations, two beams of light with phase difference of  $\pi/2 + \Delta\phi$  are injected into the MMI, and the two output powers are calculated as shown in the insets of Fig. 3(b). A large tolerance of  $\pm 100$  nm is obtained while the crosstalk is kept below 15 dB. Finally, for the MMI, in a Rayleigh range, a length tolerance can be estimated as  $\Delta L_{\text{MMI}} = \pi n_r w_0^2 / 4\lambda_0$  [16], where  $w_0$  is defined as the input Gaussian beam waist,  $n_r$  is the material refractive index, and  $\lambda_0$  is the operating wavelength. The corresponding width tolerance and operation bandwidth can be calculated as  $\Delta w_{\text{MMI}} = w_{\text{MMI}} \Delta L_{\text{MMI}} / 2L_{\text{MMI}}$  and  $\Delta\lambda_0 = \lambda_0 \Delta L_{\text{MMI}} / L_{\text{MMI}}$ , respectively [16]. With  $w_0 = 700$  nm,  $n_r = 3.476$ , and  $\lambda_0 = 1550$  nm, a length tolerance  $\Delta L_{\text{MMI}}$  of 860 nm, a width tolerance  $\Delta w_{\text{MMI}}$  of 63 nm, and a bandwidth  $\Delta\lambda_0$  of 98 nm are expected. Thus, an overall size deviation tolerance of  $\Delta w_{\text{device}} = 63$  nm is expected for the whole device with a bandwidth of 98 nm.

The device was fabricated on a SOI wafer (top silicon thickness 250 nm, buried silicon dioxide  $3 \mu\text{m}$ ) by a single step of E-beam lithography (JEOL JBX-9300FS) and inductively coupled plasma reactive ion etching (STS Advanced Silicon Etcher). Figure 4(a) shows the fabricated device with design parameters as introduced previously.

The total length of the device, including the  $140 \mu\text{m}$  long adiabatic taper-based  $TM_0$ - $TE_1$  mode converter, is  $190 \mu\text{m}$ . Note that the smallest feature size of the device is the inner corner of the Y-splitter, enabling our scheme to be fabricated with other methods [19]. Figure 4(b)

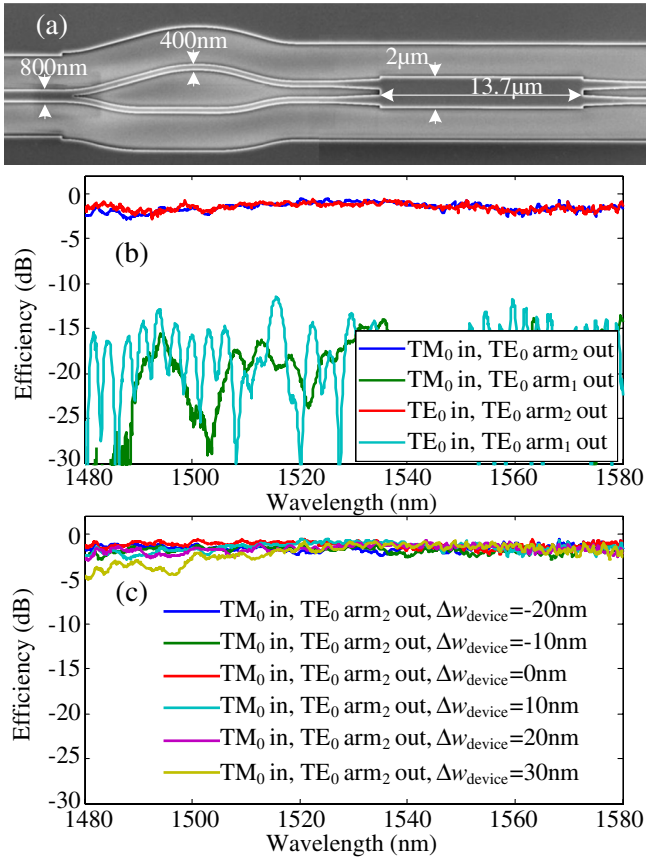


Fig. 4. (Color online) (a) Scanning electron microscope (SEM) picture of the fabricated device. (b) Measured coupling efficiency to the two output ports for TE<sub>0</sub> and TM<sub>0</sub> inputs. (c) Measured TM<sub>0</sub>-TE<sub>0</sub> conversion efficiency for different device size deviations.

shows the measurement results. Details on the measurement setup and calibration procedure can be found in [12]. A low insertion loss (from inputs on either the TM<sub>0</sub> or TE<sub>0</sub> mode to output arm 1 or 2 on the TE<sub>0</sub> mode, normalized to a straight waveguide) better than 2.5 dB with a minimum insertion loss of 0.6 dB and polarization crosstalk lower than -12 dB are obtained over a wide bandwidth of 100 nm. To improve the insertion loss, more efficient Y splitters with lower insertion loss should be used [20]. In addition, the polarization crosstalk can be improved by increasing the width of the 2 × 2 MMI so that the two output waveguides are separated sufficiently to avoid evanescent coupling between them. To further investigate the fabrication tolerance of the device, six devices with device size deviations from -20 nm to 30 nm were fabricated and characterized, as shown in Fig. 4(c). One can find that similar high

conversion efficiencies are obtained over a better than 50 nm device size deviation, in good agreement with the simulations.

In conclusion, we have proposed and demonstrated a PSR built on the SOI platform, which is fabricated by simple processing. A low insertion loss better than 2.5 dB with a minimum insertion loss of 0.6 dB and polarization crosstalk lower than -12 dB over a wide bandwidth of 100 nm are demonstrated together with a large fabrication tolerance better than 50 nm.

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