Window-Based Susceptance Models for Large-Scale RLC Circuit Analyses†

Hui Zheng[1], Byron Krauter[2], Michael Beattie[1], Lawrence Pileggi[1]

[1]Carnegie Mellon University
Department of Electrical and Computer Enginnering
5000 Forbes Avenue
Pittsburgh, PA 15213

[2]IBM Corporation
11400 Burnett Road
Austin, TX 78758

ABSTRACT

Due to the increasing operating frequencies and the manner in which the corresponding integrated circuits and systems must be designed, the extraction, modeling and simulation of the magnetic couplings for final design verification can be a daunting task. In general, when modeling inductance and the associated return paths, one must consider the on-chip conductors as well as the system packaging. This can result in an RLC circuit size that is impractical for traditional simulators. In this paper we demonstrate a localized, window-based extraction and simulation methodology that employs the recently proposed susceptance (the inverse of inductance matrix) concept. We provide a qualitative explanation for the efficacy of this approach, and demonstrate how it facilitates pre-manufacturing simulations that would otherwise be intractable. A critical aspect of this simulation efficiency is owed to a susceptance-based circuit formulation that we prove to be symmetric positive definite. This property, along with the sparsity of the susceptance matrix, enables the use of some advanced sparse matrix solvers. We demonstrate this extraction and simulation methodology on some industrial examples.

1. Introduction

Today's integrated circuits and systems rely on several layers of complex on-chip wiring and short, sometimes complex connections to off-chip packaging to transmit signals and deliver power reliably. While the noise generated and received by these interconnects -- particularly the power and ground lines -- can ultimately determine whether or not a system properly functions, a detailed analysis for pre-manufacturing verification is often impossible. Simulating these behaviors is impractical primarily for two reasons: 1) the extraction runtime can be extremely long and memory requirements can be very large due to the large number of conductors involved; And 2) even if we can construct the inductance matrix, traditional simulators can not simulate the resulting circuits in a reasonable amount of time due to the number of mutual coupling terms (density of the inductance matrix).

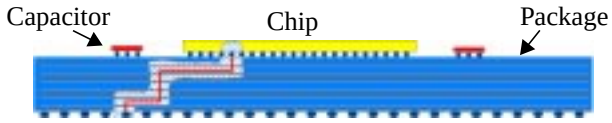

Fig. 1: Simultaneous Switching Analysis

As an example, to guarantee the integrity of the signal lines in a state-of-the-art electronic IC package, simultaneous switching analysis is required. Referring to Fig. 1, we would have to trace tens of signal lines travelling from the chip to the card through the package. However, due to magnetic coupling, the power and ground network surrounding the signal lines would also have to be included to provide the accurate return path information. To create an accurate representation of the simulation problem, tens or even hundreds of thousands of conductors would be required to represent the interconnect system.

For a complex interconnect system it has become a standard practice to model three-dimensional inductance using the concept of partial inductance [6]. For integrated circuits and systems it is used primarily because the return paths can not be determined prior to the extraction and simulation of an interconnect system. The drawback of this approach is that the resulting inductance matrix is extremely large and dense, and arbitrarily discarding terms to sparsify it can destroy the positive definiteness and thereby render the corresponding circuit model unstable [8]. A shift-truncate strategy has been devised to sparsify the partial inductance matrix while preserving its positive definiteness [5]; however, the shell radius has to be chosen to be large enough so that the shell encompasses the possible return paths.

Very recently the concept of susceptance has emerged as an alternative way of modeling magnetic couplings [1, 3]. As the inverse of a partial inductance matrix, a susceptance matrix has properties similar to a capacitance matrix (the inverse of a potential matrix). Firstly, susceptance inherently provides a shielding effect whereby the mutual susceptance terms drop off much faster than the mutual inductance terms with distance. Secondly, a susceptance matrix is diagonally dominant which guarantees its positive definiteness under simple truncation. As a result, window-based extraction can be used to build a sparse susceptance

†This work was supported by Semiconductor Research Corporation (SRC) under contract 2000-TJ-778 and International Business Machines Corporation (IBM).

matrix by piecing together the localized extraction window results.

Compared to other provably stable localized inductance extraction approaches [5, 8], the window size for susceptance can be made smaller and does not necessarily have to include the actual return paths to achieve a certain accuracy. We provide a qualitative explanation for this important characteristic of susceptance in Section 2.

We also demonstrate further advantages of the sparse susceptance matrix formulation. In Section 3 we prove that the corresponding nodal-analysis equations based on the susceptance models are symmetric positive definite (s.p.d.). Because sparse s. p. d. matrices can be solved more efficiently than general sparse matrices [11], this property allows us to substantially speed up the simulation process.

In Section 4 we contrast window-based susceptance extraction to shift and truncate inductance extraction. And finally in Section 5 we demonstrate this combined extraction and simulation methodology on an industrial example from a production design that was otherwise impossible to fully analyze prior to manufacturing.

2. Stepping-Stone Behavior of Susceptance Models in Transient Simulation

The recent work in [1, 3, 4] clearly showed truncated susceptance (or K) models are more accurate in transient circuit simulation than shift and truncated inductance models, and provided some physical meaning for this new circuit element. These papers did not however, clearly explain the reasons for the improved accuracy. We believe the accuracy differences can be intuitively understood by comparing the inductance based and susceptance based companion models and examining the behavior of these models in a small circuit example. What the reader will observe in the following paragraphs, is that sparse susceptance models like sparse capacitance models, provide a high degree of indirect coupling through any floating or high-impedance interconnects.

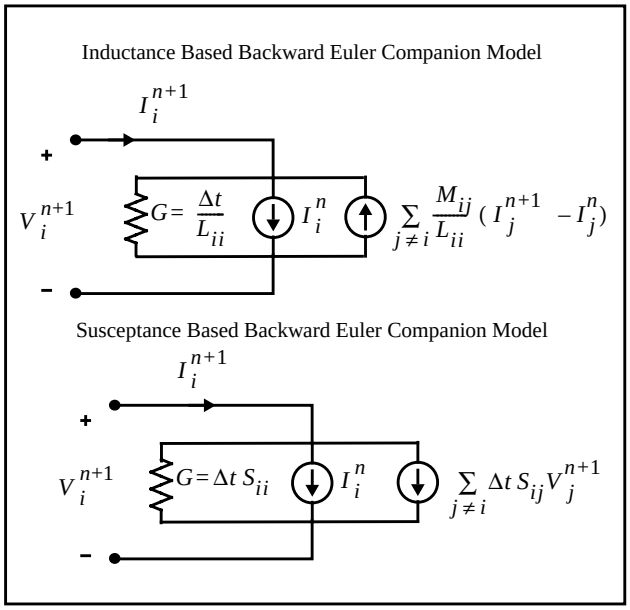

Fig. 2: Inductance and Susceptance Based Backward Euler Companion Models for a Coupled

Consider the Backward Euler companion models depicted in Fig. 2 for an inductor L_i at time step n+1. For ease of comparison, both the inductance and susceptance based companion models have been cast in their Norton equivalent forms. Note that the inductance model employs current controlled current sources while the susceptance model employs voltage controlled current sources. This difference is the root cause of the indirect coupling in sparse susceptance models that is not present in sparse inductance models.

Consider the circuit depicted in Fig. 3. While it looks unusual, this example might represent a large capacitance C_L being driven through the first and last wires of a long ribbon cable with all the wires in between grounded at the near end of the cable. If the load capacitance C_L is much larger than the wire capacitances, the wire capacitances can be ignored and this strange looking model will, provided that the full L matrix is used, accurately model the transient behavior of the cable.

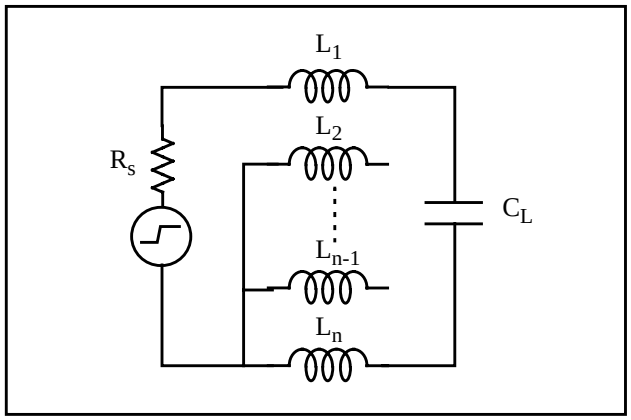

Fig. 3: Circuit example that demonstrates indirect coupling in sparse susceptance models

Now let's compare what happens when the sparse inductance and susceptance models are used instead. Because wires 2 through n-1 are open circuited at the far end of the cable, currents I_2 through I_{n-1} are zero. This eliminates any indirect coupling in the sparse inductance model because the inductance based companion model uses current controlled current sources.

Indirect coupling, however, still occurs in the sparse susceptance model even in the absence of any branch currents in S_2 through S_{n-1}. When a voltage develops across S_1, the voltage controlled current source in the S_2 companion model produces a voltage across S_2. This voltage drop in turn produces a current in the S_3 companion model and a voltage drop across the S_3 element. And so on and so on.

3. Symmetric Positive Definiteness of S-based Formulation for Transient Simulation

In this section, we will prove the important property which makes the susceptance-based formulation superior to the inductance-based formulation: symmetric positive definiteness. For comparison, the inductance-based formulation is also shown. We assume that there is no voltage source in the circuits, which can almost always be satisfied for timing or noise analysis since Norton equivalent circuits can be used to model the driving gates. For clarity, we only show the derivations for Backward Euler integration method, but the conclusions will also apply for Trapezoidal integration method.

For an inductance-based circuit, the differential linear system can be represented as:

$$\begin{bmatrix} G & A_L \\ -A_L^T & 0 \end{bmatrix} \begin{bmatrix} V_n \\ I_L \end{bmatrix} + \begin{bmatrix} C & 0 \\ 0 & L \end{bmatrix} \begin{bmatrix} \dot{V}_n \\ \dot{I}_L \end{bmatrix} = \begin{bmatrix} -A_{CS} I_{CS} \\ 0 \end{bmatrix} \tag{1}$$

where $G = A_R G_0 A_R^T$ and $C = A_C C_0 A_C^T$. The complete incidence matrix for the circuit contains four parts for resistors, capacitor, inductors and current sources:

$$A = \begin{bmatrix} A_R & A_C & A_L & A_{CS} \end{bmatrix} \tag{2}$$

G_0 and C_0 are diagonal matrices.

By integrating Eq. (1) by BE method, we get:

$$\begin{bmatrix} G & A_L \\ -A_L^T & 0 \end{bmatrix} \begin{bmatrix} V_n(t+\Delta t) \\ I_L(t+\Delta t) \end{bmatrix} \Delta t + \begin{bmatrix} C & 0 \\ 0 & L \end{bmatrix} \begin{bmatrix} V_n(t+\Delta t) - V_n(t) \\ I_L(t+\Delta t) - I_L(t) \end{bmatrix} = \begin{bmatrix} -A_{CS} I_{CS}(t+\Delta t) \\ 0 \end{bmatrix} \Delta t \tag{3}$$

After collecting some terms, we can further obtain the linear system for the inner-loop solve at each time point:

$$\begin{bmatrix} G + \frac{C}{\Delta t} & A_L \\ -A_L^T & \frac{L}{\Delta t} \end{bmatrix} \begin{bmatrix} V_n(t+\Delta t) \\ I_L(t+\Delta t) \end{bmatrix} = \begin{bmatrix} -A_{CS} I_{CS}(t+\Delta t) + \frac{C}{\Delta t} V_n(t) \\ \frac{L}{\Delta t} I_L(t) \end{bmatrix} \tag{4}$$

As we can see, the matrix on the left-hand side is not a symmetric system. We could force it to be symmetric by negating the second row in the equation:

$$\begin{bmatrix} G + \frac{C}{\Delta t} & A_L \\ A_L^T & -\frac{L}{\Delta t} \end{bmatrix} \begin{bmatrix} V_n(t+\Delta t) \\ I_L(t+\Delta t) \end{bmatrix} = \begin{bmatrix} -A_{CS} I_{CS}(t+\Delta t) + \frac{C}{\Delta t} V_n(t) \\ -\frac{L}{\Delta t} I_L(t) \end{bmatrix} \tag{5}$$

However, the matrix turns out to be an indefinite matrix.

Next, we will demonstrate that for a susceptance-based circuit, the matrix for the inner-loop system is not only smaller, but also provably symmetric positive definite. For a susceptance-based circuit, the differential linear system is a little different:

$$\begin{bmatrix} G & A_L \\ -SA_L^T & 0 \end{bmatrix} \begin{bmatrix} V_n \\ I_L \end{bmatrix} + \begin{bmatrix} C & 0 \\ 0 & I \end{bmatrix} \begin{bmatrix} \dot{V}_n \\ \dot{I}_L \end{bmatrix} = \begin{bmatrix} -A_{CS} I_{CS} \\ 0 \end{bmatrix} \tag{6}$$

where $S = L^{-1}$. We do not differentiate between the incidence matrices for the self susceptors and the corresponding self inductors, for they are the same.

Similarly, the BE-integrated equation is:

$$\begin{bmatrix} G & A_L \\ -SA_L^T & 0 \end{bmatrix} \begin{bmatrix} V_n(t+\Delta t) \\ I_L(t+\Delta t) \end{bmatrix} \Delta t + \begin{bmatrix} C & 0 \\ 0 & I \end{bmatrix} \begin{bmatrix} V_n(t+\Delta t) - V_n(t) \\ I_L(t+\Delta t) - I_L(t) \end{bmatrix} = \begin{bmatrix} -A_{CS} I_{CS}(t+\Delta t) \\ 0 \end{bmatrix} \Delta t \tag{7}$$

which can be split into the upper and lower parts. After some manipulations, the upper part is written as:

$$\left(G + \frac{C}{\Delta t}\right) V_n(t+\Delta t) + A_L I_L(t+\Delta t) = \frac{C}{\Delta t} V_n(t) - A_{CS} I_{CS}(t+\Delta t) \tag{8}$$

and the lower part can be conveniently organized as:

$$I_L(t+\Delta t) = SA_L^T \Delta t V_n(t+\Delta t) + I_L(t) \tag{9}$$

Substituting (9) into (8), we obtain the nodal-analysis representation of the inner-loop system:

$$\left(G + \frac{C}{\Delta t} + A_L S A_L^T \Delta t\right) V_n(t+\Delta t) = \frac{C}{\Delta t} V_n(t) - A_{CS} I_{CS}(t+\Delta t) - A_L I_L(t) \tag{10}$$

Theorem. For a connected circuit which only contains resistors, capacitors, susceptors and current sources, the linear system for the inner-loop solve is symmetric positive definite.

Proof. We only prove the theorem for BE integration method. For the Trapezoidal case, the only difference for the matrix is that Δt is replaced by $\Delta t/2$ and the same conclusion holds.

The matrix in (10) can be represented in another way with the incidence matrices:

$$G + \frac{C}{\Delta t} + A_L S A_L^T \Delta t = \tilde{A} \begin{bmatrix} G_0 & 0 & 0 \\ 0 & \frac{C_0}{\Delta t} & 0 \\ 0 & 0 & S\Delta t \end{bmatrix} \tilde{A}^T \tag{11}$$

where $\tilde{A} = \begin{bmatrix} A_R & A_C & A_L \end{bmatrix}$. The matrix in the middle is a positive definite matrix, since the three individual matrices on the diagonal are positive definite.

It is a well-known fact in graph theory that: [7]

If A(G) is an incidence matrix of a connected graph G with N vertices, the rank of A(G) is N-1.

For circuit analysis, the common reference node is omitted in the incidence matrix formulation, so the incidence matrix in (2) is of full rank. Furthermore, except for some pathological cases, removing current sources in a cir-

cuit does not change the connectedness of the circuit. Therefore, the following holds:

$$rank(A) = rank(\tilde{A}) = n \tag{12}$$

where n is the number of non-reference nodes, i.e., the number of rows of the incidence matrices.

For any non-zero n-dimensional vector X, we have: $\tilde{A}^T X \neq 0$ since all the columns in $\tilde{A}^T$ are linearly independent. Consequently,

$$X^T\left(G + \frac{C}{\Delta t} + A_L S A_L^T \Delta t\right)X = X^T \tilde{A} \begin{bmatrix} G_0 & 0 & 0 \\ 0 & \frac{C_0}{\Delta t} & 0 \\ 0 & 0 & S\Delta t \end{bmatrix} \tilde{A}^T X > 0 \tag{13}$$

which is exactly the definition of a positive definite matrix. QED

The positive definiteness of the NA formulation was also pointed out in a recent paper [10]. However, the inductance and susceptance matrices were assumed to be diagonal. We prove that the positive definiteness holds for more general susceptance matrices.

4. Window-based Susceptance versus Shift and Truncate Inductance Extraction

When comparing window-based susceptance extraction to shift and truncate inductance extraction, it's important to specify the frequency context of the final model. That is, whether the extraction method produces a low-frequency or high-frequency model. The relative cost of the two methods changes based on the model of interest.

For a low-frequency model, the shift and truncate inductance extraction is cheaper. The conductor currents are assumed to be uniformly distributed, and the partial inductances are computed directly using partial inductance formulas and shift and truncate adjustments [5]. The S matrix computation, however, requires a matrix inversion of the same (or a similar) partial inductance inductance matrix, $S = L^{-1}$. While this additional cost can be minimized by the window technique which only requires the calculation of one column in the S matrix for each local window [1], the additional step makes window-based susceptance extraction necessarily more expensive.

For a high-frequency model, the shift and truncate inductance extraction is more expensive because it now has a extra step. The conductor currents are not assumed to be uniform and individual conductors are subdivided into smaller cross-sections in order to capture proximity and skin effects [12]. The bigger partial inductance matrix L_d can be formed similarly as in the low-frequency case, but the high-frequency port inductance model can only be obtained after first computing the high-frequency port susceptance model.

To be more explicit, the high frequency port susceptance matrix is calculated by: $S_p = AL_d^{-1}A^T$, where A is the incidence matrix for all filaments, and the high-frequency port inductance matrix L_p is be obtained by inverting S_p. Finally the shift and truncate adjustments are made to the high-frequency port inductance model L_p. While any additonal cost can again be minimized by a similar window-based strategy, the computational expense of sparse inductance extraction will necessarily be higher than sparse susceptance extraction if the high-frequency effects need to be considered.

While extraction can be time-consuming, it is not the bottleneck in large RLC circuit analysis, since both localization methods - window-based susceptance and shift and truncate inductance extraction - can be readily parallelized to reduce both the time and memory requirements. Instead, the bottleneck in RLC circuit analysis is simulation for its large memory usage, and as the next section will demonstrate, sparse susceptance models are clearly superior to sparse inductance models for the subsequent simulation problem.

5. Results for a Package Example

We have implemented the window-based susceptance extraction methodology in [1] and the simulation strategy presented in this paper into a set of prototype tools in an industrial setting. Our prototype simulation tool uses fixed time step integration and employs various direct and iterative matrix solvers. The results presented here were obtained using the symmetric solver in WSMP [9] [Watson Sparse Matrix Package].

In order to test the accuracy and show the superiority of the susceptance-based approach, a very efficient inductance-based extraction and simulation flow was also implemented in which the shell-based shift-truncate strategy from [5] was used to sparsify the L matrix and the general part of WSMP (considered possibly the best general direct sparse solver available) solves the inner-loop linear system in (4). All of the following experimental results are from an RS/6000 Model 397 workstation.

One application of our flow is to model and simulate the simultaneous switching activities as illustrated in Fig. 1. In our example, there are 9 adjacent signal lines running from one chip to another chip on an MCM package. The power/ground meshes and vias surrounding the signal lines are also included for extraction. We performed three extractions on the 9299 segments involved in this system: 1) S-based extraction (referred to as S later). We chose the window size to be big enough to cover the nearest and second-

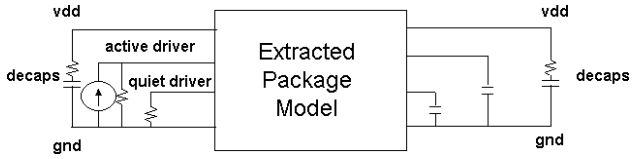

Fig. 4: Simulation Configuration for Chip to Chip Simultaneous Switching Analysis on an

nearest neighbors. As a result, the windows do not necessarily enclose the return paths; 2) accurate L-based extraction (La). We chose the radius to be big enough so that the shell encompasses the possible return paths. 3) sparser L-based extraction (Ls). The radius used is smaller so that the sparsity of the L matrix is close to that of the S matrix. The numbers of mutual terms and densities of the three S or L matrices are shown in Table 1.

The simulation configuration for simultaneous switching analysis is shown in Fig. 4. In the peripheral circuits, the active drivers are modeled as Norton equivalents, and decoupling capacitors are placed to balance the power and ground noise. Since we only want to compare S-based and L-based approaches for magnetic coupling, we use the same extracted capacitance matrix for all of the following simulations.

One simulation setting is that we switch all the 9 signal lines simultaneously and then check the delay and noise on the center line. Fig. 5 shows the voltage waveforms at the near-end and far-end of the center signal line for different L/S-based circuit decks. As we can see, the results from S and La are very close in term of capturing the delay and peak noise, while Ls results are a bit off. However, the inaccuracy of Ls can be shown more evidently in Fig. 6. This simulation setting is that we keep the center line quiet and switch all the other 8 lines to see how much noise can be generated on the center line. This time Ls results are far off while S and La results are still pretty close. These two experiments validate that the S-based extraction can capture magnetic couplings accurately with an S matrix which can be much sparser than a shift-truncated L matrix.

	L/S Matrix (#muts / density)	NA/MNA Matrix (size / #nonzeros)	Memory Usage (Mb)	Simulation Time (sec)
S	68643 / 0.09%	15277 / 557729	137.9	110.7
La	193160 / 0.23%	24576 / 478089	507.1	858.7
Ls	67265 / 0.09%	24576 / 226299	416.5	773.9

Table 1: Comparison of Runtime & Memory Usage

Table 1 tabulates the comparison of memory usage and run-times for L and S-based simulations. Although the L-based simulations are already very fast because of the use of

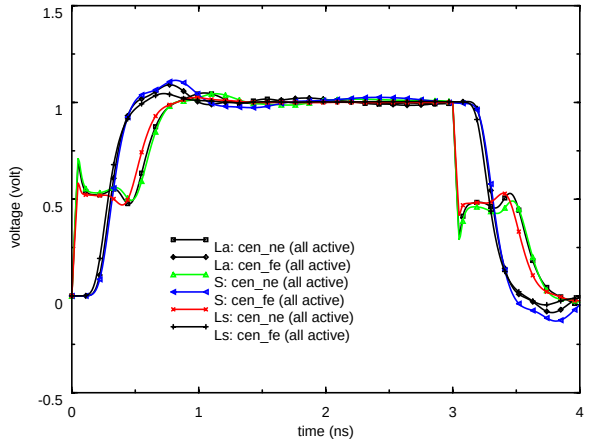

Fig. 5: Simulation results for all-active case

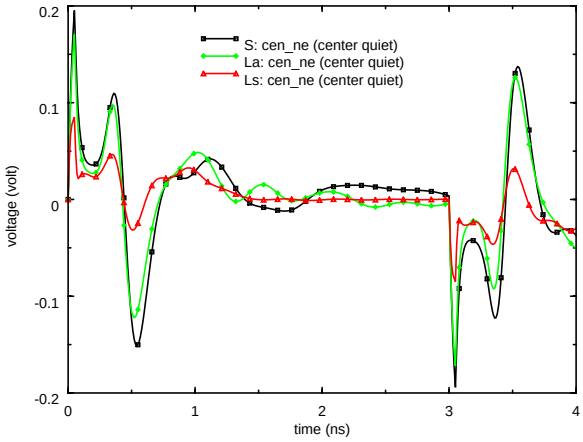

Fig. 6: Simulation results for center-quiet case

WSMP, the S-based simulation still outperforms them with a 7-8x speed-up and a 2-3x memory saving. It is interesting to note that there are more nonzeros in the S-based NA matrix than the L-base MNA matrices. However, as we have discussed in Section 4, the symmetric positive definiteness of the S-based NA matrix enables Cholesky method and better ordering algorithms which significantly bring down the number of potential fill-ins and consequently the memory usage.

6. Conclusions

In this paper, we have demonstrated the multiple advantages of susceptance-based approach for modeling and simulating magnetic couplings in a large interconnect system. For the modeling part, we show that the stepping-stone phenomenon ensures that a sparse S matrix preserves the long-distance coupling information through indirect couplings; for the simulation part, we prove that the S-based formulation is symmetric positive definite, which is the key property that some advanced sparse matrix solvers exploit to reduce runtime and memory usage. The application of the S-based methodology to an industrial package example demonstrates that the S-based simulation is superior to the L-based simulation with significant speed-up and memory savings.

7. Acknowledgments

The authors would like to thank Frank Liu for providing the interface to matrix solvers and Anand Haridass for providing the package example.

References

[1] M. Beattie and L. Pileggi, “Efficient Inductance Extraction via Windowing,” in Proc. Design Automation & Test in Europe, pp. 430-436, March, 2001

[2] M. Beattie and L. Pileggi, “Modeling Magnetic Coupling for On-Chip Interconnect”, in Proc. 38-th Design Automation Conference, pp. 335-340, June 2001.

[3] A. Devgan, H. Ji, and W. Dai., “How to Efficiently Capture On-Chip Inductance Effects: Introducing a New Circuit Element K,” in Proc IEEE International Conference on Computer Aided Design, pp. 150-155, Nov. 2000

[4] H. Ji, A. Devgan, and W. Dai, “KSim: A Stable and Efficient RKC Simulator for Capturing On-Chip Inductance Effect”, in Proc ASP-DAC 2001, pp. 379-384. Jan 2001.

[5] B. Krauter and L. Pileggi, “Generating Sparse Partial Inductance Matrices with Guaranteed Stability,” in Proc. IEEE International Conference on Computer Aided Design, pp. 45-52, Nov. 1995.

[6] D. Ling and A. Ruehli, *Circuit Analysis, Simulation and Design -- Advances in CAD for VLSI, Vol. 3, Part II*, Chapter 11, Elsevier Science Publisher B. V., North-Holland, 1987

[7] N. Deo, *Graph Theory with Applications to Engineering and Computer Science*, Chapter 7, Prentice-Hall Inc., 1974

[8] Z. He, M. Celik and L. Pileggi, “SPIE: Sparse Partial Inductance Extraction,” in Proc. 34-th Design Automation Conference, pp. 137-140, June 1997

[9] A. Gupta. “WSMP: Watson Sparse Matrix Package,” Technical Report RC 21888 (98472), IBM T. J. Watson Research Center, NY, Nov. 2000

[10] T. Chen and C. Chen, “Efficient Large-Scale Power Grid Analysis Based on Preconditioned Krylov-Subspace Iterative Methods,” in Proc. 38-th Design Automation Conference, pp. 559-562, June 2001

[11] A. George and J. Liu, *Computer Solution of Large Sparse Positive Definite Systems*, Prentice-Hall Inc., 1981

[12] W. T. Weeks, L. L. Wu, M. F. McAllistor, and A. Singh. “Resistive and Inductive Skin Effect in Rectangular Conductors”, IBM Journal of Research and Development, vol. 23, November 1979.