Wireless NoC as Interconnection Backbone for Multicore Chips: Promises and Challenges

Sujay Deb, *Student Member, IEEE*, Amlan Ganguly, *Member, IEEE*, Partha Pratim Pande, *Senior Member, IEEE*, Benjamin Belzer, *Member, IEEE*, and Deukhyoun Heo, *Member, IEEE*

***Abstract*—Current commercial systems-on-chips (SoCs) designs integrate an increasingly large number of predesigned cores and their number is predicted to increase significantly in the near future. For example, molecular-scale computing promises single or even multiple order-of-magnitude improvements in device densities. The network-on-chip (NoC) is an enabling technology for integration of large numbers of embedded cores on a single die. The existing method of implementing a NoC with planar metal interconnects is deficient due to high latency and significant power consumption arising out of long multi-hop links used in data exchange. The latency, power consumption and interconnect routing problems of conventional NoCs can be addressed by replacing or augmenting multi-hop wired paths with high-bandwidth single-hop long-range wireless links. This opens up new opportunities for detailed investigations into the design of wireless NoCs (WiNoCs) with on-chip antennas, suitable transceivers and routers. Moreover, as it is an emerging technology, the on-chip wireless links also need to overcome significant challenges pertaining to reliable integration. In this paper, we present various challenges and emerging solutions regarding the design of an efficient and reliable WiNoC architecture.**

***Index Terms*—Bandwidth, energy dissipation, network-on-chip (NoC), wireless interconnect.**

I. Introduction

THE CONTINUING progress and integration levels in silicon technologies make possible complete end-user systems on a single chip. This massive level of integration makes modern multi-core chips all pervasive in domains ranging from weather forecasting, astronomical data analysis and biological applications, to consumer electronics and smart phones. Network-on-chips (NoCs) have emerged as communication backbones to enable a high degree of integration in multi-core systems-on-chip (SoCs) [1]. Despite their advantages, an important performance limitation in traditional NoCs arises from planar metal interconnect-based multi-hop communications, wherein the data transfer between two far apart blocks causes high latency and power consumption. There have been some efforts to address this problem by introducing ultra-low-latency and low power express channels between highly separated nodes [2] and high radix networks [3]. Although these communication channels are significantly more efficient in terms of power and delay compared to their conventional counterparts, they are still metal wires. According to the International Technology Roadmap for Semiconductors (ITRS) [4], improving characteristics of metal wires will no longer satisfy performance requirements and new interconnect paradigms are needed. Different approaches such as 3-D, photonic NoCs and NoC architectures with multi-band radio-frequency (RF) interconnects (RF-I) [5]–[9] have already been explored. All these approaches reduce the latency and power dissipation to some degree, but they do not generally solve the difficult problem of laying out interconnects across the chip. Moreover, 3-D and photonic NoCs must overcome technological and manufacturing challenges to become viable for mass production. Though RF-I NoCs can be built using existing complementary metal–oxide–semiconductor (CMOS) technology, they require laying of long on-chip transmission lines to serve as wave guides, without eliminating any existing links [9].

Recent research has established characteristics of silicon integrated antennas operating in the millimeter (mm)-wave range of a few tens to one hundred gigahertz and it is now a viable technology for intra- and inter-chip communication [10]. Moreover excellent emission and absorption characteristics leading to antenna-like behavior in carbon nanotubes (CNTs) operating at optical frequencies have been observed recently [11]. These findings open up new opportunities for detailed investigations into the design of wireless NoCs (WiNoCs) with on-chip antennas and suitable transceivers. On-chip wireless communication links not only alleviate the latency and energy dissipation issues of conventional technologies but also eliminate complex interconnect routing and layout problems arising in some of the alternative technologies. Hence, such interconnects enable design of novel and efficient architectures which mitigate the multi-hop communication of traditional NoCs to achieve significant performance gains. WiNoCs present unique opportunities and challenges, which should be explored to make them mainstream. This paper presents a detailed survey regarding the promises and design challenges of this emerging paradigm.

II. Physical Layer Design

The effectiveness of WiNoCs strongly depends on the design of the physical layer. In turn, the miniaturized on-chip antennas

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S. Deb, P. P. Pande, B. Belzer, and D. Heo are with the Department of Electrical Engineering and Computer Science, Washington State University, Pullman, WA 99164 USA (e-mail: sdeb@eecs.wsu.edu; pande@eecs.wsu.edu; belzer@eecs.wsu.edu; dheo@eecs.wsu.edu).

A. Ganguly is with the Department of Computer Engineering, Rochester Institute of Technology, Rochester, NY 14623 USA (e-mail: amlan.ganguly@rit.edu).

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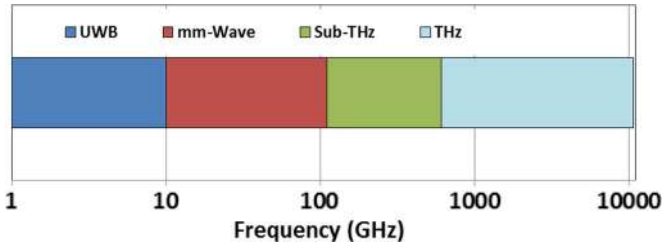

Fig. 1. Different frequency ranges used for wireless NoCs.

and the wireless transceivers influence the performance of the physical layer. Characteristics of the antennas and the transceivers also depend on the adopted frequency range of communication. WiNoC architectures explored so far by different research groups can be broadly classified into four classes depending on their frequency range of operation. Details of the range of frequency and corresponding classification are shown in Fig. 1.

A. Ultra Wide Band (UWB)

One possibility for WiNoC design is to use intra-chip ultra wide band (UWB) interconnections. A carrier-free impulse radio-based UWB transceiver has been utilized for WiNoCs [12]. The transmitter is designed to generate the desired pulse with suitable driving strength so that signal can be efficiently radiated from an on-chip antenna. A CMOS integrated Gaussian monocycle pulse (GMP) generator creates an ultra short pulse giving rise to extremely low power spectral density. The receiver consists of a wideband LNA, a correlator, an analog-to-digital converter (ADC), and synchronization circuits. The antenna used is a 2.98-mm-long meander type dipole antenna with 1 mm data transmission range. This UWB transceiver can sustain a data rate of 1.16 Gb/s for a single channel at a central frequency of 3.6 GHz.

B. Millimeter (mm)-Wave

According to the ITRS, the cutoff frequency and unity maximum available power gain frequency targets are 600 GHz and 1 THz, respectively, in 16 nm CMOS technology. With such scaling the required antenna and circuit areas will scale down allowing easy on-chip integration. Coupled with significant advances in mm-wave transceiver design this opens up new opportunities for detailed investigations into mm-wave WiNoCs. The on-chip antenna for the mm-wave WiNoCs has to provide the best power gain for the smallest area overhead. A metal zigzag antenna has been demonstrated to possess these characteristics and suits this application [10]. This antenna also has negligible effect of rotation (relative angle between transmitting and receiving antennas) on received signal strength. Zigzag antennas were initially used to demonstrate performance of on-chip wireless interconnects [13] for distributing clock signals. This antenna is used to design a millimeter (mm)-wave wireless NoC in [14]. As an example, we show the forward transmission gain (S21) of the zigzag antenna working in the 60 GHz range in Fig. 2. A 0.38-mm antenna achieves 3 dB bandwidth of 16 GHz with a center frequency of 57.5 GHz. By varying the axial

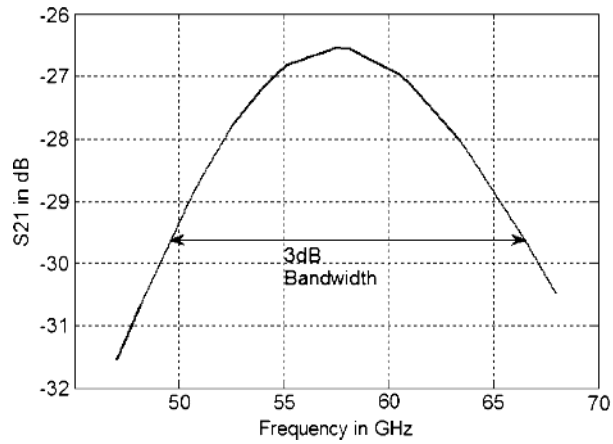

Fig. 2. Zigzag antenna transmission gain (S21) response.

length, trace width, arm element length and bend angle the antenna bandwidth can be varied. This type of antenna is also used to design a reconfigurable hybrid 3-D wireless NoC. By placing the antennas in different layers of a 3-D IC different frequency channels can be created [15].

At mm-wave frequencies the effect of metal interference structures such as power grids, local clock trees and data lines on on-chip antenna characteristics like gain and phase have been investigated [16]. It has been found that short metal lines running over antennas have negligible impact on antenna gain and phase, and the dummy fills needed for chemical mechanical polishing also have negligible effect. Hence, other metal wires in the vicinity of these antennas do not significantly affect their performance. The demonstration of intra-chip wireless interconnection in a 407-pin flip-chip package with a ball grid array (BGA) mounted on a PC board [17] has addressed the concerns related to influence of packaging on antenna characteristics. Design rules for increasing the predictability of on-chip antenna characteristics have been proposed in [16].

To ensure the high throughput and energy efficiency of the WiNoC, the transceiver circuitry has to provide a very wide bandwidth as well as low power consumption. The mm-wave frequency band can provide abundant bandwidth while not suffering from severe signal degradation, thanks to the short communication distances in the WiNoC. In designing the on-chip mm-wave wireless transceiver, low power design considerations need to be taken into account both at the architecture and circuit levels. In [18], a noncoherent on–off keying (OOK) based transceiver is designed for an mm-wave WiNoC. OOK is selected as it allows relatively simple and low-power circuit implementation. As illustrated in Fig. 3, the transmitter (TX) circuitry consists of an up-conversion mixer and a power amplifier (PA). On the receiver (RX) side, direct-conversion topology is adopted, consisting of a low noise amplifier (LNA), a down-conversion mixer and a baseband amplifier. An injection-lock voltage-controlled oscillator (VCO) is reused for TX and RX. With both direct-conversion and injection-lock technology, a power-hungry phase-lock loop (PLL) is eliminated. This transceiver can sustain a data rate of 16 Gb/s with power consumption of 43.6 mW in TSMC 65 nm process with an area requirement of 0.3 mm^2. Furthermore, using body

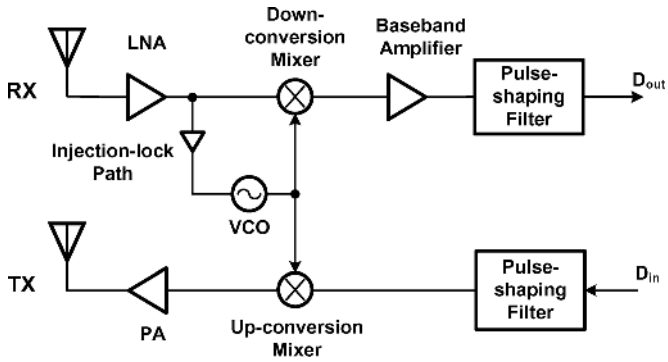

Fig. 3. OOK transceiver block diagram for mm-wave WiNoC.

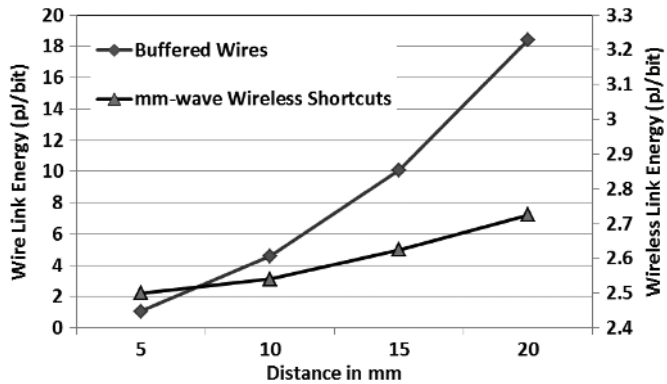

Fig. 4. The variation of energy dissipation per bit with distance for a wired and a mm-wave wireless link.

biasing methodology it is possible to improve energy efficiency without compromising the performance of high-speed analog and RF subsystems. Consequently, body biased mm-wave transceivers are capable of improving the energy efficiency of WiNoC architectures [19]. Using the above characteristics of the antennas and mm-wave transceivers, a comparative analysis of the energy dissipation per bit between the wireless and wired communication channels has been carried out in [19]. The wired channels are considered to be 32 bits wide and each link of the wired channel is designed with uniformly placed and sized repeaters for optimum delay. Fig. 4 presents how energy dissipated per bit changes as a function of length for both wireless and wired links. From this plot it can be observed that mm-wave wireless shortcuts are always energy efficient whenever the link length is 7 mm or more. Hence, implementation of long range links beyond 7 mm using mm-wave wireless makes the design energy efficient and simpler in terms of layout. An alternative approach to mm-wave WiNoCs proposes to use waveguide based multi-band transmission lines called RF-I, wherein electromagnetic (EM) waves are guided along on-chip transmission lines created by multiple layers of metal and dielectric stack [9]. As the EM waves travel at the effective speed of light, low latency and high bandwidth communication can be achieved. RF-I NoCs are predicted to dissipate an order of magnitude less power than traditional planar NoCs with significantly reduced latency. Here, RF-I based on BPSK modulation is used. RF-I performance with scaling is elaborated in [9] and using 65 nm technology it is possible to have eight different frequency channels, each operating with a data rate of 6 Gb/s. But these RF-I transmission line based interconnects face several challenges in the many-core setting [20]. The RF-I transmission line needs to span the entire chip area, and requires excessive branching points to connect to local cores. Moreover, the transmission lines are not as effective as antennas at very high frequencies. The cross-talk or inter-channel interference between adjacent transmission lines may also pose problems for long transmission lines [20].

C. Sub Terahertz (Sub THz)

The feasibility of designing miniature antennas and simple transceivers that operate in the sub-THz frequency range for on-chip wireless communication has been demonstrated in [20]. This work is based on the fact that with the CMOS technology scaling the size and cost of the antenna and required transceiver circuits will decrease dramatically. From an electromagnetic point of view, high resistivity silicon is desired to avoid substrate loss. Moreover, as proposed in [20], the on-chip antenna can be placed in a polyimide layer to reduce substrate loss. Using this technique it is possible to extend the communication range up to 10–20 mm.

It is predicted that it is possible to have 16 nonoverlapping channels in the frequency range of 100–500 GHz for the on-chip wireless networks. Each channel can transmit at a rate of 10–20 Gb/s in 32-nm CMOS process. However, the issues of inter-channel interference due to multiple adjacent frequency channels remain unresolved in this work. In a 1000-core chip multiprocessor design, the total aggregate data rate is predicted to be as high as 320 Gb/s.

A simple asynchronous amplitude-shift-keying (ASK) based system is proposed to achieve a low power and simple transceiver design. It has one oscillator and one ASK modulator in the TX and one demodulator and simple baseband circuit in the RX. With such simple transceiver architecture, it is predicated to use only 1%–2% of the total system power of the considered chip multiprocessor (CMP) [20].

D. Terahertz (THz)

If the transmission frequencies can be increased to THz/optical range then the corresponding antenna sizes decrease, occupying much less chip real estate. Antenna characteristics of carbon nanotubes (CNTs) in the THz/optical frequency range have been investigated both theoretically and experimentally [11]. These antennas can achieve a bandwidth of around 500 GHz, whereas antennas operating in the millimeter wave range achieve bandwidths of tens of gigahertz. Thus, antennas operating in the THz/optical frequency range can support much higher data rates. CNTs have numerous characteristics that make them suitable as on-chip antenna elements for optical frequencies. Given wavelengths of hundreds of nanometers to several micrometers, there is a need for virtually 1-D antenna structures for efficient transmission and reception. With diameters of a few nanometers and any length up to a few millimeters possible, CNTs are the perfect candidate. Such thin structures are almost impossible to achieve with traditional micro fabrication techniques for metals. Virtually defect-free CNT structures do not suffer from power loss due to surface

TABLE I
SUMMARY OF RECENTLY PROPOSED WiNoC PHYSICAL LAYER CHARACTERISTICS

Frequency Range	Technology Node	Antenna Used	Modulation Scheme	Trans-mission Range	Data Rate (Gbps)	Energy per bit
UWB [12]	180 nm	Meander type dipole	Pulse position modulation (PPM) or biphase modulation (BPM)	1 mm	1.16	Not available
mm-Wave [14]	65 nm	Zigzag antenna	Non-coherent on-off keying (OOK)	20 mm	16	2.3 pJ
Sub THz [20]	32 nm	Not available	Amplitude-shift keying (ASK)	10-20 mm	320	4.5 pJ
THz [22]	Not Applicable	Multi-walled carbon nanotube (MWCNT) antennas	Non-coherent on-off keying (OOK)	23 mm	240	0.33 pJ

roughness and edge imperfections found in traditional metallic antennas. In CNTs, ballistic electron transport leads to quantum conductance, resulting in reduced resistive loss, which allows extremely high current densities, 4–5 orders of magnitude higher than copper. By shining an external laser source on the CNT, radiation characteristics of multi-walled carbon nanotube (MWCNT) antennas are observed to be in excellent quantitative agreement with traditional radio antenna theory, although at much higher frequencies of hundreds of THz [11]. Using various lengths of the antenna elements corresponding to different multiples of the wavelengths of the external lasers, scattering and radiation patterns are shown to improve. High directional gains of these antennas, demonstrated in [11], aid in creating directed channels between source and destination pairs. Using this technology 24 nonoverlapping channels each with 10 Gb/s bandwidth can be created [21], [22]. Hence, CNT antenna-based wireless link is another possibility for WiNoC design as shown in [22]. A noncoherent OOK based transceiver is used here.

Table I summarizes the characteristics of the various physical layers used for designing WiNoCs working in different frequency ranges. All these physical layers designed in different frequency bands have antenna and transceiver area and power overheads. Thus, architectural innovations are required to achieve the best performance-overhead trade off and fully exploit the advantages of wireless links.

III. WiNoC ARCHITECTURE

The goal of on-chip communication system design is to transmit data with low latencies and high throughput using the least possible power and resources. Currently, the major challenges in traditional wire-based NoCs are the high latency and power consumption of their multi-hop links. Design of suitable on-chip antennas, wireless routers and transceiver circuits enable efficient wireless links that can be used optimally to maximize overall network performance without excessive overhead. We broadly classify the WiNoC architectures into two sub categories, viz. mesh-topology based where the wireless links are principally inserted on top of a regular mesh and small-word network based.

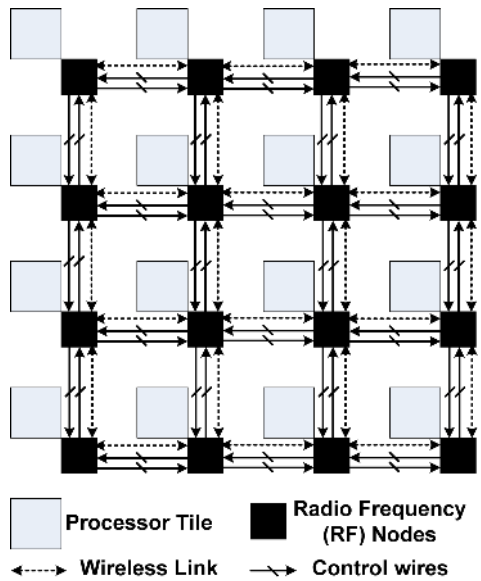

Fig. 5. UWB 4 × 4 2D mesh architecture.

A. Mesh-Topology Based NoCs

This section discusses the different WiNoC architectures that are variants of the traditional mesh topology.

In [12] the design of a wireless NoC based on CMOS ultra wideband (UWB) technology is demonstrated. This work considers tiled multi-core design. The processor tiles access the network via RF nodes and their packets are delivered to destinations through one or multiple hops across the network. Fig. 5 illustrates such a NoC organized in a 4 × 4 2D mesh. This NoC is demonstrated to achieve 23.3% average performance (execution time) improvement and 65.3% average end-to-end latency reduction over a baseline mesh-based wire line NoC consisting of 64 cores.

A two-tier hybrid wireless/wired architecture to interconnect hundreds to thousands of cores in CMPs using sub-THz wireless links is proposed in [20]. This architecture benefits from the baseline 2-D concentrated mesh to provide a base network with very short wires and exploits a wireless backbone to enhance connectivity, reducing network latency. The sub-THz wireless infrastructure is a recursive structure called the WCube that features a single transmit antenna and multiple

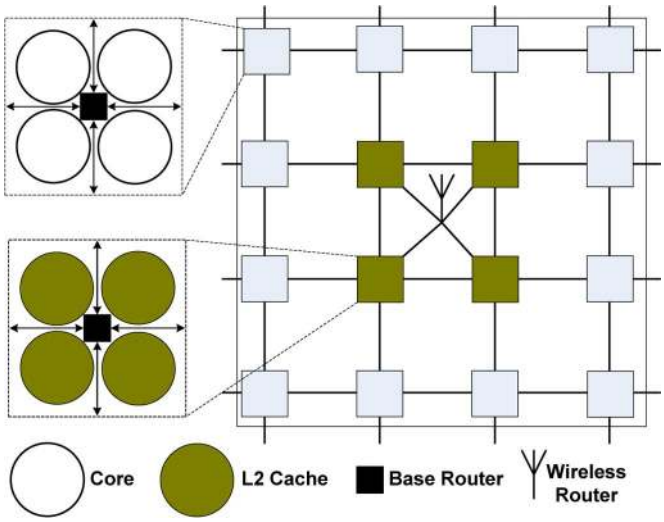

Fig. 6. WCube structure of a cluster of 16 base routers (i.e. 64 nodes).

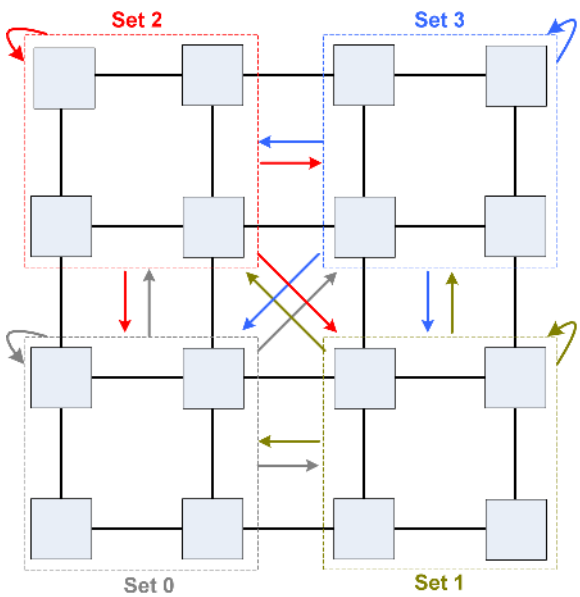

Fig. 7. A 64-core iWISE architecture showing the wireless communication between four sets (each set has four cluster and each cluster has four cores).

receiver antennas at each micro wireless router and offers scalable performance in terms of latency and connectivity. Fig. 6 illustrates a WCube structure. This design reduces the observed latency by 20%–45%, and consumes power that is comparable to or less than current 2D wire line mesh design for a 1024-core system.

An inter-router wireless scalable express channel in the mm-wave frequency range for NoC (iWISE) architectures that reduces power consumption and area overhead and improves performance is proposed in [23]. In this work, the cores are arranged in a grid fashion, and each router has its own transmitter and receiver. This design reduces the hop count by distributing the transceivers at each router as opposed to a centralized hub. This hybrid network with distributed wireless hubs allows for a one-hop 64-core network and maximum of three-hops 256-core network. Fig. 7 shows a 64-core architecture of the proposed design with four sets, each set has four clusters and each cluster has four cores. This architecture is demonstrated to achieve a 2.5X performance increase and saving of 2X power for a 256-core system when compared to other competing architectures like networks with RF-Interconnect [9] and WCube [20].

B. Small-World Network Based NoCs

All the works discussed in the previous sub-section predominantly use a regular wired mesh-based NoC overlaid with wireless links. Possibilities of creating novel architectures aided by the on-chip wireless communication have been proposed in [22].

It is possible to design high-performance, robust and energy efficient multi-core chips by adopting novel architectures inspired by complex network theory in conjunction with the on-chip wireless links. Modern complex network theory [24] provides a powerful method to analyze network topologies. Between a regular, locally interconnected mesh network and a completely random Erdös–Rényi topology, there are other classes of graphs, such as small-world and scale-free graphs. Networks with the small-world property have a very short average path length, defined as the number of hops between any pair of nodes. The average path length of small-world graphs is bounded by a polynomial in $\log(N)$, where N is the number of nodes, making them particularly interesting for efficient communication with minimal resources. Using the "small-world" approach we can build a highly efficient NoC with both wired and wireless links. The neighboring cores should be connected through normal metal wires while widely separated cores will communicate through long-range, single hop wireless links. In [25], the design of fault-tolerant small-world wireless NoCs (SWNoCs) with a power-law based interconnection architecture is presented. This approach not only significantly improves NoC performance; it also makes NoCs capable of handling a high-degree of possible faults in the wireless communication channels without significant impact on performance. Another way of improving NoC performance efficiently is to design a hierarchical architecture as proposed in [22]. The whole system can be partitioned into multiple small clusters of neighboring cores called subnets. As subnets are smaller networks, intra-subnet communication has a shorter average path length than a single NoC spanning the whole system. Subnets consist of relatively fewer cores, giving increased flexibility in designing their architectures. Instead of a single NoC spanning the entire system, as is traditional, there will be subnets with varying architectures for different parts of the chip. Fig. 8 shows such a hybrid (wireless/wired) NoC architecture with heterogeneous subnets. For inter-subnet data exchange the cores within a subnet communicate to a central hub and the hubs from all subnets are connected in a second level network forming a hierarchical structure. To reduce wireless link overheads, the neighboring hubs should be connected by traditional metal wires and a few wireless links should be distributed between widely separated and/or more frequently communicating hubs. Reducing long-haul multi-hop wired communication is essential to achieve the full benefit of WiNoCs for multi-core systems. The hubs will be connected via wireless and wired links while the subnets are wired only.

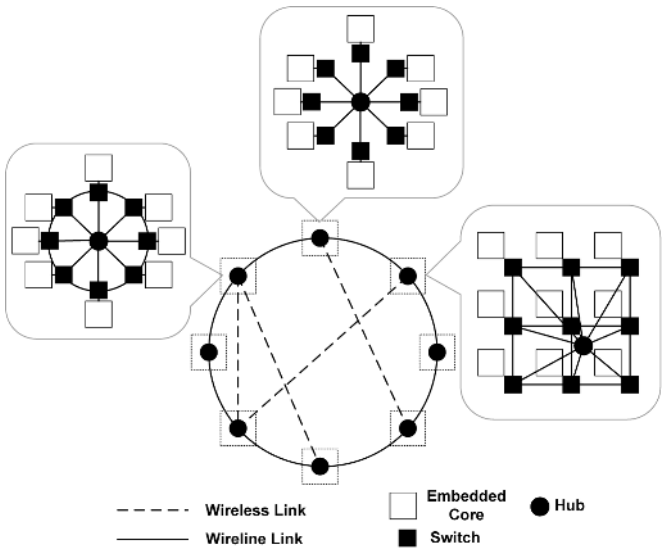

Fig. 8. Hybrid hierarchical NoC architecture with heterogeneous subnets.

The hubs with wireless links are equipped with wireless interfaces (WIs) that transmit and receive data packets over the wireless channels. Different hierarchical small-world wireless NoC architectures incorporating THz and mm-wave wireless links are explored in [22] and [14], respectively. These works have demonstrated that, by using wireless links as long-range communication channels between widely separated cores along with wired interconnects connecting adjacent cores, it is possible to obtain significant gains in achievable bandwidth and improve the energy dissipation profiles without introducing significant hardware area overhead.

IV. Comparative Performance Evaluation

In this section, we present a comparative performance evaluation of different WiNoC architectures in terms of achievable bandwidth and packet energy. Fig. 9 shows the achievable bandwidth along with packet energy for different NoCs for a 256-core system. The hierarchical NoCs were divided into 16 subnets with each subnet of size 16. In a hierarchical WiNoC, several combinations of architectures for the subnets and the upper level are possible. It is shown that an upper level mesh with overlaid wireless shortcuts in conjunction with the Star-Ring subnets provides the best performance-overhead tradeoff for mm-wave WiNoC [19]. Hence, this architecture is considered here. Performance of RF-Interconnect based small world NoC (RFNoC) [19] is also presented for comparison along with a conventional mesh. RFNoC maintains the same hierarchical topology as mm-wave WiNoC with wireless communication links replaced with RF-Is. The THz WiNoC also has the same architecture as the mm-wave WiNoC with THz wireless links used as the shortcuts. THz WiNoC and RFNoC architectures can achieve higher bandwidth compared to mm-wave WiNoC because multiple shortcuts can work simultaneously in them, whereas in mm-wave WiNoC (where the wireless channel is a shared medium) only one pair can communicate at a particular instant of time. Though THz WiNoC shows better performance than mm-wave WiNoC, it is not a CMOS compatible solution

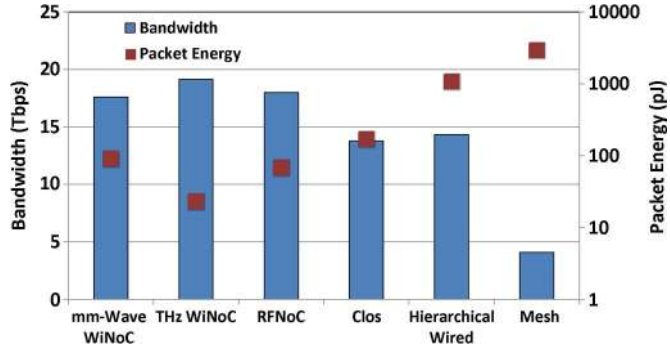

Fig. 9. Achievable bandwidth and packet energy for different NoCs.

and the integration and reliability of CNT devices need more investigation. Similarly, the total long-range link area overhead and the layout challenges of the RFNoC are more significant compared to mm-wave WiNoC.

We also present a comparative performance analysis between the WiNoCs and a few wired NoC architectures for a system size of 256 cores. We have considered three possible wired NoC architectures, viz., Clos, a hierarchical architecture and a flat mesh NoC. Clos represents a high-radix topology. It is implemented using three router stages with 16 routers per stage and radix 16 routers. The hierarchical wired NoC has the same topology as the WiNoC, without the shortcuts. All the long range wires used in these NoCs are considered as buffered wires. The mesh NoC switches have three pipeline stages and two virtual channels per port. From Fig. 9 it can be observed that Clos and hierarchical wired NoC perform considerably better than flat mesh, but the small-world based wireless/RF-I NoCs can sustain higher bandwidth compared to all the wired NoCs because of their better connectivity and efficient shortcuts.

Along with achievable bandwidth, we also present the packet energy dissipation, E_{pkt} [22] to quantify the energy dissipation characteristics of the different NoC architectures. For hierarchical NoCs packet energy is calculated as

$$E_{\mathrm{pkt}} = \frac{N_{\mathrm{intrasubnet}} E_{\mathrm{subnet,hop}} h_{\mathrm{subnet}} + N_{\mathrm{intersubnet}} E_{\mathrm{upper,hop}} h_{\mathrm{upper}}}{N_{\mathrm{intrasubnet}} + N_{\mathrm{intersubnet}}} \tag{1}$$

where $N_{\mathrm{intrasubnet}}$ and $N_{\mathrm{intersubnet}}$ are the total number of packets routed within the subnet and between the subnets in the second level of the hierarchy, respectively, $E_{\mathrm{subnet,hop}}$ is the energy dissipated by a packet traversing a single hop on the wired subnet, and $E_{\mathrm{upper,hop}}$ is the energy dissipated by a packet traversing a single hop on the second level of the hierarchical network. For the subnets, the sources of energy dissipation are the router blocks and the inter-router wires. The $E_{\mathrm{upper,hop}}$ takes into account relevant wireless/RF interconnect energy dissipation (including the transceivers) for the WiNoC and RFNoC. The average number of hops per packet in the subnet and the upper level network are denoted by h_{subnet} and h_{upper}, respectively. For nonhierarchical NoCs, the packet energy is calculated as

$$E_{\mathrm{pkt}} = E_{\mathrm{pkt,hop}} * h_{\mathrm{pkt}}, \tag{2}$$

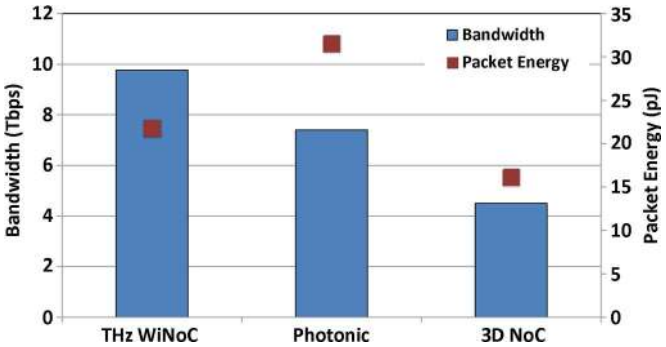

Fig. 10. Packet energy dissipation and achievable NoC bandwidth for various types of emerging NoC paradigms for system size of 128 cores.

where $E_{\mathrm{pkt,hop}}$ is the average energy dissipated by a packet traversing a single hop. It consists of energy dissipated by the routers and the inter-router wired links. The average number of hops per packet in the network is denoted by h_{pkt}. It can be observed from Fig. 9 that the wireless/RF-I based small-world NoCs perform significantly better than all the wired alternatives. This is because as discussed in Section II-B, mm-wave wireless shortcuts are always energy efficient compared to a wired link whenever the link length is 7 mm or more. In the small-world mm-wave WiNoC architecture, the minimum and maximum distances between the WIs communicating using the wireless channel are 7.07 and 18 mm, respectively [19]. Therefore, in the mm-wave WiNoC, using the wireless channel is always more energy efficient. A similar result holds for the THz WiNoC and RFNoC as well.

These small-world WiNoC architectures with energy efficient long range links reduce the average hop count, and hence the latency between the cores. Packets get routed faster and hence occupy resources for less time and dissipate significantly less energy compared to a traditional mesh-based NoC. THz WiNoC is most energy efficient among the NoCs compared here as it has the most efficient wireless links followed by RFNoC and mm-wave WiNoC. By increasing the number of non-overlapping channels, the performance of the mm-wave WiNoC can be improved further. These hierarchical and small-world WiNoC architectures are shown to perform orders of magnitude better than their traditional counterparts.

Among WiNoC architectures the THz WiNoC offers highest bandwidth with least packet energy dissipation. We also present a sample comparative performance evaluation of the THz WiNoC with other emerging NoC paradigms like photonic and 3-D NoCs in Fig. 10 under a uniform random traffic scenario. A system with 128 cores and packet size of 64 flits is considered as in [22]. We map this to a 3-D mesh-based NoC with four layers as in [26]. The photonic NoC architecture is adopted from [6].

It can be observed that among all the emerging NoC architectures, the hybrid THz WiNoC has the lowest packet energy and the highest peak bandwidth. This is because in the THz WiNoC each of the 24 wireless channels can sustain a data rate of 10 Gb/s. THz WiNoC reduces the average hop count compared to the 3-D NoC. The photonic NoC considered in the comparative evaluation requires an electrical control network to configure photonic switching elements which uses a flat wireline mesh NoC. This causes overheads and hence limits its performance. However, an alternative photonic NoC architecture, Corona, demonstrated in [7] employs an optical network amalgamated onto a 3-D chip. This particular architecture achieves a higher bandwidth than the WiNoC [22] as it takes advantage of both photonic links and 3-D integration simultaneously.

V. Communication Resource Management

To attain the desired performance benefits using WiNoC, the available communication resources should be utilized optimally. Efficient media access mechanism along with optimum routing protocol is crucial for efficient utilization of the wireless channels. In this section, we discuss about the different media access control (MAC) mechanisms and routing protocols used for WiNoCs so far.

A. Media Access Control

In WiNoCs incorporation of a suitable MAC mechanism is very important to sustain an acceptable performance level. The adopted MAC has to be simple and lightweight. It should not introduce undue area and power overheads. Implementation of the MAC protocol also depends on the characteristics of the physical layer.

In [27], a MAC protocol is proposed for wireless NoCs with short-range UWB transceivers. As the wireless communication range is very short it is possible to divide the whole NoC into physically separated zones with minimal interference from wireless signals in other zones. Within a particular zone, access to the wireless medium is granted based on a centralized arbitration policy. As ultra-short pulses can be used with the UWB technology, the authors in [12] propose time-hopping multiple access to improve the performance of the NoC. In this scheme a transmitting RF node uses pseudorandom timing of its pulses within the UWB signal interval, which is unique for each receiver. This enables concurrent multiple channels between multiple transceiver pairs. Even at the largest network size the area cost for the MAC unit synthesized in 0.18 μm technology is about 0.15% of a 1 cm^2 chip area [12].

For mm-wave WiNoCs, due to omni-directional antennas the wireless medium is shared between multiple wireless nodes, so the performance of the NoC will improve if all the nodes can access the medium simultaneously and adaptively based on the particular application. Due to limitations in the available bandwidth and complexity of transceiver designs, multiple nonoverlapping channels at high operating frequencies is a non-scalable solution. In [14] and [19], a token flow control based MAC protocol is implemented. In this scheme, the particular wireless node possessing the token can broadcast flits into the wireless medium. All other hubs will receive the flit as their antennas are tuned to the same frequency band. When the destination address matches the address of the receiving hub then the flit is accepted for further routing. It is routed either to a core in the subnet of that hub or to an adjacent hub. The token is released to the next wireless node after all flits belonging to a single packet at the current token-holding hub are transmitted. But the token passing protocol does not scale well with

increasing number of wireless nodes. Specifically, the token return period increases with the number of wireless nodes. Hence, the delay in acquiring the wireless medium for a node also increases. Using multiple access mechanisms such as code division multiple access (CDMA) the number of simultaneous accesses can be increased. Consequently, this will improve the performance of WiNoCs with mm-wave wireless links significantly. In [28] the authors use a Walsh code of eight CDMA chips per bit, which enables seven simultaneous transmissions using the wireless medium. The associated area overhead per wireless switch is 0.003 mm^2.

In [20], a frequency division multiple access (FDMA) based wireless MAC is used in sub terahertz WiNoC design. It uses different frequency channels to deliver a packet at each wireless router. This FDMA-based MAC effectively offers a dedicated link for each transmission.

The wireless NoC proposed in [29] also uses a FDMA-based MAC to achieve simultaneous multiple communication between wireless routers. Each wireless transmitter and receiver pair uses an independent carrier frequency to accommodate data from different channels.

Using CNT antennas it is possible to create simple combined frequency division multiplexing and time division multiplexing channelization schemes. By using multiband laser sources to excite CNT antennas, different frequency channels can be assigned to pairs of communicating nodes. This requires antenna elements tuned to different frequencies for each pair, thus creating a form of frequency division multiplexing (FDM) allocating dedicated channels between a source and destination pair. This is possible by using CNTs of different lengths, which are multiples of the wavelengths of the respective carrier frequencies. In [22], 24 continuous wave laser sources of different frequencies [21] are used. These 24 frequencies can be assigned to multiple wireless links in the WiNoC so that a single frequency channel is used only once to avoid signal interference. The number of distinct channels can be increased by adopting simple time division multiplexing (TDM) techniques on top of the FDM scheme.

B. Routing Protocol

To sustain the predicted WiNoC performance a deadlock free routing algorithm must be designed. The routing protocol also needs to be simple without incurring too much power, area and latency overheads.

In the UWB-based WiNoC deadlock is avoided through restricted-turn oriented location-based routing (LBR) [12]. The algorithm developed in this work ensures distributed, cycle-free, shortest-path, and deterministic routing. Its distributed logic-based routing results in low-latency, low-power and low-area overhead communication along with restricted-turn routing, which guarantees deadlock freedom.

For a small-world based WiNoC, introduction of the wireless shortcuts imposes restrictions on the adopted routing algorithm to achieve deadlock freedom. If the overall network is a mesh with wireless shortcuts then a combination of XY routing for the hubs without wireless shortcuts and south–rast routing algorithm for the hubs with wireless shortcuts can be adopted as this routing algorithm is shown to be deadlock free in [30]. In case of the irregular WiNoC architectures achieving deadlock freedom is more complicated. One way to make the routing deadlock free is to follow the tree-based routing architecture for irregular networks (TRAIN) algorithm [31], in which data is routed along a minimum spanning tree (MST) of the network. An allowed route never uses a link in the up direction after it has been in the down path. Hence, channel dependency cycles are prohibited and deadlock freedom is achieved. Links not in the MST are used for packet transmission only if they provide a shorter path to the destination than the MST route. These links are the shortcuts and the wireless channels should be used as the shortcuts in this routing algorithm. Hence, by combining the TRAIN algorithm with wireless shortcuts deadlock can be avoided in an irregular WiNoC.

For the sub terahertz wireless NoC design of [20], a deadlock free static routing table based mechanism along with XY routing for baseline mesh is used.

An adaptive minimal routing algorithm is used in [29], which takes buffer utilization into account while deciding routing paths. The algorithm uses buffer utilization information from wireless routers (WRs) to avoid traffic build up when there is congestion at WRs.

A centralized routing where the complete path from source to destination is predetermined at the source is used in the THz WiNoC [22].

The MAC and routing protocols for WiNoCs need to be complemented by suitable flow control mechanisms to enable optimum utilization of the wireless medium. Among all the WiNoC architectures, only the mm-wave WiNoC has incorporated a suitable flow control mechanism [19], [32]. Between a pair of source and destination hubs without WIs, the routing path involving a wireless link should be chosen if it reduces the total path length compared to the wired path. This can potentially give rise to a hotspot situation in the WIs because many messages try to access wireless shortcuts simultaneously, thus overloading the WIs and resulting in higher latency. Token flow control proposed in [33] and distributed routing can be used to alleviate this problem. Tokens are used to communicate the status of the input buffers of a particular WI to other nearby hubs, which need to use that WI for accessing wireless shortcuts. Every WI input port has a token and the token is turned on if the availability of the port's buffer is greater than a fixed threshold and turned off otherwise. Consequently, the distributed routing and token flow control effectively improves performance by distributing traffic though alternative paths.

All these proposed MAC and routing methods help to improve the achievable performance of the WiNoCs, but incur area and power overheads. A comprehensive study quantifying merits and limitations of these techniques and their implementation challenges needs to be carried out for an informative comparative analysis.

VI. Reliability

The on-chip wireless communication link is an emerging technology and it is in a formative stage. Challenges in reliability and integration demand radically different architectural design to make this emerging interconnect paradigm viable for large-scale adoption. Architecture adopted from natural

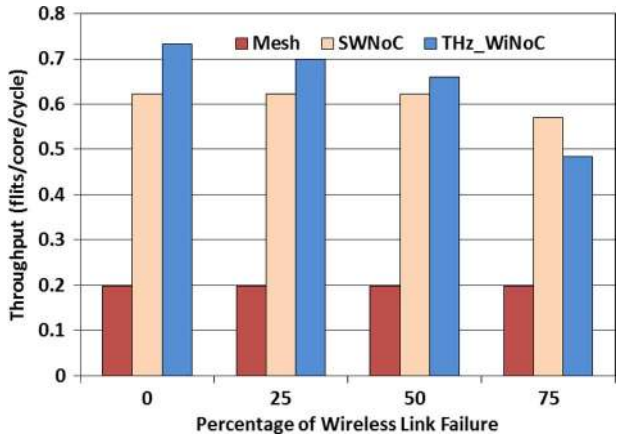

Fig. 11. Saturation throughput of mesh, SWNoC and THz WiNoC for a 256-core system.

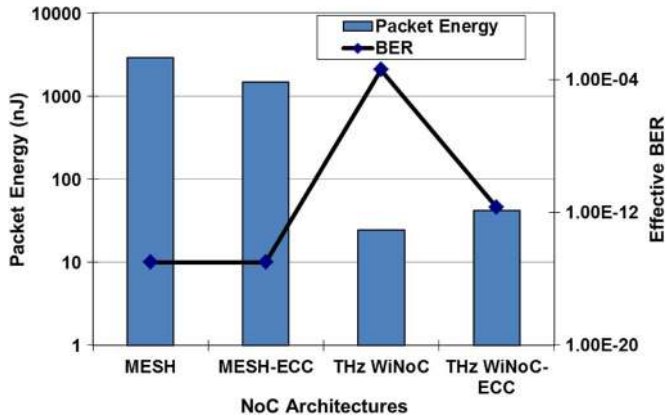

Fig. 12. Packet energy dissipation and worst case channel BER for THz WiNoC and mesh architectures with and without ECC.

complex networks is a promising alternative in this perspective [34].

A few highly connected nodes and many peripheral nodes with very few connections characterize networks having a connectivity structure known as scale-free graphs. Under these conditions random faults result mostly in failure of those nodes with very few connections as they occur in large majority. However, failure of these nodes only marginally affects the entire network due to their relatively few connections. On the other hand these networks are very vulnerable to preferential failures of the important nodes which are highly connected. In contrast, small-world graphs are characterized by near equal connectivity of all nodes. These networks consequently perform similarly in response to random as well as preferential failures. Hence, depending on the failure patterns of this emerging interconnect technology, network architectures inspired from complex network theory can be designed to provide inherent reliability against such faults. One of the first attempts to design a complex network-inspired reliable WiNoC is made in [25]. It is shown that a small-world based WiNoC architecture (SWNoC) performs better than their conventional wired counterparts even in the presence of a high number of faults in the wireless links. Fig. 11 shows the variation in throughput for 256-core mesh, SWNoC and hierarchical THz WiNoC (with 16 subnets each of size 16) in presence of same degree of wireless link failure in uniform random traffic scenario. The hierarchical THz WiNoC is considered to have a ring upper level with overlaid wireless shortcuts and the cores in the subnets are connected in a mesh topology as in [22]. The wireless link failures do not impact the performance of the flat wireline mesh architecture. Hence, its performance remains unchanged. It is interesting to note that the performance of the THz WiNoC degrades comparatively more rapidly than that of the SWNoC with increasing degree of failure. The THz WiNoC has higher throughput than the wireless SWNoC in the failure-free case due to the hierarchical structure, however it has poorer resilience to failure of the wireless links. This is because the THz WiNoC does not have a perfect small-world topology and that results in increase of average distance between cores with failure of wireless links. Whereas in case of SWNoC, the rise in average hop count with failure is insignificant [25]. Consequently, the performance degradation is minimal.

Although these architectural innovations enable resilience against permanent failures, the wireless channels are inherently more prone to transient errors than their wireline counterparts. It is demonstrated in [35] that with carefully designed error control coding (ECC) schemes in the WiNoC it is possible to achieve high gains in performance due to the wireless links while maintaining reliability comparable to that of a traditional wire line NoC. This work shows that, by implementing joint crosstalk avoidance triple error correction and simultaneous quadruple error detection (JTEC-SQED) codes [36] in the wire line links and Hamming code based product codes (H-PCs) in the wireless links of a hierarchical wireless NoC with CNT antennas [35] it is possible to improve the overall reliability of the wireless NoC manifold. Fig. 12 shows the energy dissipated in delivering a packet from source to destination on average and the bit error rate (BER) of the most unreliable link in the entire hierarchical THz WiNoC (ring upper level with subnet cores connected as mesh) with 256 cores divided into 16 subnets. It can be seen that applying the JTEC-SQED code on the wireline mesh NoC reduces its packet energy, as the interconnects could tolerate lower noise margins and hence lower rail voltages [36]. Although the THz WiNoC reduces the packet energy by orders of magnitude the worst case BER is poor due to the wireless links. H-PC can achieve simultaneous random and burst-error correction on the wireless links, and by employing this code it is possible to improve the worst case BER for the wireless links.

Application of ECC also introduces timing and area overhead. The timing overhead is reflected in the form of increased packet latency for the NoC. So for optimum performance, a trade-off point should be obtained where the performance improvement caused by introduction of ECC will outweigh the associated overheads. Fig. 13 presents the overall latency characteristics of the WiNoC and the wireline mesh with and without coding [35] for a 256-core system. Due to the low code rate of the H-PC as well as codec overheads the overall latency of the WiNoC with coding is higher than that of the WiNoC without

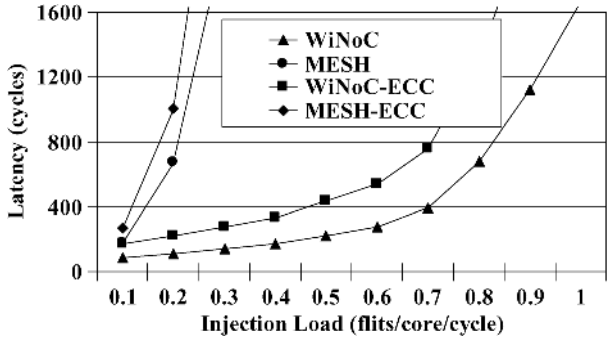

Fig. 13. Latency characteristics of mesh and WiNoC architectures with and without ECC.

TABLE II
COMPARISON OF THE THREE EMERGING INTERCONNECT PARADIGMS

		3D Integration	Optical Interconnects	Wireless Links
Design Requirements		Multiple layers with active devices	Silicon photonic components	On-chip metal or CNT-based antennas
Performance Gains	Bandwidth Advantage	Higher connectivity & less hop count	High speed optical devices and links	Single hop high bandwidth wireless links
	Lower Power Dissipation	Shorter average path length	Negligible power dissipation in optical data transport	Multi-hop paths replaced by single hop links
Reliability Issues		Vertical Via Failure	Temperature sensitivity of photonic components	Noisy wireless channels
Challenges		Heat dissipation due to higher power density, yield	Integration of on-chip photonic components	Low power mm-wave transceivers & Control over CNT growth

coding. However, even with coding the latency at network saturation of the WiNoC is much less compared to that of a wireline mesh NoC without any coding.

VII. CONCLUDING REMARKS

Communication plays a crucial role in the design and performance of multi-core SoCs. NoCs have been proposed as a promising solution to simplify and optimize SoC design. However, it is expected that improving traditional communication technologies and interconnect organizations will not be sufficient to satisfy the demand for energy-efficient and high performance interconnect fabrics, which continues to grow with each new process generation. Among several emerging possibilities, wireless NoC is a promising option. In this paper we have presented various design possibilities and challenges for WiNoC architectures as communication backbones for multi-core chips. We have highlighted several issues, including overall architecture, physical layer design, MAC protocols, routing and reliability. The WiNoC paradigm is still in its initial stages. It needs extensive investigations to make it a viable alternative to existing interconnect infrastructures. Also, it should be noted that on-chip wireless communication is not the only emerging paradigm alternative to traditional planar metal/dielectric-based interconnects for building the communication infrastructure of future multi-core SoCs. Three-dimensional integration and nanophotonic communication are other alternatives. Each of these emerging interconnect paradigms, whose main features are summarized in Table II, could offer remarkable advantages [37]. However, in order to harvest their potential more research is necessary to address various challenges in multiple areas including system architecture, circuit design, device fabrication and CAD tool development. Moreover, the achievable performance benefits of WiNoCs need to be benchmarked and relevant design trade-offs need to be established with respect to other alternative emerging paradigms.

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Sujay Deb received the B.Tech. degree in electronics and communication engineering from North Eastern Regional Institute of Science and Technology, Arunachal Pradesh, India, in 2004, the M.S. degree in telecommunication engineering from the Indian Institute of Technology, Kharagpur, India, in 2007, and the Ph.D. degree in electrical and computer engineering from the Washington State University, Pullman, in 2012.

His broader research interest is design of novel interconnect architectures for multi-core chips. Specifically, it comprises analysis of network-on-chip communication fabrics in presence of long range millimeter-wave wireless links.

Dr. Deb received the "Outstanding Ph.D. student award in Computer Engineering" at Washington State University for his contributions in research.

Amlan Ganguly (M'11) received the B.S. degree from Indian Institute of Technology, Kharagpur, India, and the M.S. and Ph.D. degrees from Washington State University, Pullman.

He is an Assistant Professor in the Department of Computer Engineering at Rochester Institute of Technology, Rochester, NY, since 2010. His research interests are in fault-tolerant and secure architectures for massive multi-core chips and emerging interconnect technologies for on-chip networks. He has worked at Intel India Development Center, India, and the Pacific Northwest National Laboratories, Richland, WA.

Partha Pratim Pande (SM'11) received the M.S. degree in computer science from the National University of Singapore and the Ph.D. degree in electrical and computer engineering from the University of British Columbia, Vancouver, BC, Canada.

He is an Associate Professor at the School of Electrical Engineering and Computer Science, Washington State University, Pullman. His current research interests are novel interconnect architectures for multicore chips, on-chip wireless communication networks, and hardware accelerators for biocomputing. He has around 50 publications on this topic in reputed journals and conferences. He is the Guest Editor of a special issue on sustainable and green computing systems for ACM *Journal on Emerging Technologies in Computing Systems*.

Dr. Pande currently serves on the Editorial Board of IEEE Design and Test of Computers and Sustainable Computing: Informatics and Systems (SUSCOM). He also serves in the program committee of many reputed international conferences.

Benjamin Belzer (S'93–M'96) received the B.A. degree in physics from the University of California-San Diego, La Jolla, in 1982, and the Ph.D. degree in electrical engineering from the University of California-Los Angeles, in 1996.

From 1981 to 1991, he worked as a Software Engineer for Beckman Instruments, Hughes Aircraft, Northrop Corporation, Source Scientific, and Develco, Inc. Since 1996 he has been with the School of Electrical Engineering and Computer Science at Washington State University, Pullman, where he is currently an Associate Professor. His research interests include iterative detection and equalization, coding for networks-on-chip, coded modulation for wireless communications, and combined source and channel coding.

Deukhyoun Heo received the B.S.E.E. degree in electrical engineering from Kyoungpuk National University, Daegu, South Korea, in 1989, the M.S.E.E. degree in electrical engineering from the Pohang University of Science and Technology (POSTECH), Pohang, South Korea, in 1997, and the Ph.D. degree in electrical and computer engineering from the Georgia Institute of Technology, Atlanta, in 2000.

In 2000, he joined the National Semiconductor Corporation, where he was a Senior Design Engineer involved in the development of silicon RFICs for cellular applications. He is an Associate Professor in the Electrical Engineering and Computer Science Department at Washington State University, Pullman. He has primarily been interested in RF/microwave/opto transceiver design based on CMOS, SiGe BiCMOS, and GaAs technologies for wireless and wireline data communica-

tions, battery-less wireless sensors and intelligent power management system for sustainable energy sources, adaptive beam former for phased array communications, low-power high-data rate wireless link for biomedical applications, and wireless network on chip solution. He has around 100 publications, including 30 peer-reviewed journal papers, and 70 international conference papers.

Dr. Heo was the recipient of the 2000 Best Student Paper Award presented at the IEEE International Microwave Symposium (IMS). He is the recipient of National Science Foundation (NSF) CAREER award in 2009. He has been a member of Technical Program Committee of IMS and International Symposium of Circuit and Systems (ISCAS) and has served as an Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II: EXPRESS BRIEFS from 2007 to 2009 and IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES since 2010.