Word Line Pulsing Technique for Stability Fault Detection in SRAM Cells

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Abstract

Stability testing of SRAMs has been time consuming. This paper presents a new programmable DFT technique for detection of stability and data retention faults in SRAM cells. The proposed technique offers extended flexibility in setting the weak overwrite test stress, which allows to track process changes without time-consuming post-silicon design iterations. Moreover, it does not introduce extra circuitry in the SRAM array and surpasses the Data Retention Test in test time and detection capability.

1 Introduction and Motivation

The stability of embedded SRAMs is a growing concern in the design and test community. Maintaining an acceptable Static Noise Margin (SNM) of embedded SRAMs while scaling the minimal feature sizes and supply voltages of the Systems on a Chip (SoC) becomes increasingly challenging. Increased process spreads of modern scaled-down technologies and non-catastrophic defect related sensitivity to environmental parameters cause stability degradation in SRAMs [1]. Moreover, minimal feature sizes of SRAM cell transistors combined with high packing density of SRAM arrays often involving relaxed design rules aggravate this problem. SNM can serve as a figure of merit in evaluation of the stability of SRAM cells. Due to the factors, which are discussed in the following sections, SNM even in defect-free cells is declining with scaling. In the presence of non-catastrophic defects such as resistive vias and contacts, cell stability is degraded even further. Such defective cells however, can escape the standard functional memory tests.

ITRS-2003 [2] predicts "greater parametric yield loss with respect to noise margins" for high density circuits such as SRAM arrays, which are projected to occupy more than 90% of the SoC area in less than ten years. In more severe cases, poor noise margin caused by weak opens in the cell can lead to a Data Retention Fault (DRF). Detection of DRFs and Stability Faults (SFs) has been a time consuming and expensive effort. In this paper, we refer to the cells causing such faults as to *weak cells*. Traditional Data Retention (a.k.a. Delay or Pause) Test (DRT) has a limited defect resistance coverage with respect to the weak cell detection, is time consuming and may require elevated temperatures to improve its detection capability. Moreover, DRT can be ineffective in detecting most of the SFs. If undetected, the SFs can manifest themselves under the adverse circumstances not covered in the production test and may lead to the field failures. Since the SFs are often caused by manufacturing defects, they can also indicate potential long-term reliability issues.

Detection of SFs in SRAM cells requires sensitizing such cells by applying a test stress. The test stress should on one hand be sufficient to flip the unstable cells and on the other hand insufficient to flip the healthy cells. A number of weak cell detection DFT techniques utilizing weak disturbs have been proposed in the field. However, most of these techniques lack flexibility in setting the detection threshold, which is defined by the degree of stress applied to the cell during the test. In this paper we propose a new defect-oriented DFT technique for Stability Fault detection. The proposed technique offers easily changeable degree of test stress applied to the Cell Under Test (CUT), does not require any additional circuitry in SRAM array and can be easily incorporated into the memory structure.

The rest of the paper is organized as follows: Section 2 defines stability faults and the factors influencing SRAM cell stability. In Section 3 we introduce a classification of SRAM stability test methods and discuss their implementation challenges. In Section 4 we describe the proposed programmable test technique for weak cell detection and its possible implementation variations. Section 5 demonstrates the detection capabilities of the proposed DFT. Section 6 presents a summary of the main contributions of this work.

2 SRAM Stability Faults

A typical six-transistor (6T) SRAM cell that we will be referring to in this paper is presented in Figure 1(a), where $Q1$ and $Q2$ – driver, $Q3$ and $Q4$ – load, and $Q5$ and $Q6$ – access transistors respectively. In terms of the cell stability, the worst case is observed when a cell is read-accessed [3]
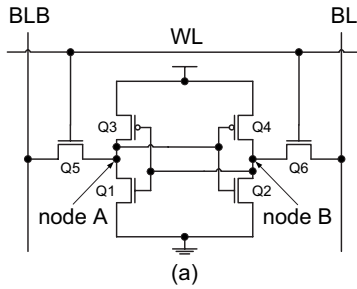
Figure 1   A Six-transistor SRAM cell (a) and its equivalent circuit in read-access (b)

as shown in its equivalent circuit in Figure 1(b). Suppose that the right internal cell node (node B) carries a "zero". When the cell is read-accessed, $Q4$ is off and the saturated access transistor $Q6$ effectively takes its place. The current of the driver transistor $Q2$ now has to contend with the saturation current of $Q6$, which degrades the level of logic "zero" stored in the node as shown in Figure 2.
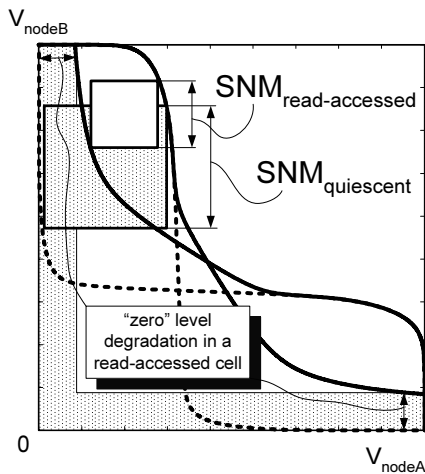

Figure 2   Simulated VTCs of a 6T SRAM cell (CMOS 0.18μm) in the quiescent and the read-accessed modes.

Figure 2 presents simulated Voltage Transfer Characteristics (VTCs) of a quiescent and a read-accessed cell. The "zero" level stored in node B of a read-accessed cell becomes degraded, causing an almost two-fold reduction of the SNM, which is defined as a side of the *smaller* of the two biggest squares between the VTCs of the cell [3]. The degree of the SNM degradation is inversely proportional to the cell ratio $r = (W/L)_{driver}/(W/L)_{access}$. The cell ratio r is typically set from 1.5 to 3 and represents a tradeoff between the read current I_{read} (speed) and stability on one hand and the cell area on the other. Since the read-accessed mode represents the worst-case SNM of the cell, in this paper we will assume this mode.

In the near future SRAM designers will have to cope with the decreasing SNM of the cell as shown in Figure 3. VTCs for 90nm and 65nm technology nodes have been obtained using Berkeley Predictive Technology Model (BPTM) [4] and may give overly optimistic SNM values. SNM of only
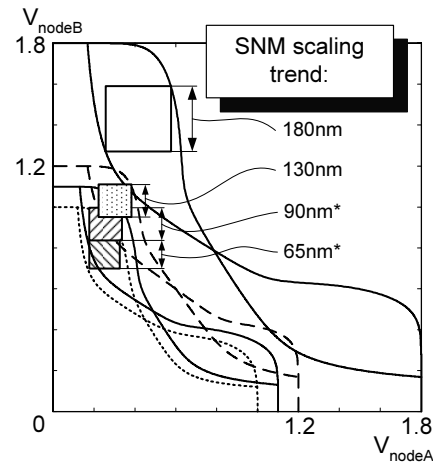

Figure 3   Simulated SNM trends for CMOS 180nm, 130nm, 90nm* and 60nm* technologies (*simulated using BPTM [4]).

95mV has been reported for 65nm technology [5], which is over four times less than for 180nm technology, while the supply voltage has been scaled down less than twice. With relatively high supply voltage and increasingly tall interconnect aspect ratios, the coupling and substrate noise effects will require serious attention. Combined with the increasing process spread and defect density, these factors will make the cell stability one of the major concerns in SRAM design.
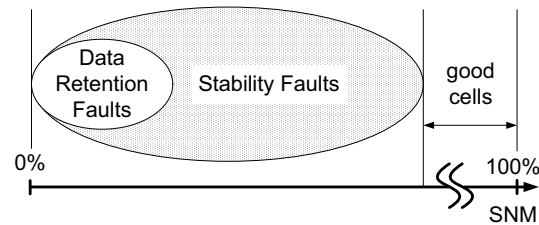

Figure 4   Relationship between the SNM, Data Retention and Stability Faults in SRAM cell.

Depending on the severity of the SNM degradation, the stability problems in SRAM cells can be classified into the Data Retention Faults and the Stability Faults with the former being a subset of the latter, as shown in Figure 4. A cell with extremely low values of the SNM the cell is likely to flip its state if not rewritten with the same data again shortly after, i.e. it fails to retain its data demonstrating a DRF. If the SNM is sufficient to handle the driver NMOS off-state leakage current that discharges the node storing a "1", under normal conditions it can retain its data as long as the power is supplied to the cell. However, under the adverse conditions such as the reduced supply voltage, elevated temperature, increased coupling noise, multiple read accesses etc., i.e. the conditions contributing to the further SNM degradation, the same cell may become unstable and flip its state exhibiting an SF. And finally, the cells with the SNM high enough to withstand the worst possible case scenario deemed to be free from the SFs and are outside of the
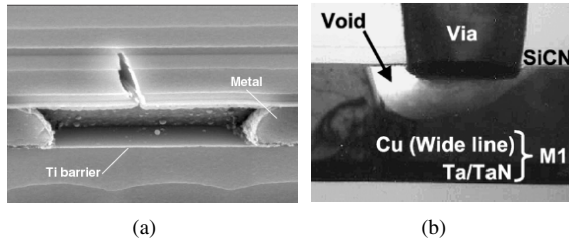
Figure 5 Weak open defects: (a) detailed cross-section of a metal open line, showing the metal cavity and formation of a weak open defect due to the Ti barrier [6]; and (b) an open via [7].
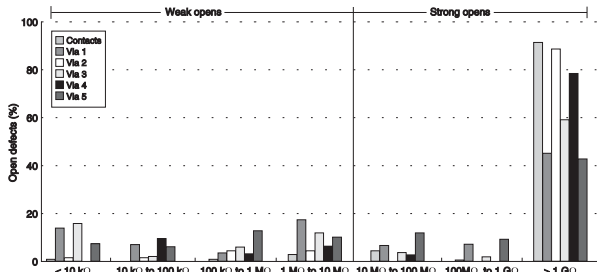

Figure 6 Resistance distribution for contact and via opens [6].

Figure 7 Layout of a 6T SRAM cell, where resistances of contacts 1, 2 and 3 correspond to respectively R1, R2 and R3 shown in Figure 8.

Figure 8 SRAM cell schematic with resistors in place of potential weak opens that can cause stability faults as per layout in Figure 7.

oval representing the SFs in Figure 4. We will refer to the cells inside and outside of the patterned oval representing SFs as *weak* and *good* respectively.

2.1 Resistive Opens

The typical CMOS process involves numerous contacts to diffusion areas and vias between metal layers. With technology nodes scaling down to the decananometer region, the operation speed of LSI circuits tends to be limited by the interconnects. Providing reliable contacts and vias is a growing challenge [6, 7], especially in high-density SRAM arrays. Poorly formed contacts and vias can cause delay faults if located in the timing or signal propagation paths. When located in the pull-up path of an SRAM cell, such defects can cause a DRF or a SF depending on their severity and can escape the traditional functional memory tests.

Figure 5 illustrates weak open defects in metal and via formation. Difficult-to-detect weak opens with $R_{open} < 10M\Omega$ constitute a significant part of the total number of opens, as is suggested by Figure 6. Weak opens are likely to be equally distributed across the entire range from $10k\Omega$ to $10M\Omega$ showing relatively high and flat probability of a weak open with any resistance value [6].

SRAM arrays are the densest form of circuitry and can occupy a significant silicon area. Each cell contains from ten contacts as in the cell used in this work (Figure 7) to fourteen in the latest technologies [8]. These contacts are the potential locations of weak opens. A weak open in contact "1" in Figure 7 represents a symmetric defect when both sources of the load PMOS transistors $Q3$ and $Q4$ are connected to the power supply through a resistor $R1$ (Fig-
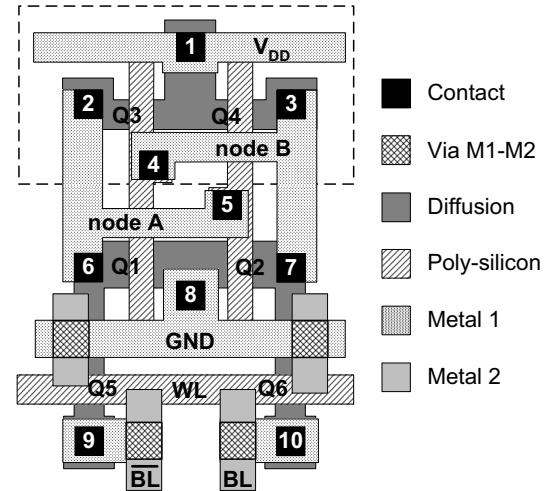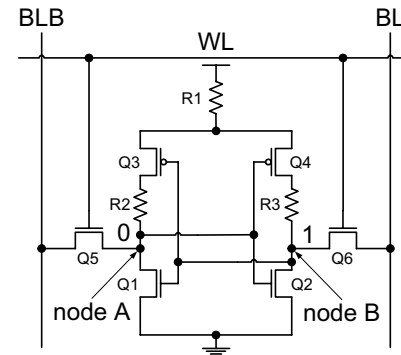
ure 8). Infinite value of $R1$ corresponds to a strong open in the cell's supply connection or a situation when both PMOS transistors are missing. Open in contact "2" or "3" on the left-hand and right-hand sides of the cell respectively corresponds to a resistive connection of $Q3$ or $Q4$ drains to nodes A or B respectively (Figure 8) and represents an asymmetric defect [9]. As the technology is moving towards the smaller feature sizes, the "split word line" cell layouts have been adopted by the foundries [5, 8]. They have separate source contacts for each of the load PMOS devices thus increasing the total number of possible locations of open contacts which can cause DRFs or SFs to four.

Our research shows that the presence of weak opens (breaks) in an SRAM cell can cause degradation of its static noise margin (SNM). The simulation results showing the SNM values as a function of the resistive opens introduced in an SRAM cell are presented in Figure 9. As mentioned before, resistive open defects are likely to appear in place of poor or absent contacts, vias or silicide [9, 10]. Cell stability is the most sensitive to weak opens in driver tran-
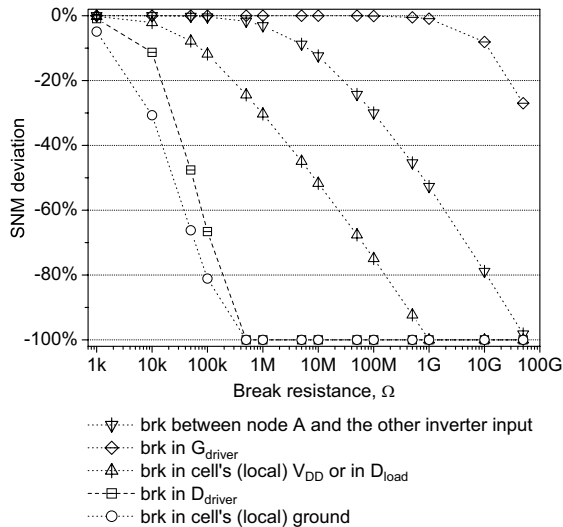
Figure 9   SRAM cell SNM as a function of resistive opens (simulation results for CMOS 0.13μm technology) [1].

sistor drains (D_{driver}), the power supply lines and drains of the load transistors (D_{load}). Whereas resistive opens in transistor gates do not cause a noticeable SNM degradation unless the open resistance exceeds 1 $G\Omega$, which falls into the strong open category [6]. Since resistive opens in the pull-down path of SRAM cell reduce I_{read}, the more severe cases are likely to be detected by the functional tests. Whereas, the resistive opens in the pull-up path of the cell are more difficult to detect by a functional test. Opens exceeding 100 $M\Omega$ can reveal themselves as the DRFs only at elevated temperatures after a delay on the order of 100ms. However, most of the less resistive open defects in the pull-up path will escape the functional test. Breaks in the gates of PMOS transistors may be more difficult to detect as their impact on the SNM is smaller.

2.2   Resistive Bridges

Memory cells are often laid out using very aggressive design rules [5]. Lithography and etching limitations may introduce particles of residual material or affect the quality of material removal between the densely packed and high aspect-ratio cell layout elements. All these factors contribute to the increasing probability of resistive bridges in the cell, which can degrade its stability. Figure 10 shows an abrupt and uniform SNM degradation for many kinds of bridges with resistance of less than $1M\Omega$.

2.3   Threshold Voltage Mismatch

The drive for higher bit-count of embedded memories necessitates the usage of minimal feature size transistors in SRAM cells. With the physical gate length shorter than the drawn gate length by approximately 1.45 times and extremely thin t_{ox} [2], transistor channel is becoming increasingly atomistic [11]. Random doping effects can introduce large threshold voltage mismatches even in defect-free
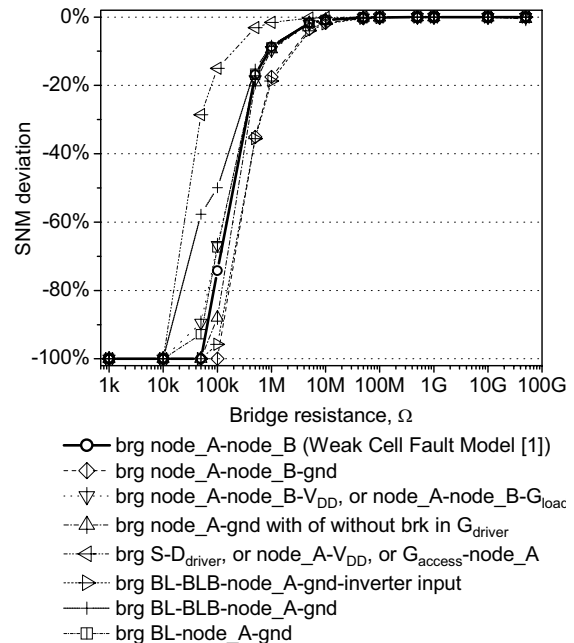

Figure 10   SRAM cell SNM as a function of resistive bridges (simulation results for CMOS 0.13μm technology) [1].

cells.

Our research shows a strong impact of V_{TH} mismatch of SRAM cell transistors on the cell's SNM and hence on its stability due to the introduced asymmetry between the transistors drive in the cell, which skews the shape of the equivalent inverters' VTCs and directly impacts the SNM of the cell. Since the worst-case SNM is measured as the size of the *smaller* square of the maximal size drawn between the "eyes" of the VTC (Figure 2), the resulting SNM value of an asymmetrical cell will decrease.

Figure 11 presents several cases of the SNM vs. V_{TH} dependencies when V_{TH} of more than one transistor in the SRAM cell is not at its typical value. For instance, $Q2_-(Q1=-25\%)$ in Figure 11 represents the dependence of the SNM on V_{TH} of $Q2$ provided that V_{TH} of $Q1$ is below its typical value by 25%. This dependence has its maximum at the point where $V_{TH\_Q1}=V_{TH\_Q2}=-25\%$ (i.e., where the cell is symmetrical). SNM vs. V_{TH} of $Q5_-(Q1=-25\%$, $Q2=+25\%$, $Q3=+40\%$, and $Q4=-40\%$) represents an example of one of the worst cases of the SNM degradation due to the multiple transistor V_{TH} mismatches.

SRAM yield is correlated with the SNM spread. It is reported that, $\mu-6\sigma$ of SNM is required to exceed $0.04\cdot V_{DD}$ to reach a 90% yield on 1MB SRAM [12]. Poor transistor matching (increased $A_{\Delta V_{TH}}$) leads to a reduction in $\mu-6\sigma$ and increases the number of unstable SRAM cells, impacting SRAM yield.

A number of factors can affect the SRAM cell stability. In extreme cases each of them can cause significant SNM degradation making the cell susceptible to stability prob-
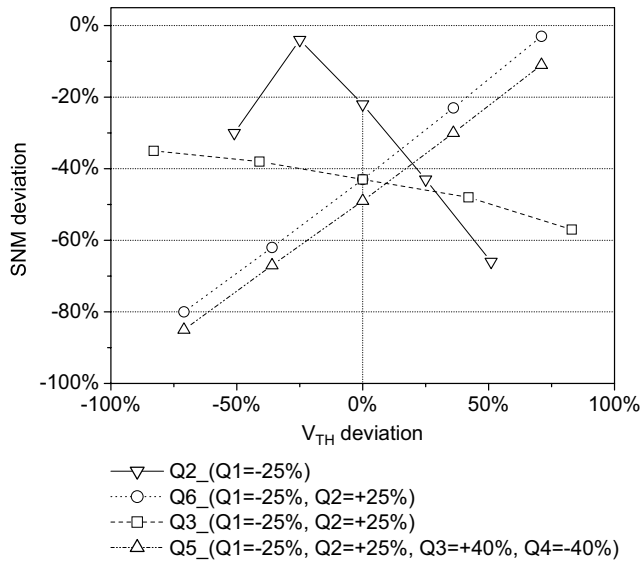
Figure 11 SRAM cell SNM vs. threshold voltage deviation (simulation results for CMOS 0.13μm technology) [1].

lems. However, a combination of even more subtle defects and mismatches found in a cell has a potential to result in a strong impact on its stability. The typical march tests used for SRAM functional test may not detect the SFs, as their detection may require stronger disturbance or stress applied to the CUT. Special detection techniques for stability fault detection have been developed to address this problem and we will try to classify them in Section 3.

3 SRAM Cell Stability Test Methods

SRAM cell stability test methods can be classified based on the utilized principle as passive (functional) and active (defect-oriented). In turn, the active methods can be divided into those offering a single test stress setting and those allowing for the programmability of the test stress.

3.1 Passive Methods

Passive functional tests commonly used by memory manufacturers include [9]: Data Retention (DRT, a.k.a. Delay and Pause), Read Disturb and the Long Write. Passive methods have limited defect resistance coverage detecting only the most severe cases. For instance, the DRT relies on the off-state leakage of the driver NMOS transistor to discharge the floating node carrying a "1" and cause the cell to change state. In normal conditions, the required pause time can be in the range of a few hundred ms. Elevated temperature helps to improve the test time of the DRT. However, the defect resistance coverage remains very limited while the test time and the test cost due to the lower tester throughput remain significant.

3.2 Active Methods

Recently, a number of methods actively stressing the CUT to determine the degree of its stability have been proposed.

3.2.1 Single Test Stress

Initially, the proposed active methods offered a single stress setting, which was defined by the best available estimates of the process conditions. One of the well-known techniques, the Weak Write Test Mode (WWTM) by Banik et al. [9], applies a weak overwrite stress to detect weak cells. Weak write circuit can be a stand-alone as in [9] or integrated into a write driver [13]. While the WWTM makes use of weaker write driver transistors, the Data Retention Weak Write Circuit described in [14] uses weaker access transistors to apply weak write stress by underdriving the access transistors using lower word line voltage during a regular write operation. Conversely, an elevated word line voltage that further degrades the stored "zero" level and thus reduces the cell's SNM can be used to apply the test stress and detect a weak cell [15]. Kuo et al. [16] suggested a Soft Defect Detection (SDD) technique based on the fact that defect-free inverters of an SRAM cell will provide certain I_{read} upon access. If there is a open in a cell's connections, the I_{read} may be insufficient or absent. Another approach proposed Kwai et al. is to separate the power supply of the memory array from that of the periphery [10]. With the corresponding isolated terminal the memory array can be operated at a lower voltage, making it susceptible to read or write disturb. However, this test alone cannot guarantee detection of all SFs and is mostly used for process development. Moreover, having a separate pad for each of the tens of memory instances in modern SoCs may be impractical. Yang et al. proposed a No Write Recovery Test Mode [17], which is capable of replacing the DRT and detecting all the open defects related to the PMOS transistor. However, this approach may have a limited defect resistance coverage range.

Many of the single detection threshold methods can be altered to enable analog control of the weak overwrite stress. However, global analog levels are more difficult to control if implemented internally or more pad- and tester-demanding if controlled at the ATE level.

3.2.2 Programmable Test Stress

The increasing process spread of modern scaled technologies necessitated the programmable test stress techniques for weak cell detection, which better track process variation or allow to adjust the pass/fail threshold during the test. Selvin et al. proposed one of the possible extensions of the WWTM using a decoder that switches the bias-setting transistors to vary the overwrite stress applied to the CUT [18]. This solution requires a dedicated bias voltage generator and the number of possible stress settings is limited by the number of the predefined bias settings.

A digitally programmable technique using the ratio of read currents of SRAM cells within a column to create a weak overwrite stress to the CUT is described in [1]. The ratio of I_{read}s is defined by the number of the cells carrying "0"s in the total number of cells (n) forming the ratio. One of the cells among the n is the CUT. After enabling of all n word lines at once, the bit lines will be partially discharged. The side with a larger number of "0"s will discharge the corresponding bit line deeper. The degree of the bit line discharge is proportional to the sum of I_{read}s of the cells discharging each bit line. If the CUT is carrying a "1" and the true bit line has been discharged deeper than the complementary, a weak overwrite stress will be applied to the CUT. A CUT with poor stability will flip its state, whereas a good CUT will withstand the test stress. By changing the number of "0"s on the same side where the CUT is carrying a "1", one can program the overwrite stress applied to the CUT. The resolution of the method can be refined by increasing of the total number of cells n comprising the I_{read} ratio and/or by changing the pulse width of the pulse enabling all n cells.

4 Proposed Programmable Detection Method

In this paper we propose a new active digitally programmable DFT technique called *Word Line Pulsing Technique* (WLPT) [19] for data retention and stability test in SRAM cells. We believe that our technique offers extended flexibility over the previous art. Similarly to other digitally programmable techniques([1] and [18]), it enables testing of memory arrays with several stress settings and selecting the stress setting that satisfies a predetermined quality versus test yield tradeoff.

4.1 Concept

Let us consider the circuit in Figure 12 representing a section of a column in an SRAM array with two identical cells. We will call the top cell the Reference Cell and the bottom cell - the Cell Under Test (CUT).

Suppose node A of the CUT carries a "0", node B carries a "1" and resistors $R1$ or $R3$ represent opens in the pull-up path of the CUT. It is well known that the strong opens in the pull-up path of an SRAM cell can cause DRFs if the pull-up current through $R1 - Q4 - R3$ (Figure 12) fails to compensate for the off-state leakage current of the driver transistor $Q2$. Given sufficient time, the leakage current of $Q2$ will discharge the capacitance of node B. Once V_{node_B} has crossed the switching threshold of the cell, the cell will flip states and can be detected by a consecutive read operation. This situation is similar to a very slow and weak overwriting of the cell. For higher values of $I_{pull-up\_path}/I_{leakage\_driver}$ ratio, the time required to discharge node B and flip the CUT can be longer than is economical for the DRT to detect such a defect. Moreover, if the pull-up current is even marginally greater than
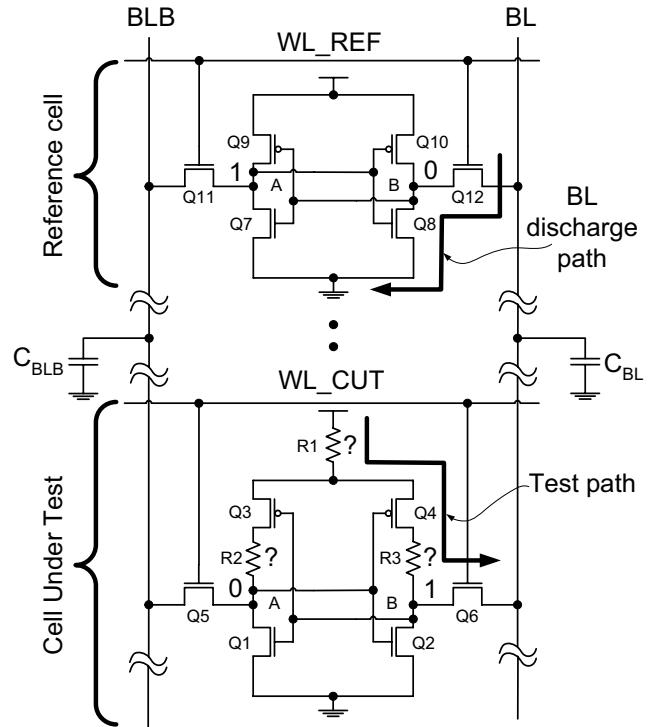

Figure 12 Reference cell and Cell Under Test (CUT). R1 represent a symmetric and R2, R3 - asymmetric defects.

the off-state leakage current of $Q2$, the cell may escape the DRT even with extended test delay periods at elevated temperature. Memories with such highly unstable cells can be shipped out and cause customer returns.

The gate voltage of $V_{G\_Q1} = V_{node\_B}$ will not change significantly unless $I_{leak\_Q2}(R1 + R3)$ is significant, i.e. at least one of the weak opens $R1$ or $R3$ qualifies for a strong open. So, node A and the gate of $Q4$ will remain at "0" and the effective pull-up current for node B of the CUT will be proportional to the equivalent resistance of the path $(R1 - Q4 - R3)$.

Suppose we have means to freely change the potential on the bit line (BL) and have set it to be $0.6V$ while the complementary bit line (BLB) remains fully precharged to the supply voltage. After enabling WL_CUT, $Q6$ will pass the reduced V_{BL} onto the node B of the CUT. Node B potential is proportional to the ratio I_{Q4}/I_{Q6}. The overwrite condition for node B is ensured if we can pull node B below the switching threshold of the inverter formed by transistors $Q1$ and $Q3$. Since the effective pull-up drive of node B is weakened by the defect resistance $(R1 + R3)$, the overwrite condition will be met earlier and the weak cell will be overwritten, whereas a good cell with $(R1 + R3) \rightarrow 0$ can withstand the same stress.

This is the principle behind the proposed technique, which can be further illustrated by Figure 13. Z_{good} and Z_{weak} are the metastability points or switching thresholds of a defect-free and a defective cell respectively. If we can set the test
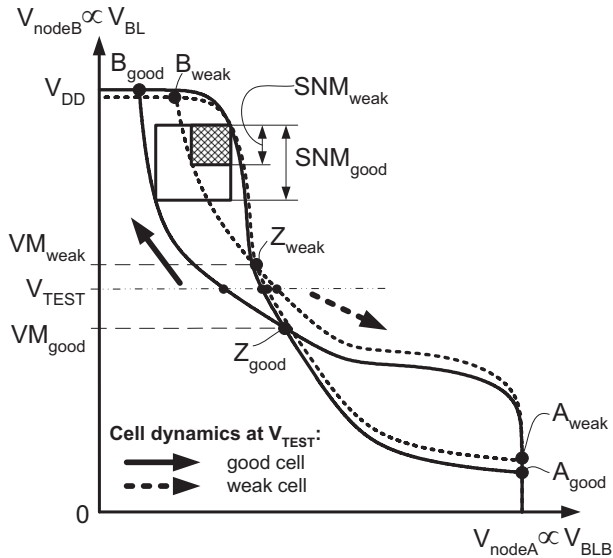
Figure 13 Choice of V_{TEST} with respect to the VTCs of a good and a weak SRAM cell.

voltage V_{TEST} to be above VM_{good} but below VM_{weak}, the weak cell will flip, whereas the good cell will withstand the test stress. Solid and dotted arrows illustrate the cell's dynamics after V_{TEST} has been lifted.

The proposed technique is based on the realization that the precharged bit line BL coupled through the access transistor $Q12$ to the node B of the reference cell carrying a "0" (Figure 12) will be gradually discharged by the I_{read} of the reference cell. The discharge rate can be expressed by Eq.(1) and is a function of the *total duration* that the word line of the reference cell has been enabled.

$$\Delta V_{BL} = \frac{I_{read} * t_{WL\_REF\_pw}}{C_{BL}} \qquad (1)$$

where: ΔV_{BL} – discharge of the bit line after each enabling of the WL_REF; I_{read} – cell read current of the reference cell; $t_{WL\_REF\_pw}$ – pulse width of the reference cell word line pulse; C_{BL} – bit line capacitance.
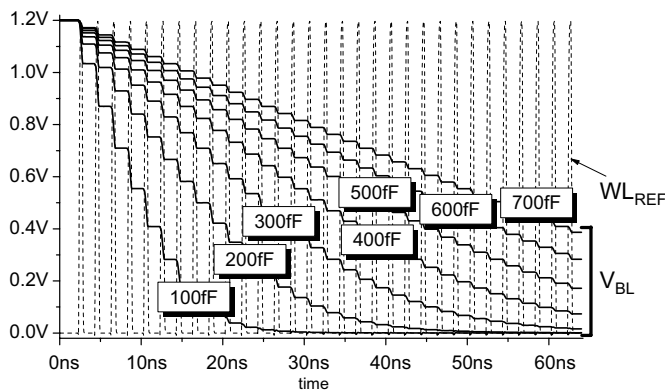

Figure 14 Word line pulses of the reference cell discharge the bit line for various values of the bit line capacitance. CMOS 0.13μm, $t_{WL\_REF\_pw} = 410ps$.
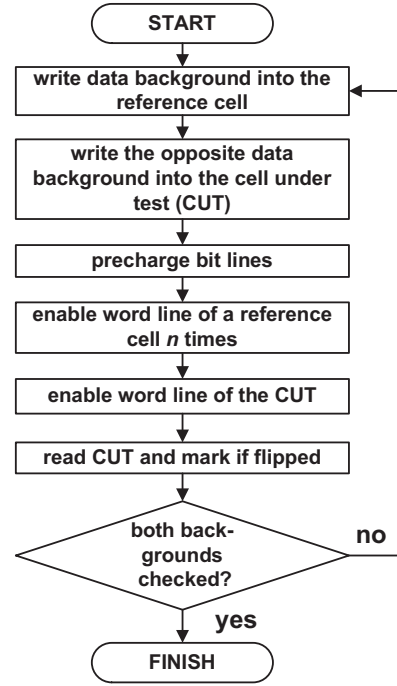

Figure 15 Flow diagram of the proposed Word Line Pulsing Technique for stability fault detection in SRAM cells.

Figure 14 shows the waveforms of the step-wise discharge of V_{BL} after applications of each of the 32 WL_REF pulses. Since ΔV_{BL} is inversely proportional to C_{BL}, the bit line discharge rate is slower for the more capacitive bit lines. Smaller ΔV_{BL} steps facilitate higher precision in setting of the bit line voltage and thus, finer programmable stress settings for the proposed technique. In SRAM architectures with hierarchical bit lines, C_{BL} can be increased during the application of the WLPT by enabling all the bit line MUXs that connect the local bit lines to the global in a given column.

The flow diagram of the proposed weak cell detection technique is shown in Figure 15. The test procedure consists of writing the opposite data backgrounds into the reference cell and the CUT. Next, after the normal precharge we enable the word line of the reference cell N times gradually discharging the bit line as shown in Figure 14. Then, we enable the word line of the CUT to subject the CUT to the weak overwrite stress. After that a normal read operation is performed on the CUT to determine whether or not the CUT has flipped. To ensure the coverage of asymmetric defects as well, we invert the data background stored in the reference cell and the CUT and repeat the test sequence. This test can be conducted in parallel on a word line by word line basis with one reference cell and one CUT per column.

4.2 Implementation Variations

Since the rate of the bit line discharge by the reference cell is determined by the total duration that the word line of the

reference cell has been enabled, the required degree of the bit line discharge can be achieved in several ways. The first method is illustrated in Figure 14. The total enabled duration of WL_REF can be composed of N pulses. The desired resolution of the bit line discharge can be provided by changing the number of the WL_REF pulses. The second possible approach is to fix the number of WL_REF pulses N while changing their pulse width. The third approach is to hold WL_REF for a predefined time period ($N = 1$) to discharge the bit line to the required level.

The reference cell can be interchanged with the CUT or another cell sharing the same bit lines with the CUT. Spread of I_{read} of the reference cells caused by the process variations can be alleviated by using a larger dedicated reference cell. Another degree of freedom can be provided by employing several dedicated reference cells with different I_{read}. In other words, the WLPT offers extended implementation flexibility of setting the weak overwrite stress.

5 WLPT Detection Capabilities

This section demonstrates the weak cell detection capabilities of the proposed technique.

The proposed WLPT has been verified for various values of the bit line capacitance C_{BL}, number N and the pulse width $t_{WL\_REF\_pw}$ of WL_REF pulses. It proved to be capable of detecting a wide range of resistive defects. To demonstrate the detection capabilities of the proposed technique we will use twelve WL_REF pulses with the pulse width of $410ps$ and $C_{BL} = 400fF$.

It was found that if the overwrite stress is too strong, i.e. the bit line is discharged below a certain point, which in our case was 0.55V, then even the defect-free cells will flip. This region is represented in Figure 16 by the patterned rectangle. As was mentioned before, the rate of the bit line discharge and thus, the number of stress settings is a function of C_{BL}. Depending on C_{BL} values, a different number of WL_REF pulses is required to reach the desired degree of the bit line discharge.

Detection of a symmetric defect (resistive contact "1" in Figure 7 and $R1$ in Figure 12) is shown in Figure 17. After WL_REF has been enabled twelve times, the bit line has been discharged to $V_{BL} = 650mV$. Figure 17(a) demonstrates that for $R1 = 80k\Omega$ the potentials of nodes A and B of the cell have not reached the metastable point and a symmetric defect with resistance of $80k\Omega$ has not been detected. However, for the defect resistance of $120k\Omega$ (Figure 17(b)), node B has been driven low enough to cross the switching threshold of the inverter formed by transistors $Q1$ and $Q3$ and the CUT has flipped its state. Consequently, when the CUT is read back after the application of the test procedure, the cell with the defect resistance $R1 = 120k\Omega$ will be marked as defective.

Note that the slope dV_{out}/dV_{in} of the cell's VTC in the metastability region, which is proportional to the ac gain of
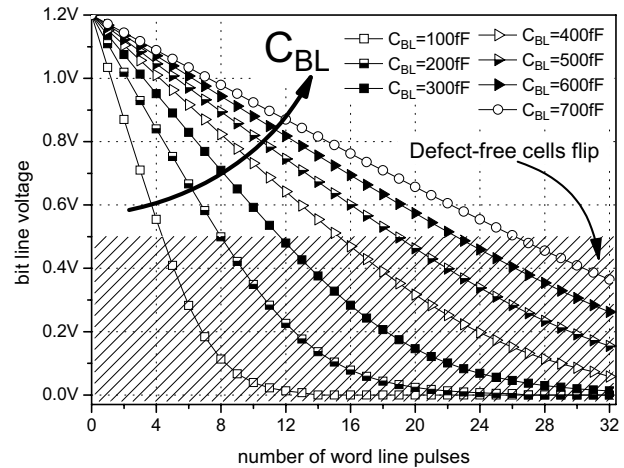

Figure 16 **Discharge of the bit line as a function of the number of word line pulses of the reference cell and the bit line capacitance.**

the cell is steeper for the cell with the higher SNM (Figure 13). The resolving capability (gain-bandwidth product) of the cell in the metastable region is also proportional to the SNM [20]. Therefore, if the SNM of the cell is higher, the cell will have a higher immunity against the metastable state and will recover from the test disturbance quicker. However, if the stability of the cell is weakened by a defect or a mismatch and the SNM is reduced (Figures 9,10,11), such a cell will stay in the metastability region longer. Thus, to extend the lower end of the detection range of the weak open defect resistance, the duration of the WL_CUT pulse should be sufficient to allow for the extended metastability window of the weaker CUT before it resumes a stable state.

For instance, if the value of $R1$ in the CUT is between $80k\Omega$ and $120k\Omega$, e.g. $95k\Omega$, the potentials of node A and node B move closer to each other and to the metastable point of the CUT. Due to the reduced ac gain in this region, WL_REF pulse should be asserted for several nanoseconds for such a cell to reach a stable state.

Waveforms very similar to those presented in Figure 17 have been obtained for an asymmetric defect $R3$ with $R3_{undetected} = 180k\Omega$ and $R3_{detected} = 190k\Omega$. The proposed WLPT has also been verified to successfully detect strong opens in the gates of PMOS transistors.

The detection range of the proposed technique has been characterized for symmetric (Figure 18(a)) and asymmetric (Figure 18(b)) defects causing DRFs and SFs. It demonstrated high detection selectivity of the defect resistances. The solid line represents the detection boundary, where the area above is the detected values of the defect resistance at a given bit line voltage and the patterned area represents the not detected region.

Figure 18(c) demonstrates the detection of the bridge resistance between node A and node B as per the Weak Cell Fault Model presented in [1]. According to our estimations, a resistive bridge between node A and node B (shown
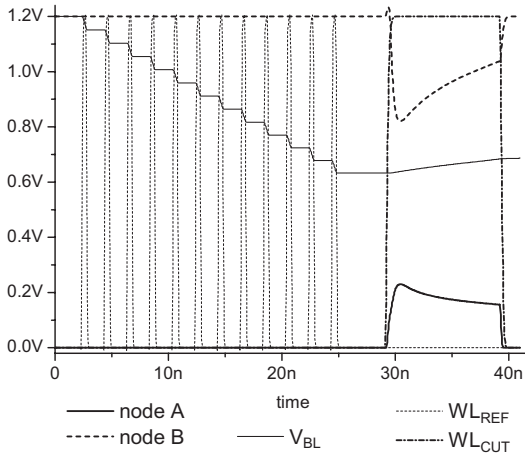
(a) Symmetric defect with $R1 = 80k\Omega$ is not detected.
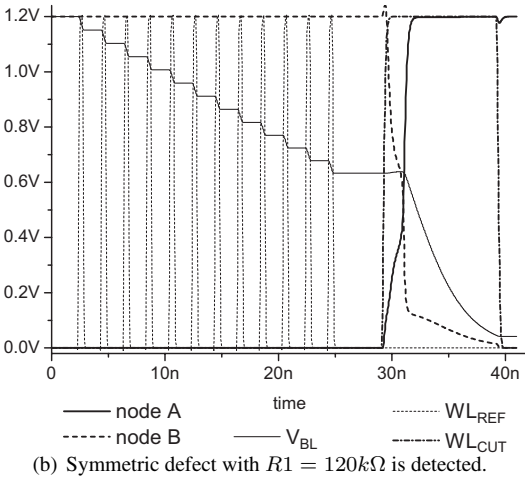
(b) Symmetric defect with $R1 = 120k\Omega$ is detected.

Figure 17 **Example of a symmetric defect with (a) resistance of $80k\Omega$ (not detected) and (b) resistance of $120k\Omega$ (detected). CMOS 0.13μm, $C_{BL} = 400fF$.**

in Figures 1,7) is one of the more probable bridge defects in the cell. Since it also represents a symmetric negative feedback branch for the two cell's inverters, its resistance directly reducing the gain of the cell in the metastable region, changes the shape of its VTCs and thus, reduces the SNM of the cell. We believe that it can mimic the behavior of a multitude of resistive bridges in an SRAM cell (see Figure 10). Since the SNM dependence on the bridge resistance is the inverse of that of the resistive opens, the solid line in Figure 18(c) also has the inverse slope as compared to Figures 18(a) and 18(b). The higher bridge resistance values correspond to a more stable cell with a higher SNM. Thus the detected resistance region in Figure 18(c) is below the solid boundary line.
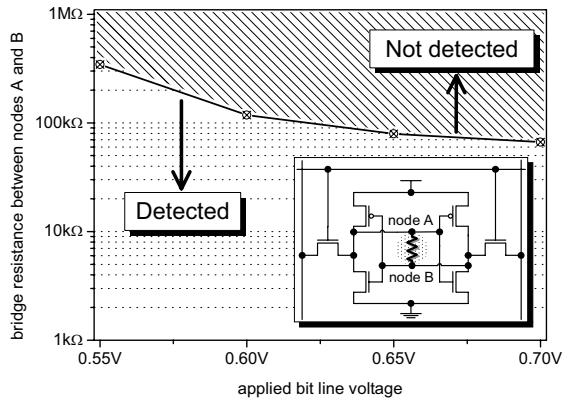
6 Conclusions

March tests often fail to detect subtle defects in SRAM arrays. These subtle defects, depending on severity, can cause Stability Faults (SFs) or Data Retention Faults (DRFs). Detection of many of such faults requires special defect-
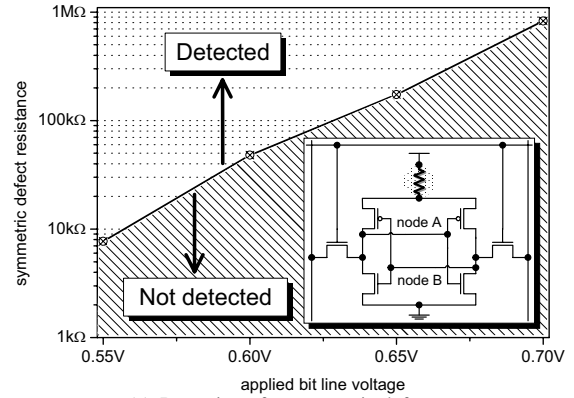
(a) Detection of a symmetric defect.
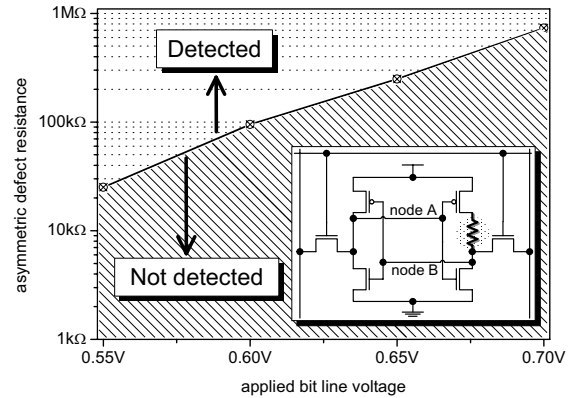
(b) Detection of an asymmetric defect.

(c) Detection of a resistive bridge between node A and node B (shown in Figures 1,7).

Figure 18 **Detection of a symmetric (a), an asymmetric (b) defects in PMOS transistors of 6T SRAM cell and a resistive bridge between node A and node B (CMOS 0.13μm, $C_{BL} = 400fF$).**

oriented DFT techniques, such as the Weak Write Test Mode [9]. However, the increased defect density and process spread in modern technologies calls for test techniques with digitally adjustable test stress. The proposed Word Line Pulsing Technique (WLPT) for detection of SFs and DRFs in SRAM cells offers extended flexibility in terms of the test stress setting and the implementation options. Due to higher precision of the stress setting for the

more capacitive bit lines, the WLPT may be more attractive for the cell stability testing in the larger SRAM arrays.

We believe that the WLPT has a potential to replace the Data Retention Test. It has short test time, no high-temperature requirements and a significantly greater range of the detected defect resistances with the ability to adjust this range during the test. Moreover, the programmability of the test stress allows tracking and compensating for the process changes without the time-consuming post-silicon design iterations.

7 Acknowledgments

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