World's first monolithic 3D-FPGA with TFT SRAM over 90nm 9 layer Cu CMOS

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Abstract

World's first monolithically integrated Thin-Film-Transistor (TFT) SRAM configuration circuits over 90nm 9 layers of Cu interconnect CMOS is successfully fabricated at 300mm LSI mass production line for 3-dimensional Field Programmable Gate Arrays (3D-FPGA). This novel technology built over the 9th layer of Cu metal features aggressively scaled amorphous Si TFT having 180nm transistor gate length, 20nm gate oxide, fully silicided gate, S/D, all below 400C processing essential to not impact underlying Cu interconnects. Low temperature TFT devices show excellent NTFT/PTFT transistor I_{on}/I_{off} ratios over 2000/100 respectively, operate at 3.3V, E-field scalable, and are stable for SRAM configuration circuits. We believe this 3D-TFT technology is a major breakthrough innovation to overcome the conventional CMOS device shrinking limitation.

Introduction

Downscaling of conventional CMOS device has reached its limitations and cost to develop sub 40 nm processes has dramatically increased. To overcome the CMOS shrinking limitation, various technologies such as high-k, metal gate, stress liner, and e-SiGe etc. are applied [1] or many new concept devices are reported [2-4].

We propose a new concept for a novel 3D-FPGA using a-Si TFT configuration SRAM (Fig. 1) over bulk CMOS logic to reduce FPGA die area, die cost and power [5]. 3D-FPGA is for prototype & low volume production. For high volume production, the TFT layer is replaced with metal layer (Fig. 2) during fabrication, which means FPGA die converts to timing-exact ASIC die without redesign effort, lowering die cost further and improving reliability. In this paper, we present the TFT fabrication technology & TFT device characteristics built over 9 layers of Cu interconnected CMOS circuits at processing temperature below 400C.

Process technology

Process flow for the TFT device on LSI is shown in Fig. 3. First, underlying LSI was fabricated on 300mm-Si Toshiba standard 90nm CMOS technology. After opening via's to connect the LSI to TFT, a-Si TFT' were fabricated below 400C, which is essential to maintain the reliability of Cu metal. This constraint limits the performance of TFT devices. Fig. 4 shows a cross sectional image of 9 metal layer CMOS with TFT layer (left Fig.) and a detailed TFT transistor (right Fig.). TFT transistor channel length is 180nm, with 20nm gate dielectric formed by plasma-TEOS. Fully silicided a-Si gate electrode (FUSI gate) is formed to control the Vth and boost the transistor performance. S/D is also fully silicided for higher current and to connect to underlying CMOS. NiPt and a-Si thickness is accurately controlled to form FUSI gate and S/D. TFT transistor image is shown in Fig. 5. TFT transistor performance is enhanced by using majority carrier accumulation devices. Table-1 shows the key features for this a-Si TFT technology demonstrating the densest integration for a-Si TFT in the industry. Key features of TFT processing used Toshiba 65nm CMOS fabrication techniques.

Device characterization

Fig. 6 (a) shows TFT transistor characteristics. At Vg=3.3V, I_{on}/I_{off} ratio of NTFT (L/W=180/160 nm) > 2000 and PTFT (L/W=180/200 nm) > 100 are achieved. Fig. 6 (b) depicts the output characteristics and Fig. 7 is C-V characteristics of TFT device. Though PTFT I_{on}/I_{off} ratio is lower with under 400C a-Si, all I_{on}/I_{off} ratios ($I_{on}N/I_{off}N$, $I_{on}P/I_{off}P$, $I_{on}N/I_{off}P$, $I_{on}P/I_{off}N$) are over 100 (Fig. 8). To achieve these high I_{on}/I_{off} ratios, O_2 plasma and thinner EOT are applied. Moreover, Vth is controlled by FUSI gate and implantation condition.

O_2 plasma is implemented before gate dielectric deposition to enhance PTFT drive current (Fig. 9). O_2 atoms decrease the trap states in TFT active area [6]. Channel implant conditions are carefully chosen to fix the optimal Vth (Fig. 10). Fig. 11 shows PTFT has a larger effect than NTFT on I_{on}/I_{off} ratio by decreasing EOT thickness. On the other hand, Fig. 12 indicates that 20nm EOT is needed to meet 10 year TDDB lifetime. Therefore, EOT 20nm is chosen at the expense of transistor performance. TDDB lifetime of TFT transistor is shorter than that of conventional CMOS transistor due to plasma-TEOS gate Oxide and increased trap density.

Fig. 13 is a top view of 9-transistor conservative TFT SRAM cell after gate formation. Fig. 14 shows the TFT SRAM circuit and inverter characteristics. We successfully get the ideal inverter curve. Over 230 Million TFT transistors (26Mb SRAM) are used to configure 100K Look-Up-Table logic 3D-FPGA (Fig. 15). TFT transistor on and off currents scale with lateral E-field. Off currents for devices with channel lengths 90nm to 250nm at 2.5V, 3.3V and 5V is shown in Fig. 16. Similarly on currents (not shown) also scale with lateral E-field. Thus these TFT transistors can be scaled with underlying CMOS to 40nm logic node easily to fabricate high density 3D-FPGA.

Conclusions

Excellent 3.3V a-Si TFT characteristics with FUSI gate and S/D fabricated below 400C on 9 layers of Cu interconnects LSI are demonstrated. By optimizing the O_2 plasma, Vth, and EOT, sufficient I_{on}/I_{off} ratios for fully functional 26Mb SRAMs are obtained. Moreover, we confirmed the TDDB lifetime met 10 year with 20nm EOT. This new E-field scalable TFT structure would be a breakthrough innovation to overcome the conventional CMOS device shrinking limitation, and to manufacture high density, low cost novel 3D-FPGA.

References

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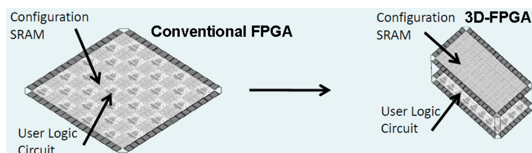


Fig.1: A new concept for a novel 3D-FPGA using a-Si TFT configuration SRAM over bulk CMOS.

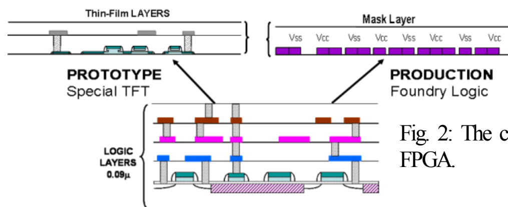


Fig. 2: The concept of 3D-TFT FPGA.

- Formation of underlying CMOS
- Formation of via's to connect the LSI to TFT
- a-Si TFT active area formation and channel implantation
- TFT gate formation with O_2 plasma
- S/D implantation and formation of sidewall
- NiSi metallization at TFT active area and gate a-Si
- Formation of TFT Metal 1 and passivation

Fig. 3: Main process flow of TFT over 9 layer Cu CMOS.

Table.1: TFT Technology minimum pitchs

	Width (nm)	Pitch (nm)
Contact to LSI M9	120	430
Active Area	100	220
Gate	180	300
Contact to TFT M1	120	300
TFT Metal 1	120	240

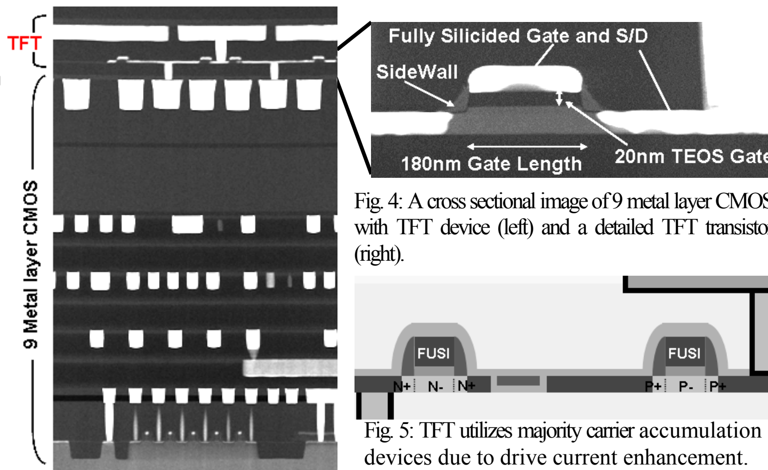
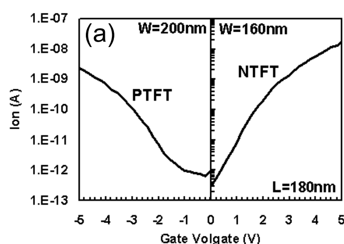


Fig. 4: A cross sectional image of 9 metal layer CMOS with TFT device (left) and a detailed TFT transistor (right).

Fig. 5: TFT utilizes majority carrier accumulation devices due to drive current enhancement.



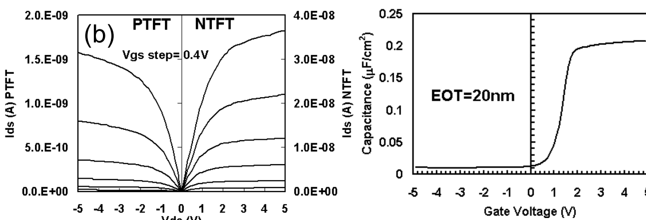


Fig. 6: (a) TFT transistor characteristics. I_{on}/I_{off} ratio of NTFT > 2000 and PTFT >100 at 3.3V are achieved. (b) Output characteristics of NTFT and PTFT transistor.

Fig. 7: C-V characteristics. 20nm gate dielectric is formed by plasma-TEOS.

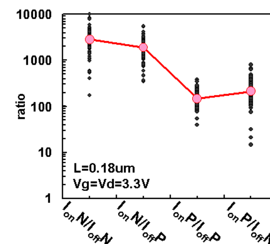


Fig. 8: All Ion/Ioff ratios are over 100 by optimization of O_2 plasma, EOT, and Vth.

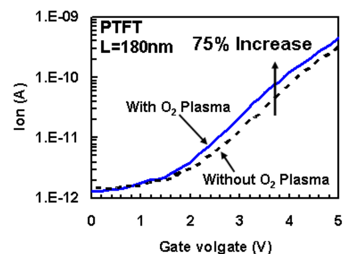


Fig. 9: 75% Improvement of PTFT drive current was obtained with O_2 plasma.

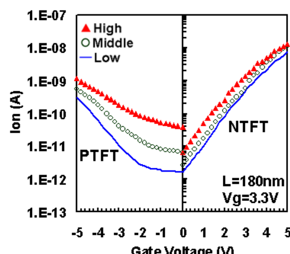


Fig. 10: Channel implant dose dependence. Optimal conditions were chosen.

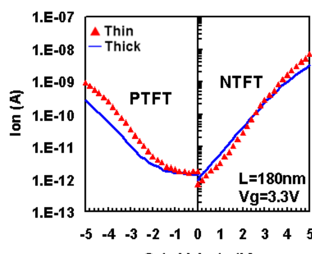


Fig. 11: Improvement of NTFT and PTFT I_{on}/I_{off} ratio by thinning EOT. EOT was finally chosen to maintain the TDDB lifetime.

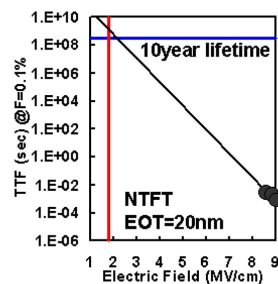


Fig. 12: TFT TDDB lifetime prediction. Lifetime meets 10 year with 20nm EOT.

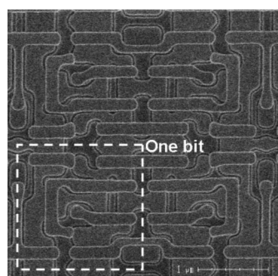


Fig.13: A top view of 9-transistor conservative TFT SRAM after gate formation.

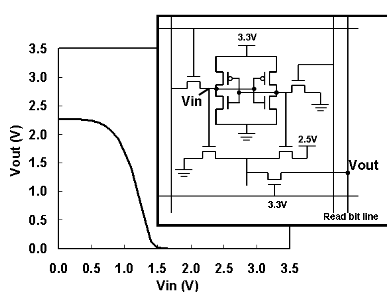


Fig.14: The TFT SRAM circuit and inverter characteristics. The ideal inverter curve was obtained.

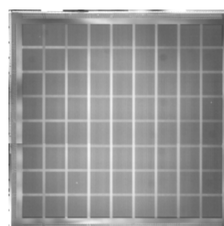


Fig. 15: A die photo image. 26Mb TFT SRAM on CMOS.

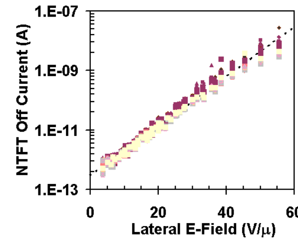


Fig. 16: NTFT Off currents with channel lengths 90nm to 250nm at 2.5V, 3.3V and 5V.