npj | 2D Materials and Applications

www.nature.com/npj2dmaterials

ARTICLE OPEN

Check for updates

$WSe_2/SnSe_2$ vdW heterojunction Tunnel FET with subthermionic characteristic and MOSFET co-integrated on same WSe_2 flake

Nicolò Oliva[1]✉, Jonathan Backman[2], Luca Capua[1], Matteo Cavalieri[1], Mathieu Luisier[2] and Adrian M. Ionescu[1]

Two-dimensional/two-dimensional (2D/2D) heterojunctions form one of the most versatile technological solutions for building tunneling field effect transistors because of the sharp and potentially clean interfaces resulting from van der Waals assembly. Several evidences of room temperature band-to-band tunneling (BTBT) have been recently reported, but only few tunneling devices have been proven to break the Boltzmann limit of the minimum subthreshold slope, 60 mV per decade at 300 K. Here, we report the fabrication and characterization of a vertical p-type Tunnel FET (TFET) co-integrated on the same flake with a p-type MOSFET in a $WSe_2/SnSe_2$ material system platform. Due to the selected beneficial band alignment and to a van der Waals device architecture having an excellent heterostructure 2D–2D interface, the reported tunneling devices have a sub-thermionic point swing, reaching a value of 35 mV per decade, while maintaining excellent ON/OFF current ratio in excess of 10^5 at $V_{DS} = 500$ mV. The TFET characteristics are directly compared with the ones of a WSe_2 MOSFET realized on the very same flake used in the heterojunction. The tunneling device clearly outperforms the 2D MOSFET in the subthreshold region, crossing its characteristic over several orders of magnitude of the output current and providing better digital and analog figures of merit.

npj 2D Materials and Applications (2020)4:5 ; https://doi.org/10.1038/s41699-020-0142-2

INTRODUCTION

The scaling of transistors has been the driving force behind the digital revolution over the last decades, enabling enhanced switching frequency, higher density, decreased cost and enormous increase in computational power[1]. However, several fundamental and technical challenges potentially jeopardize the performance of aggressively scaled CMOS technology nodes[2,3]. In particular, the power supply scaling, fundamental in order to reduce the dynamic power consumption of a transistor, is currently halted because of the fundamental physical limit of 60 mV per decade for the subthreshold slope of devices relying on thermionic injection. Voltage scaling at constant gate overdrive results in an unacceptable increase of the OFF state current and consequently of the static power consumption[4].

In order to overcome the Boltzmann limit to the subthreshold slope, it is necessary to rely on a different carrier injection mechanism[4–6]. Tunnel FETs (TFETs), for instance, exploit band-to-band tunneling (BTBT) so as to achieve subthermionic subthreshold slope and potentially outperform CMOS in the subthreshold regime[4,7]. Promising performance has been obtained in silicon, germanium, III–V and heterojunction TFET, with sub 60 mV per decade slope[4,8,9]. However, the difficulties of obtaining sufficiently sharp doping profiles or material interfaces pose incredible challenges to the realization of tunneling switches exploiting conventional three-dimensional semiconductors. Indeed, band-tail states and trap assisted tunneling paths can drastically degrade the turn-on slope of such devices[10,11].

In this contest, two-dimensional (2D) materials are promising candidates for the realization of high performance TFETs, providing both a huge variety of electronic properties and the possibility of assembling atomically sharp van der Waals heterojunctions[12]. Several demonstrations of BTBT in 2D-based heterojunctions have been recently reported, with negative differential resistance (NDR) observed in the output characteristic at room or cryogenic temperatures[13–18]. However, few 2D TFETs were able to break the 60 mV per decade limit at room temperature[19,20]. Several materials have been investigated by either atomistic simulations or experimental studies. The onset of BTBT has been reported in WSe_2/MoS_2, $BP/SnSe_2$, BP/MoS_2, Ge/MoS_2 and $WSe_2/SnSe_2$ heterojunctions[13,15–21]. This latter material system has attracted particular interest because of the predicted broken or nearly broken gap band alignment and the peculiar electronic properties of these two members of the transition metal dichalcogenide (TMDC) family. WSe_2 is an intrinsic semiconductor that exhibits both electron and hole conduction with relatively high carrier mobility[22]. Suppression or enhancement of one of the two conduction branches can be effectively obtained exploiting electrostatic doping[23–25]. This feature, unusual for TMDC 2D materials that are usually unipolar with dominant electron conduction, presents this material as one of the best candidate for the realization of a single material 2D CMOS technology. Conversely, $SnSe_2$ is degenerately n doped and exhibits an extremely low sensitivity to electrostatic control[26,27]. Several $WSe_2/SnSe_2$ heterojunction devices exhibiting NDR have been recently reported, and an n-type TFET with minimum subthreshold slope (SS) of 50 mV per decade was demonstrated[19].

Recently, we reported at IEEE IEDM 2019 a preliminary $WSe_2/SnSe_2$ p-type TFET with room temperature subthermionic subthreshold slope, demonstrating the potential of this material system for the realization of tunneling devices with good characteristics[28]. Here, we report new data confirming the subthermionic values for the subthreshold slope derived from both source and drain currents with small hysteresis. Moreover, we report first principle derivation of the expected band alignment at

[1]Nanoelectronic Devices Laboratory (NanoLab), EPFL, 1015 Lausanne, Switzerland. [2]Department of Information Technology and Electrical Engineering, ETH, 8092 Zürich, Switzerland. ✉email: nicolo.oliva@epfl.ch

the junction obtained by density functional theory (DFT) calculations. We then discuss the possible BTBT mechanism matching our experimental findings. Finally, we provide a direct comparison of the heterojunction TFET and the built-in WSe_2 MOSFET in terms of both digital and analog figures of merit of the out best device. We show that the $WSe_2/SnSe_2$ TFET outperforms its WSe2 counterpart over several orders of magnitude of the output current both for analog and digital applications.

RESULTS AND DISCUSSION

Heterojunction band diagram

The structure of the fabricated $WSe_2/SnSe_2$ heterojunction devices is shown in Fig. 1. In order to accurately model the band alignment of the heterostructure, VASP[29], a density functional theory tool, is employed. A supercell containing six layers of each material is constructed by applying a relative rotation of 30° and a small strain of 0.22 % to both layers, resulting in a hexagonal cell containing four units of WSe_2 and three units of $SnSe_2$ in their respective layers. This configuration ($30° + 0.22\%$ strain) was chosen because it minimizes the size of the supercell required to perform DFT calculations. It should be noted that the strain value is kept very small and the rotation angle is not known experimentally. The results are expected to marginally depend on this parameter. Electronic structure calculations are performed using the generalized gradient approximation (GGA) of Perdew, Burke and Ernzerhof (PBE)[30], with a $11 \times 11 \times 1$ Monkhorst-Pack *k*-point grid and a 500 eV plane-wave cutoff energy. The convergence criteria are set to less than 10^{-2} eV Å^{-1} force acting on each ion and a total energy difference smaller than 10^{-3} eV between two subsequent iterations. van der Waals interactions are included through the DFT-D3 method of Grimme[31]. The resulting computed band structures of WSe_2 and $SnSe_2$ are shown in Fig. 1b, where the bands have been colored to indicate the material from which they originate. A closer look at the derived band alignment is provided in Fig. 1c, that shows a type III, broken gap with an expected energy overlap of 26 meV.

Figure 1d represents a qualitative band diagram of the $WSe_2/SnSe_2$ heterojunction obtained starting from reported results on similar heterostructures assembled with multilayer WSe_2 and thicker $SnSe_2$ flakes[13]. As confirmed by our DFT calculations, at the equilibrium the band alignment is of type III, resulting in a non-zero energy overlap between $SnSe_2$ conduction band and WSe_2 valence band. By applying a positive drain bias to the WSe_2 contact, electrons can tunnel from $SnSe_2$ to WSe_2 providing a BTBT conduction path. A negative bottom gate voltage determines an upward shift of WSe_2 bands, resulting in an increase of the energy overlap and an enhanced tunneling current. Therefore, we expect our three terminal heterojunction devices to exhibit a tunneling current at positive drain to source voltage with negative bottom gate bias.

Device fabrication

The three-dimensional schematic view of the final heterojunction device is shown in Fig. 1a, which consists of a back gated $WSe_2/SnSe_2$ heterojunction with Pd Schottky contacts deposited on each side of the junction. The first fabrication step is the deposition by atomic layer deposition (ALD) of 50 nm layer of hafnium oxide (HfO_2) on a Si wafer. The bottom gate electrode is then defined by electron beam lithography (EBL) on a MMA/PMMA bilayer and lift-off of 50 nm of tungsten (W). The gate stack is then completed by a second ALD deposition of 10-nm-thick HfO_2. WSe_2 flakes have been mechanically exfoliated directly on the patterned substrate starting from commercially available bulk samples. In order to form the junction, $SnSe_2$ flakes were first exfoliated on a poly(dimethylsiloxane) (PDMS) transparent substrate and then deterministically transferred on previously selected WSe_2 samples[32,33]. The source and drain contacts were deposited by lift-off of a Cr/Pd stack (5/50 nm) after a second EBL

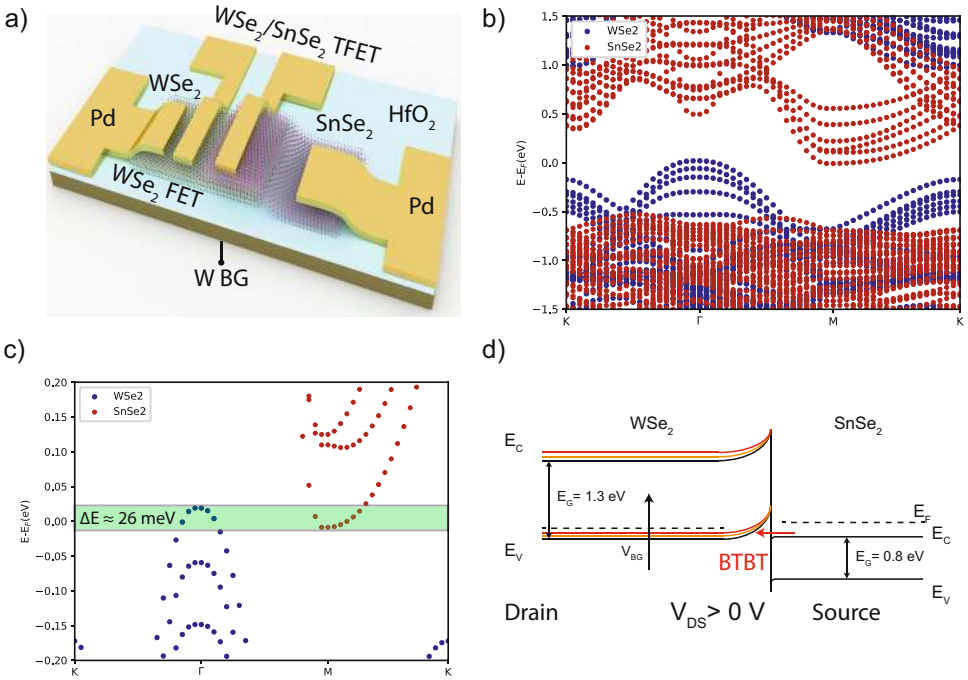

Fig. 1 Structure and expected band alignment of the fabricated $WSe_2/SnSe_2$ heterojunction. a Three-dimensional schematic of the final device structure, consisting in a back gated $WSe_2/SnSe_2$ heterojunction FET with Pd Schottky contacts to both sides of the junction. **b** Band structure of WSe_2 (blue) and $SnSe_2$ (red) flakes obtained from DFT calculations. **c** Expected band alignment at the heterojunction; according to our DFT calculations, a 26 meV energy overlap is present between the edges of WSe_2 valence band and $SnSe_2$ conduction band. **d** Qualitative band diagram at the heterojunction based on reported material properties. The expected band alignment is of type III, broken-gap, and under positive drain bias applied to the WSe_2 contact electrons are expected to tunnel from $SnSe_2$ conduction band to WSe_2 valence band.

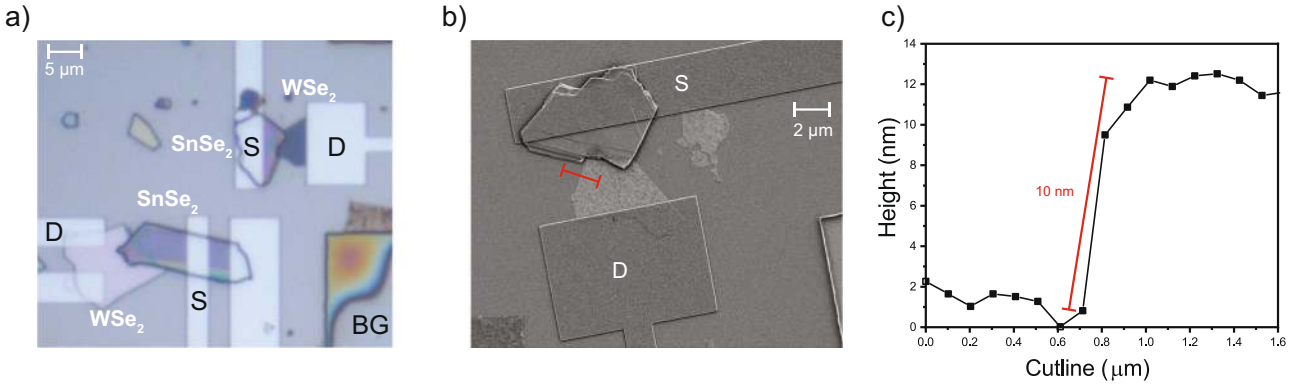

Fig. 2 Optical and scanning electron microscopy imaging. a Optical image of two fabricated $WSe_2/SnSe_2$ devices. It is possible to distinguish the two flakes for each junction, the overlap region and the Pd contacts to the two sides of the heterostructure. For flakes sufficiently large it is possible to deposit four contacts, so to be able to characterize both the internal WSe_2 FET and the heterojunction device. **b** SEM image of a final device with highlighted cutline for thickness estimation. **c** AFM profile of the WSe_2 flake taken along the red cutline shown in the SEM image. The presented devices have been fabricated with 10-nm-thick WSe_2 flakes.

step on MMA/PMMA bilayer resist. Figure 2a shows an optical image of two fabricated devices: the different flakes, the overlap region and the Pd contacts are clearly visible. Depending on the dimensions of the flakes, either two or four electrodes per heterojunction were deposited, so to be able to characterize separately the single materials and the heterostructure conduction. The last fabrication step consists in the local etching of the bottom gate dielectric by ion beam etching (IBE) in order to provide electrical access to the W contact. The mask is obtained by EBL on a PMMA resist. Figure 2b is a scanning electron microscopy (SEM) image of a completed device. Our devices are fabricated with 10-nm-thick WSe_2 flakes and relatively thick, multilayer $SnSe_2$ flakes (with thickness larger than 50 nm). The atomic force microscopy (AFM) profile of a typical WSe_2 flake (taken measuring along the red cutline in Fig. 2b) is reported in Fig. 2c.

Electrical characterization

All the electrical measurements have been performed at room temperature and ambient conditions. The WSe_2 contact is always biased as the drain of the heterojunction device.

As a first step, we characterized the electrical properties of individual $SnSe_2$ and WSe_2 flakes. The double-sweep transfer characteristic, drain current versus the gate voltage, I_D–V_G, and the output characteristic, drain current versus the drain voltage, I_D–V_D, of a representative $SnSe_2$ FET is reported in Supplementary Fig. 1. As expected, given the degenerate n doping typical of this 2D material, the gate bias has a very limited capability of modulating the conduction in the channel[27,34], that cannot be depleted of electrons for the investigated range of voltages resulting in a ON/OFF current ratio lower than two. The low drain voltage region of output characteristic shows an ohmic contact is achieved between the Pd electrodes and multilayer $SnSe_2$ flakes.

The transfer characteristic, drain current versus gate voltage, I_D–V_G, of a representative WSe_2 FET measured at different drain biases is reported in Fig. 3a. The device, whose channel is 2 μm wide, exhibits p-type polarity with ON/OFF current ratio larger than 10^5. The hole mobility can be extracted applying the Y function method (see Supplementary Fig. 2)[35,36]. At $V_D = 500$ mV, the carrier mobility is 1.8 $cm^2 V^{-1} s^{-1}$, comparable to reported results on similar devices[23]. The inset in Fig. 3a shows the transconductance of the device, g_m, which saturates upon reaching the maximum value. The ratio of the gate transconductance and the drain current gives the transconductance efficiency, plotted in Fig. 3b for three values of the drain voltage. g_m/I_D is a fundamental parameter to evaluate the potential of a technology platform for analog applications[37]. Indeed, high transconductance efficiency values are fundamental for the design of high performance, low power consumption differential couples. In a MOSFET, the maximum value of the transconductance efficiency is physically constrained to be lower than 40 V^{-1} and the maximum value can be achieved operating the device in its weak inversion regime[38]. As shown in Fig. 3b, our WSe_2 pMOSFET achieves a g_m/I_D value comprised between 25 and 30 V^{-1}, comparable to advanced bulk Si FET[39–43].

The potential of a technology to realize energy efficient, low voltage digital switches can be evaluated considering its subthreshold slope. A steep turn-on characteristic is fundamental to scale down the power supply, or to achieve higher current at lower gate voltage and, therefore, faster switching for the same gate bias. Figure 3c shows the subthreshold slope as a function of the output current for the three investigated drain biases. The minimum point value is 80 mV per decade and point slopes around 100 mV per decade are maintained also at $V_{DS} = 500$ mV. Such results are better or comparable with the best reported back gated WSe_2 FETs[23,24,44–46]. Figure 3d–f collects the corresponding results obtained measuring the $WSe_2/SnSe_2$ heterojunction TFET based on the very same WSe_2 flake characterized as MOSFET. Comparing the transfer characteristics of the two devices (Fig. 3a, d) under the same drain bias, it is clear that the heterojunction TFET exhibits lower I_{ON}, lower I_{OFF}, more negative threshold voltage and steeper turn-on characteristic than its built-in WSe_2 MOSFET. The OFF state current is limited by the gate leakage, while the relatively large tunneling resistance at the heterojunction interface likely fixes the current level in the ON state. The inset of Fig. 3d shows the transconductance of the heterojunction FET, from which it is possible to derive the transconductance efficiency curve, represented in Fig. 3e as a function of the drain current. The $WSe_2/SnSe_2$ TFET exceeds, at room temperature, the $(kT/q)^{-1}$ ~40 V^{-1} fundamental limit of MOSFET g_m/I_D analog figure of merit, for all the considered drain biases. Similarly, the subthreshold slope plotted as a function of the drain current shown in Fig. 3f exhibits point swing below the 60 mV per decade Boltzmann limit for all the three drain biases. In order to evaluate the impact of the gate leakage current on the estimation of the subthreshold slope, in particular for current levels close to the leakage floor as in our case, it is important to consider both drain and source transfer characteristics, and their relative subthreshold swings. Supplementary Fig. 3 reports the I_D–V_G and I_S–V_G characteristics, demonstrating that the numerical derivatives of both source and drain measured currents versus the gate voltage result in subthermionic values of the turn-on subthreshold slopes at room temperature.

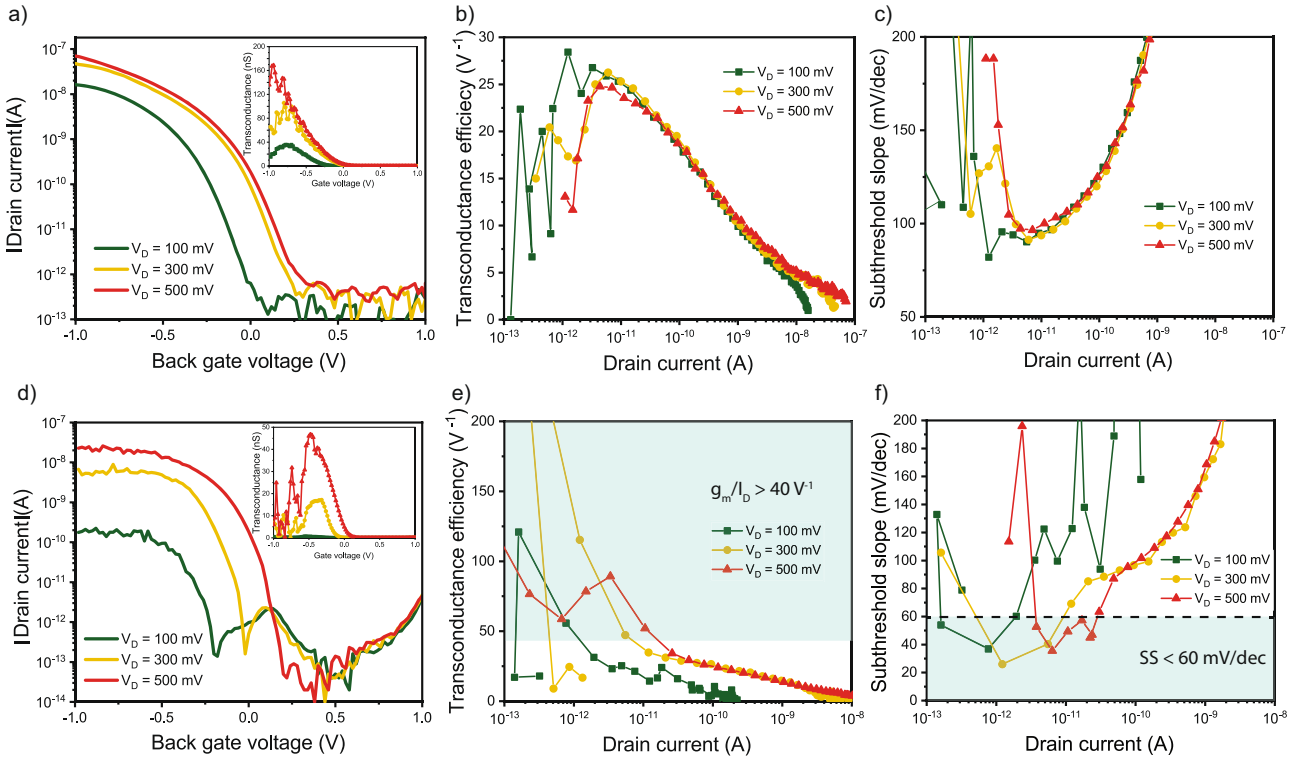

Fig. 3 Electrical characterization at room temperature (T = 300 K) of a representative WSe_2 FET and the $WSe_2/SnSe_2$ heterojunction device fabricated on the very same flake. a Transfer characteristic in semilogarithmic scale of the WSe_2 FET for increasing values of the drain bias. The ON/OFF current ratio is larger than 10^5 and the minimum subthreshold slope ranges from 80 to 110 mV per decade. Inset: transconductance as a function of the gate bias. **b** WSe_2 transconductance efficiency as a function of the device output current. **c** Subthreshold slope vs drain current for the MOSFET under different applied drain to source bias. The width of the WSe_2 FET is 2 µm. **d** Transfer characteristic in semilogarithmic scale of the $WSe_2/SnSe_2$ Tunnel FET for increasing values of the drain bias. The threshold voltage is shifted to more negative values with respect to the WSe_2 FET, while the turn-on slope is improved. Inset: transconductance as a function of the gate bias. **e** Heterojunction FET transconductance efficiency as a function of the device output current. For all the investigated drain to source biases, the peak transconductance efficiency exceeds the fundamental 40 V^{-1} limit characterizing MOSFET devices. **f** Subthreshold slope vs drain current for the TFET, showing room temperature subthermionic point swing for all the applied drain biases.

The transfer characteristics of a second couple of devices, again a WSe_2 MOSFET and its same flake $WSe_2/SnSe_2$ TFET are reported in Supplementary Fig. 4. As discussed in our IEDM paper[28], the output characteristic of this $WSe_2/SnSe_2$ TFET shows a clear, gate tunable NDR region, that together with the measured subthermionic subthreshold slopes contributes to demonstrate the onset of the BTBT conduction path schematically described in Fig. 1d.

In order to discuss in more details the differences between the WSe_2 and the heterojunction FETs, it is useful to directly compare the relative transfer characteristics. Figure 4a collects the I_D–V_G curves of our reference TFET and its built-in MOSFET, both measured applying $V_{DS} = 500$ mV. The TFET threshold voltage has been shifted so to match the MOSFET one and provide an easier correlation. The $WSe_2/SnSe_2$ heterojunction device has both a lower I_{OFF} current and steeper turn-on characteristic with respect to the WSe_2 FET (see the inset in Fig. 4a), crossing its characteristic at low current levels and indeed outperforming the MOSFET over almost three orders of magnitude of the output current. The minimum point subthreshold slope for the TFET is 35 mV per decade. As expected, the WSe_2 FET maintains a larger I_{ON} current with respect to the tunneling device[4], but the TFET current is indeed larger over the subthreshold region as highlighted in Fig. 4b, where the difference between the two devices current, normalized with respect to the WSe_2 FET current, is plotted as a function of the gate bias. This results in a larger transconductance over the corresponding bias window. Figure 4c shows the difference between the heterojunction TFET and its built-in MOSFET transconductances, normalized with respect to the MOS transconductance. In the subthreshold region, the $WSe_2/SnSe_2$ TFET provides a transconductance boost of roughly 70 % over the WSe_2 FET. A direct comparison of the two same flake devices transconductance efficiencies is presented in Fig. 4d as a function of the output current. The $WSe_2/SnSe_2$ heterojunction TFET not only overcomes the 40 V^{-1} analog efficiency limit at low current levels, but it consistently outperforms the WSe_2 FET, whose performance is comparable to long channel Si bulk MOSFETs[42,43], over the entire subthreshold region. Conversely, for large drain current the MOSFET transconductance is larger, reflecting the higher I_{ON} granted by the thermionic injection mechanism.

The reported results demonstrate the best reported experimental minimum subthreshold slope for 2D/2D heterojunction devices[13,18,19,21], while maintaining an ON/OFF current ratio larger than five orders of magnitude and co-integrating on the same flake both the heterojunction tunneling device and the WSe_2 MOSFET.

The co-integration of MOSFET and TFET on the same flake paves the way for the realization of hybrid devices with dual transport mechanism that combine the advantages of each of these devices while not requiring any additional lithography and production steps. The possibility of co-integrating TFET and MOSFET in the same material system and technology platform has been explored thoroughly for silicon and III–V based devices[47–51], but not yet in a true 2D/2D material system. Here, in Fig. 5a, we propose a new steep slope hybrid device, named dual transport (DT) FET consisting in the parallel connection of a $WSe_2/SnSe_2$ heterojunction TFET and its built-in WSe_2 MOSFET. Such device could inherit

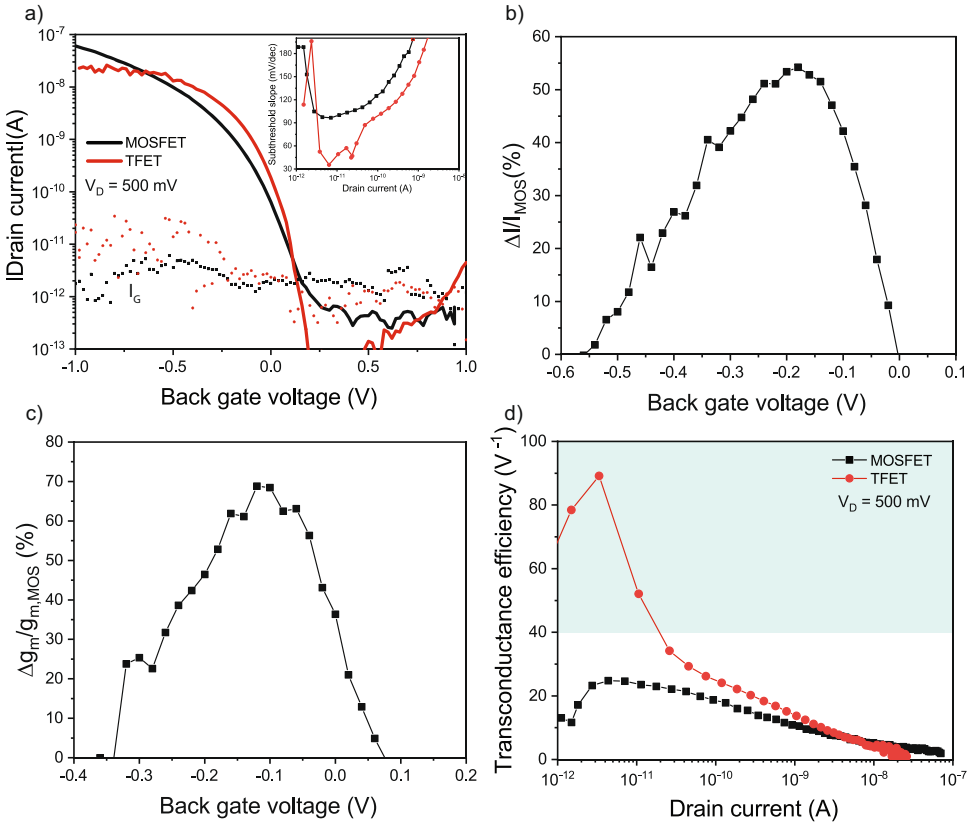

Fig. 4 Direct comparison of transfer characteristics at room temperature (T = 300 K) and digital/analog figures of merit of TFET and MOSFET built on the very same flakes. a Transfer characteristics of the TFET and its built-in MOSFET at a drain bias of 500 mV. The WSe_2/$SnSe_2$ FET threshold voltage is shifted so to match the MOSFET one and favor a more direct comparison. The dotted line is the gate leakage current. Inset: subthreshold slopes of the two devices vs the output current in logarithmic scale. **b** Difference between TFET and MOSFET output current over the subthreshold region normalized with respect to the MOSFET current. **c** Corresponding percent gain of the WSe_2/$SnSe_2$ TFET over the WSe_2 FET transconductances. **d** Direct comparison of the transconductance efficiencies of the WSe_2/$SnSe_2$ heterojunction and the WSe_2 MOSFET. The TFET reaches peak transconductance efficiency close to 90 V^{-1} and outperforms the MOSFET over the entire subthreshold region.

the best figures of merit of a Tunnel FET and a MOSFET, a subthermionic subthreshold slope (dictated by a BTBT current) and a high on current (dictated by a thermionic current), respectively. The qualitative transfer characteristic of such a device is shown in red in Fig. 5a. In order to achieve such unique behavior, it is required that the TFET and MOSFET threshold voltages fulfill a particular condition, with the turn-on of the TFET before the MOSFET. In absolute values, $|V_{Th,TFET}| < |V_{Th,MOSFET}|$ for p-type devices. Here, for simplicity, we consider the TFET threshold voltage extracted as the gate bias corresponding to the 60 mV per decade slope in the transfer characteristics, called the I_{60} drain current. More precise engineering of this design condition, for the optimization of the DT FET figures of merit by taking the best of its composing device parts, would need the development of a physics-based compact model for such hybrid device, which was not the purpose of this work. For p-type devices, operated at negative gate voltages, enforcing this condition would grant that the p-type TFET controls the turn-on of the DT FET, while the pMOSFET intervenes for more negative back gate voltages providing the higher ON current.

For our fabricated devices, as discussed both in Fig. 3 and Supplementary Fig. 4, such condition is not fulfilled correctly, preventing us to match the condition for making an ideal dual-transport experimental device. Supplementary Fig. 5 shows the measured characteristic of the first experimental implementation of our DT FET based on the WSe_2/$SnSe_2$ TFET and WSe_2 FET devices whose characteristic are collected in Supplementary Fig. 4. Because of the non-ideal relationship between the devices threshold voltages, the combined transfer characteristic follows more dominantly the MOSFET rather than the TFET at the turn-on.

In order to provide an estimation of the performance of such a device in an optimal design, we used the measured experimental transfer characteristic presented in Fig. 3 and we artificially shifted the TFET threshold voltage, as potentially possible by the use of metal contacts with different work functions. The resulting transfer curve is shown in Fig. 5b. As expected, provided that $|V_{Th,TFET}| < |V_{Th,MOSFET}|$, the DT FET turns on following the heterojunction tunneling curve and inherits both a steep transition and the higher thermionic I_{ON} current of the MOSFET. Consequently, the proposed device exhibits better analog and digital figures of merit of the constituting devices. Figure 5c collects the transconductance efficiency of the three FETs: while not achieving the peak value obtained by the TFET, the DT FET exhibits a transconductance efficiency larger than the MOSFET one for the entire range of the output current, outperforming also the TFET at large drain currents. The evolution of the subthreshold slope follows a similar trend, as reported in Fig. 5d. Even if the DT FET proposed device does not reach a point subthreshold slope as small as the heterojunction TFET, it exhibits a much steeper turn on than the MOSFET and it outperforms the TFET at large current values.

The practical engineering of the WSe_2 MOSFET and WSe_2/$SnSe_2$ threshold voltages can be obtained experimentally either by (i) changing the contact metal used for one of the two devices or (ii) depositing a top dielectric and top gate contact on the WSe_2 channel[24]. This second solution, while more challenging and cumbersome from a fabrication viewpoint, it would enable the

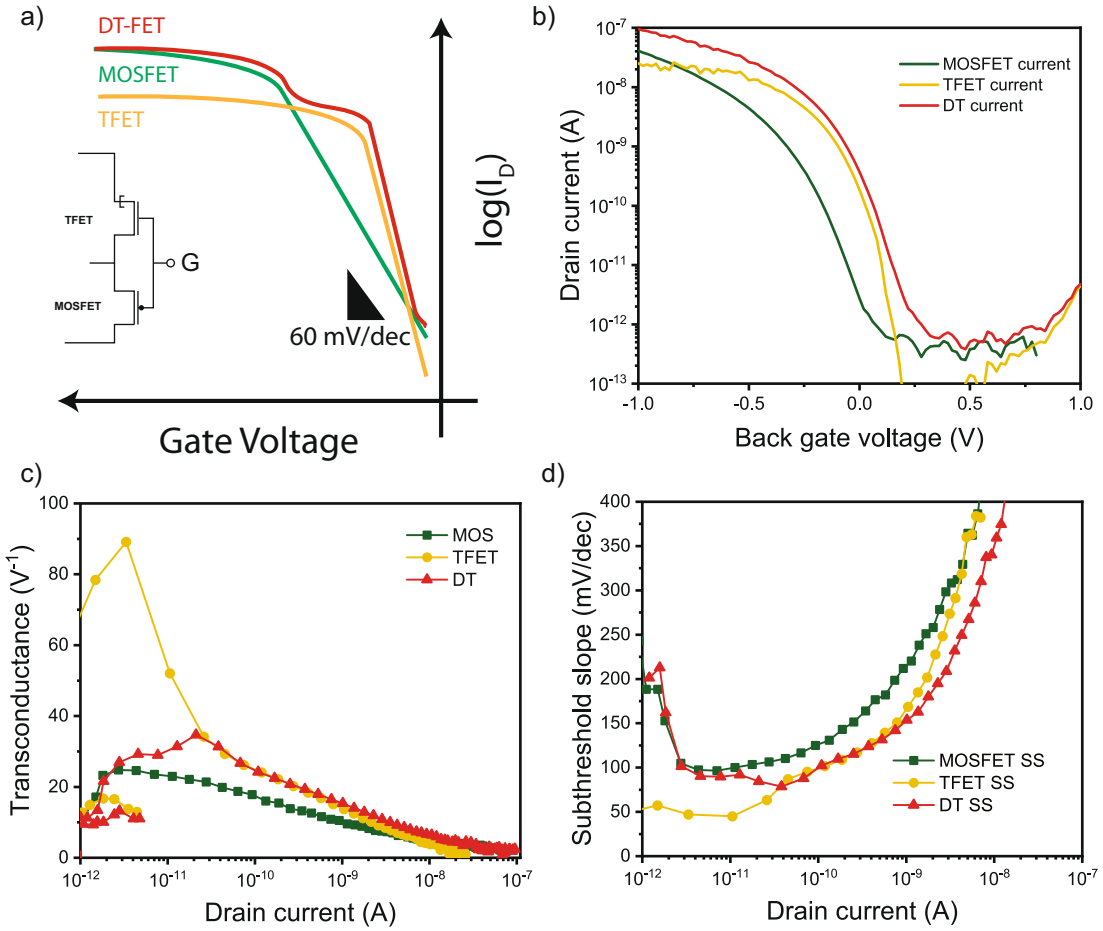

Fig. 5 Optimized dual transport (DT) steep slope FET transfer characteristic and analog/digital figures of merit. a Qualitative transfer characteristics of our 2D–2D TFET and its built-in MOSFET together with the sought after characteristic of the DT FET. Ideally, the dual transport FET should turn ON following the steep TFET curve, and then reach the thermionic I_{ON} current provided by the WSe_2 MOSFET. **b** Transfer characteristics of the WSe_2 FET and $WSe_2/SnSe_2$ TFET with optimized threshold voltages, so to obtain $V_{Th,TFET} > V_{Th,MOSFET}$. The resulting DT transfer characteristics inherits the advantages of the two devices. All the curves are measured at $V_D = 500$ mV. **c** Transconductance efficiency of the DT FET and its constituting devices. While not reaching the peak transconductance value of the $WSe_2/SnSe_2$ heterojunction, the DT FET maintains better performance of the MOSFET for all the output current range, outperforming also the TFET at large current values. **d** Direct comparison of the substhreshold slope as a function of output current for the DT FET and the base components. Similarly to the transconductance efficiency, the DT FET exhibits a minimum point subthreshold slope larger than the TFET, but it outperforms the WSe_2 MOSFET over the entire range of output current and maintains steeper characteristic than the heterojunction FET for large I_D.

possibility of programming on the fly the threshold voltage of the WSe_2 FET so to obtain the desired condition.

DISCUSSION

In this work, we reported co-integrated subthermionic 2D/2D $WSe_2/SnSe_2$ tunnel FET and WSe_2 MOSFET realized on the very same flake. The device is fabricated by deterministic assembly of the van der Waals heterojunction on top of a tungsten/HfO_2 bottom gate stack. DFT calculations confirm that this heterojunction presents an optimal broken gap band alignment, resulting in room temperature subthermionic subthreshold slope and sizeable, gate tunable negative differential resistance observable in the output characteristic. A record low point subthreshold slope of 35 mV per decade at $V_{DS} = 500$ mV has been demonstrated, while maintaining $I_{OFF} < 0.1$ pA μm^{-2} and an excellent ON/OFF current ratio exceeding 10^5. The fabricated pTFET clearly outperforms the built-in WSe_2 MOSFET, crossing its characteristic over several orders of magnitude of the drain current and providing better digital and analog performance in the subthreshold region. The demonstrated heterojunction device provides a new insight in the potential of 2D/2D systems for the realization of high performance steep-slope devices. Moreover, the possibility of cointegrating on the same flake both MOSFET and TFET with no increase in the process flow complexity paves the way to new hybrid device, such as the proposed DT FET, and circuit topologies able to harvest the steep TFET turn-on characteristic granted by the band to band tunneling conduction mechanism and the high MOSFET thermionic ON current.

METHODS

Fabrication of $WSe_2/SnSe_2$ bottom gated heterojunction devices

The starting substrate is a p doped silicon wafer. An insulation 50-nm-thick layer of HfO2 is deposited by atomic layer deposition (ALD). The bottom gate is obtained by the lift-off in acetone of 50 nm of sputtered tungsten after an electron beam lithography (EBL) step performed on a MMA/PMMA bilayer. The structure of the bottom gate is then completed by ALD of 10 nm of HfO_2. The bulk WSe_2 and $SnSe_2$ crystals were purchased respectively from hq graphene and 2D semiconductors. WSe_2 flakes are directly exfoliated by scotch taping on the final substrate, and flakes with desired geometry, thickness and position are identified by optical microscopy. $SnSe_2$ is first exfoliated on a PDMS stamp that is then used

in combination with a micromanipulator and an optical microscope to deterministically transfer SnSe2 flakes on the previously selected WSe_2 flakes. The contacts to the heterojunction devices are obtained by evaporation and lift-off of a Cr/Pd stack (5/50 nm) after a second EBL step on MMA/PMMA bilayer resist. A third EBL step is performed to pattern a PMMA mask for the low power ion beam etching of the gate dielectric in selected areas in order to gain electrical access to the bottom gate contact.

Electrical measurements

All the reported electrical measurements have been performed at room temperature and ambient conditions using conventional semiconductor parameter analyzers and electrical probes. The WSe_2 contact is always biased as the drain of the heterojunction device.

Metrology

AFM in contact mode for accurate thickness estimation and SEM have been performed after the electrical characterization, so to avoid contamination of the devices.

DATA AVAILABILITY

The raw data used in this study are available upon reasonable request to the corresponding author.

Received: 11 December 2019; Accepted: 1 April 2020;
Published online: 30 April 2020

REFERENCES

1. Moore, G. M. Moore's Law, Electronics. *Electronics* **38**, 114 (1965).
2. Meindl, J. D. Beyond Moore's law: The interconnect era. *Comput. Sci. Eng.* **5**, 20–24 (2003).
3. Yeric, G. Moore's law at 50: Are we planning for retirement? In *Technology-Design Interactions—2015 IEEE International Electron Devices Meeting (IEDM)* 111–118 (IEEE, 2015).
4. Ionescu, A. M. & Riel, H. Tunnel field-effect transistors as energy-efficient electronic switches. *Nature* **479**, 329–37 (2011).
5. Shukla, N. et al. A steep-slope transistor based on abrupt electronic phase transition. *Nat. Commun.* **6**, 2–7 (2015).
6. McGuire, F. A., Cheng, Z., Price, K. & Franklin, A. D. Sub-60 mV/decade switching in 2D negative capacitance field-effect transistors with integrated ferroelectric polymer. *Appl. Phys. Lett.* **109**, 2–7 (2016).
7. Zhang, L. & Chan, M. *Tunneling Field Effect Transistor Technology*. (Springer International Publishing: Switzerland, 2016.
8. Lu, H. & Seabaugh, A. Tunnel field-effect transistors: State-of-the-art. *IEEE J. Electron Devices Soc.* **2**, 44–49 (2014).
9. Mohata, D. K. et al. Demonstration of MOSFET-like on-current performance in arsenide/antimonide tunnel FETs with staggered hetero-junctions for 300mV logic applications. *Tech. Dig. Int. Electron Devices Meet. (IEDM)* **5**, 33.5.1–33 (2011).
10. Rosca, T., Saeidi, A., Memisevic, E., Wernersson, L. E. & Ionescu, A. M. An Experimental Study of Heterostructure Tunnel FET Nanowire Arrays: Digital and Analog Figures of Merit from 300K to 10K. In *Technology-Design Interactions—2015 IEEE International Electron Devices Meeting (IEDM)* 13.5.1–13.5.4 (IEEE, 2019).
11. Agarwal, S. & Yablonovitch, E. Band-Edge Steepness Obtained From Esaki/Backward Diode Current–Voltage Characteristics. *IEEE Trans. Electron Devices* **61**, 1488–1493 (2014).
12. Novoselov, K. S., Mishchenko, A., Carvalho, A., Neto, A. H. C. & Road, O. 2D materials and van der Waals heterostructures. *Science* **353**, aac9439 (2016).
13. Fan, S. et al. Tunable Negative Differential Resistance in van der Waals Heterostructures at Room Temperature by Tailoring the Interface. *ACS Nano* https://doi.org/10.1021/acsnano.9b03342 (2019).
14. Roy, T. et al. Dual-Gated MoS2/WSe_2 van der Waals Tunnel Diodes and Transistors. *ACS Nano* **9**, 2071–2079 (2015).
15. Xu, J., Jia, J., Lai, S., Ju, J. & Lee, S. Tunneling field effect transistor integrated with black phosphorus-MoS 2 junction and ion gel dielectric. *Appl. Phys. Lett.* **110**, 033103 (2017).
16. Nourbakhsh, A., Zubair, A., Dresselhaus, M. S. & Palacios, T. Transport properties of a MoS2/WSe2 heterojunction transistor and its potential for application. *Nano Lett.* **16**, 1359–1366 (2016).
17. Guo, Z. Independent Band Modulation in 2D van der Waals Heterostructures via a Novel Device Architecture. *Adv. Sci.* **5**, 1800237 (2018).
18. He, J. et al. 2D Tunnel Field Effect Transistors (FETs) with a Stable Charge-Transfer-Type p^+-WSe_2 Source. *Adv. Electron. Mater.* **4**, 1800207 (2018).
19. Yan, X. et al. Tunable $SnSe_2$/WSe_2 Heterostructure Tunneling Field Effect Transistor. *Small.* https://doi.org/10.1002/smll.201701478 (2017).
20. Sarkar, D. et al. A subthermionic tunnel field-effect transistor with an atomically thin channel. *Nature* **526**, 91–95 (2015).
21. Roy, T. et al. 2D-2D tunneling field-effect transistors using WSe2/SnSe2heterostructures. *Appl. Phys. Lett.* **108**, 083111 (2016).
22. Allain, A. & Kis, A. Electron and hole mobilities in single-layer WSe2. *ACS Nano* **8**, 7180–7185 (2014).
23. Resta, G. V. et al. Polarity control in WSe2 double-gate transistors. *Sci. Rep.* **6**, 6 (2016).
24. Oliva, N. et al. Hysteresis dynamics in double-gated n-type WSe2 FETs with high-k top gate dielectric. *IEEE J. Electron Devices Soc.* https://doi.org/10.1109/JEDS.2019.2933745 (2019).
25. Oliva, N., Casu, E. A., Cavalieri, M. & Ionescu, A. M. Double gate n-type WSe 2 FETs with high-k top gate dielectric and enhanced electrostatic control. *Eur. Solid-State Device Res. Conf.* https://doi.org/10.1109/ESSDERC.2018.8486867 (2018).
26. Aretouli, K. E. et al. Epitaxial 2D $SnSe_2$/2D WSe_2 van der Waals Heterostructures. *ACS Appl. Mater. Interfaces* **8**, 23222–23229 (2016).
27. Guo, C., Tian, Z., Xiao, Y., Mi, Q. & Xue, J. Field-effect transistors of high-mobility few-layer SnSe2. *Appl. Phys. Lett.* **109**, 203104 (2016).
28. Oliva, N., Capua, L., Cavalieri, M. & Ionescu, A. M. Co-integrated Subthermionic 2D/2D WSe_2/$SnSe_2$ Vertical Tunnel FET and WSe 2 MOSFET on same flake: towards a 2D/2D vdW Dual-Transport Steep Slope FET. *Electron Devices Meet. (IEDM).* https://doi.org/10.1109/iedm19573.2019.8993643 (2020).
29. Kresse, G. & Furthmüller, J. Efficient iterative schemes for ab initio total-energy calculations using a plane-wave basis set. *Phys. Rev. B Condens. Matter* **54**, 11169–11186 (1996).
30. Ernzerhof, M. & Scuseria, G. E. Assessment of the Perdew–Burke–Ernzerhof exchange-correlation functional. *J. Chem. Phys.* **110**, 5029–5036 (1999).
31. Grimme, S., Antony, J., Ehrlich, S. & Krieg, H. A consistent and accurate ab initio parametrization of density functional dispersion correction (DFT-D) for the 94 elements H-Pu. *J. Chem. Phys.* **132**, 154104 (2010).
32. Castellanos-Gomez, A. et al. Deterministic transfer of two-dimensional materials by all-dry viscoelastic stamping. *2D Mater.* **1**, 011002 (2014).
33. Oliva, N. et al. MoS2/VO2 vdW heterojunction devices: tunable rectifiers, photodiodes and field effect transistors. In *2017 IEEE International Electron Devices Meeting (IEDM)* 796–799 (IEEE, 2017).
34. Wang, Y. et al. Composition-tunable 2D SnSe2(1−x)S2x alloys towards efficient bandgap engineering and high performance (opto)electronics. *J. Mater. Chem. C.* **5**, 84–90 (2017).
35. Oliva, N., Casu, E. A., Vitale, W. A., Stolichnov, I. & Ionescu, A. M. Polarity Control of Top Gated Black Phosphorous FETs by Workfunction Engineering of Pre-Patterned Au and Ag Embedded Electrodes. *IEEE J. Electron Devices Soc.* **6**, 1041–1047 (2018).
36. Chang, H. Y., Zhu, W. & Akinwande, D. On the mobility and contact resistance evaluation for transistors based on MoS2 or two-dimensional semiconducting atomic crystals. *Appl. Phys. Lett.* **104**, 113504 (2014).
37. Enz, C., Chalkiadaki, M. A. & Mangla, A. Low-power analog/RF circuit design based on the inversion coefficient. In *ESSCIRC Conference 2015 - 41st European Solid-State Circuits Conference (ESSCIRC)* 202–208 (IEEE, 2015).
38. Barboni, L., Siniscalchi, M. & Sensale-Rodriguez, B. TFET-based circuit design using the transconductance generation efficiency {g}-{m}/ {I}-{d method. *IEEE J. Electron Devices Soc.* **3**, 208–216 (2015).
39. Subramanian, V. et al. Device and circuit-level analog performance trade-offs: A comparative study of planar bulk FETs versus FinFETs. *Tech. Dig. - Int. Electron Devices Meet. IEDM* **2005**, 898–901 (2005).
40. Girardi, A. & Bampi, S. Power constrained design optimization of analog circuits based on physical gm/ID characteristics. *J. Integr. Circuits Syst.* **2**, 22–28 (2007).
41. Chen, C. P. & Ghandi, R. Designing silicon carbide NMOS integrated circuits for wide temperature operation. In Proc. *2015 IEEE International Symposium on Circuits and Systems (ISCAS)* 109–112 (IEEE, 2015).
42. Silveira, F., Flandre, D. & Jespers, P. G. A. A gm/ID based methodology for the design of CMOS analog circuits and its application to the synthesis of a silicon-on-insulator micropower OTA. *IEEE J. Solid-State Circuits* **31**, 1314–1319 (1996).
43. Binkley, D. M., Bucher, M. & Foty, D. Design-oriented characterization of CMOS over the continuum of inversion level and channel length. *Proc. IEEE Int. Conf. Electron. Circuits, Syst.* **1**, 161–164 (2000).
44. Si, M. et al. Steep-slope WSe2 Negative Capacitance Field-effect Transistor. *Nano Lett.* https://doi.org/10.1021/acs.nanolett.8b00816 (2018).
45. Liu, W. et al. Role of metal contacts in designing high-performance monolayer n-type WSe2field effect transistors. *Nano Lett.* **13**, 1983–1990 (2013).

46. Tosun, M. et al. High-gain inverters based on WSe2 complementary field-effect transistors. *ACS Nano* **8**, 4948–4953 (2014).
47. Huang, Q. et al. A novel Si tunnel FET with 36mV/dec subthreshold slope based on junction depleted-modulation through striped gate configuration. *Tech. Dig. - Int. Electron Devices Meet. (IEDM)*. https://doi.org/10.1109/IEDM.2012.6479005 (2012).
48. Huang, Q. et al. Self-depleted T-gate Schottky barrier tunneling FET with low average subthreshold slope and high I ON/I OFF by gate configuration and barrier modulation. *Tech. Dig. - Int. Electron Devices Meet. (IEDM)*. https://doi.org/10.1109/IEDM.2011.6131564 (2011).
49. Huang, Q. et al. Device physics and design of T-gate Schottky barrier tunnel FET with adaptive operation mechanism. *Semicond. Sci. Technol.* **29**, 095013 (2014).
50. Dewey, G. et al. Fabrication, characterization, and physics of III-V heterojunction tunneling field effect transistors (H-TFET) for steep sub-threshold swing. *Tech. Dig. - Int. Electron Devices Meet. IEDM* **3**, 33.6.1–33.6.4 (2011).
51. Dewey, G. et al. III-V field effect transistors for future ultra-low power applications. *Dig. Tech. Pap. - Symp. VLSI Technol.* **14**, 45–46 (2012).

ACKNOWLEDGEMENTS

This publication has received funding from the European Research Council (ERC) under the European Union's Horizon 2020 research and innovation programme, grant agreement no. 695459, Milli-Tech.

AUTHOR CONTRIBUTIONS

N.O. and A.M.I. developed the device principle and the fabrication process flow. N.O. and L.C. worked on device fabrication. J.B. and M.L. modeled and derived the heterojunction band diagram from first principle studies. M.C. performed AFM measurements. N.O. performed electrical measurements and the data analysis. N.O., J.B., L.C., M.L. and A.M.I. wrote the manuscript.

COMPETING INTERESTS

The authors declare that they have no conflict of interest.

ADDITIONAL INFORMATION

Supplementary information is available for this paper at https://doi.org/10.1038/s41699-020-0142-2.

Correspondence and requests for materials should be addressed to N.O.

Reprints and permission information is available at http://www.nature.com/reprints

Publisher's note Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.