Z-Source Inverter for Motor Drives

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***Abstract*—This paper presents a Z-source inverter system and control for general-purpose motor drives. The Z-source inverter system employs a unique *LC* network in the dc link and a small capacitor on the ac side of the diode front end. By controlling the shoot-through duty cycle, the Z-source can produce any desired output ac voltage, even greater than the line voltage. As a result, the new Z-source inverter system provides ride-through capability duringvoltage sags, reduces line harmonics, improves power factor and reliability, and extends output voltage range. Analysis, simulation, and experimental results will be presented to demonstrate these new features.**

***Index Terms*—Line harmonics, motor drives, voltage sags, Z-source inverter.**

I. Introduction

THE TRADITIONAL general-purpose motor drive (or adjustable speed drive—ASD) system is based on the voltage-source inverter (V-source inverter), which consists of a diode rectifier front end, dc link capacitor, and inverter bridge, as shown in Fig. 1. In order to improve power factor, either an ac inductor or dc inductor is normally used. The dc link voltage is roughly equal to 1.35 times the line voltage, and the V-source inverter is a buck (or step-down) converter that can only produce an ac voltage limited by the dc link voltage. Because of this nature, the V-source inverter based ASD system suffers the following common limitations and problems.

1) Obtainable output voltage is limited quite below the input line voltage. Fig. 1 illustrates voltages of a three-phase 230-V drive system. The diode rectifier fed by the 230-V ac line produces about 310-V dc on the dc-link, which is roughly 1.35 times the line-to-line input voltage under the assumption of heavy load and continuous "double-hump" input current for large ($>$ 50 kW) drives that typically have an approximately 3% of inductance on the ac or dc side. For light load operation or small drives with no significant inductance, the line current becomes discontinuous "double-pulse," and the dc voltage is closer to 1.41 times the line-to-line input voltage (i.e., 325-V dc for a 230-V ac input). The inverter can only produce a maximum 190-V ac in the linear modulation range given the 310-V dc under the heavy load operation when the voltage is needed the most. For a 230-V motor, the low obtainable output voltage significantly limits output power that is proportional to the square of the voltage. This is a very undesirable situation for many applications because the motor and drive system has to be oversized for a required power.
2) Voltage sags can interrupt an ASD system and shut down critical loads and processes. Over 90% of power quality related problems are from momentary (typically 0.1–2 s) voltage sags of 10–50% below nominal (Fig. 2 illustrates voltage sags). The dc capacitor in an ASD is a relatively small energy storage element, which cannot hold dc voltage above the operable level under such voltage sags. Lack of ride-through capacity is a serious problem for sensitive loads driven by ASDs [1]–[6]. [6] details the vulnerability of a ASD and the dc voltage under three-phase and two phase voltage sags. Solutions have been sought to boost ride-through [2]–[6]. The ASD industry provides options using flyback converter or boost converter with energy storage or diode rectifier (Fig. 3) to achieve ride-through; however, these options come with penalties of cost, size/weight, and complexity.
3) Inrush and harmonic current from the diode rectifier can pollute the line. Low power factor is another issue of the traditional ASD system.
4) Performance and reliability are compromised by the V-source inverter structure, because 1) miss-gating from EMI can cause shoot-through that leads to destruction of the inverter, 2) the dead time that is needed to avoid shoot-through creates distortion and unstable operation at low speeds, and 3) common-mode voltage causes shaft current and premature failures of the motor.

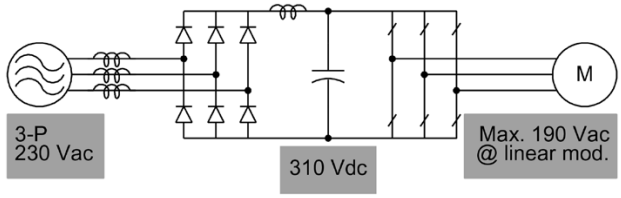

Fig. 1. Traditional variable speed drive system configuration.

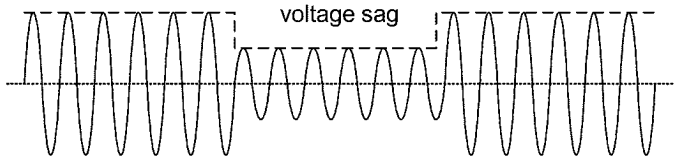

Fig. 2. Voltage sag results in dc link voltage drop and shut down.

A recently developed new inverter, the Z-source inverter [7], has a niche for ASD systems to overcome the aforementioned problems [10]. A Z-source inverter based ASD system can:

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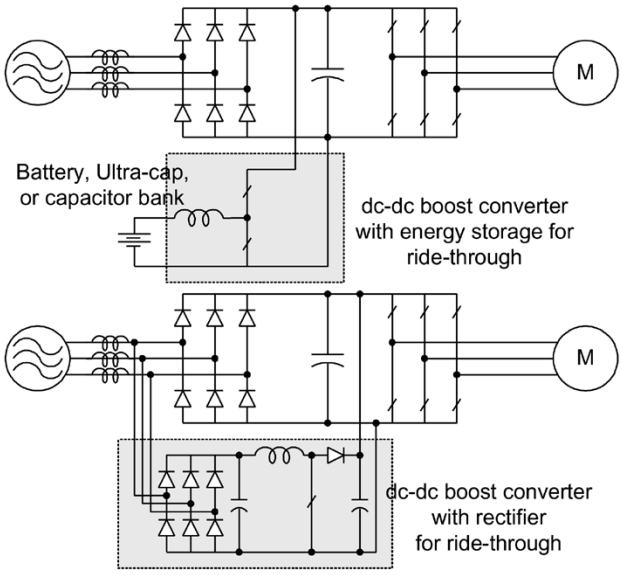

Fig. 3. Traditional variable speed drive system utilizes a dc–dc boost converter with energy storage or diode rectifier to provide ride-through.

1) produce any desired output ac voltage, even greater than the line voltage, regardless of the input voltage, thus reducing motor ratings;
2) provide ride-through during voltage sags without any additional circuits;
3) improve power factor and reduce and harmonic current and common-mode voltage.

This paper presents the Z-source inverter ASD system configuration, its equivalent circuit, analysis, and control. Simulation and experimental results are included to prove the concept and demonstrate the features of the new ASD system.

II. Z-Source ASD System

Fig. 4 shows the main circuit configuration of the proposed Z-source inverter ASD system. Similar to that of the traditional ASD system, the Z-source ASD system's main circuit consists of three parts: a diode rectifier, dc-link circuit, and an inverter bridge. The differences are that the dc link circuit is implemented by the Z-source network (C_1, C_2, L_1, and L_2) and small input capacitors (C_a, C_b, and C_c) are connected to the diode rectifier. These changes can be easily retrofitted and implemented from the traditional ASD systems. Since the Z-source inverter bridge can boost the dc capacitor (C_1 and C_2) voltage to any value that is above the average dc value of the rectifier, a desired output voltage is always obtainable regardless of the line voltage. Using the 230-V ASD system as an example, the dc capacitor voltage can be boosted to 350-V or greater in order to produce 230-V ac output regardless of the line voltage. Theoretically, the dc capacitor voltage can be boosted to any value above the inherent average dc voltage (310–325 V for a 230-V line) of the rectifier, by using shoot-through zero switching states [7] when a higher output voltage is needed or during voltage sags. The dc capacitor voltage is, however, limited by the device voltage rating in practical use.

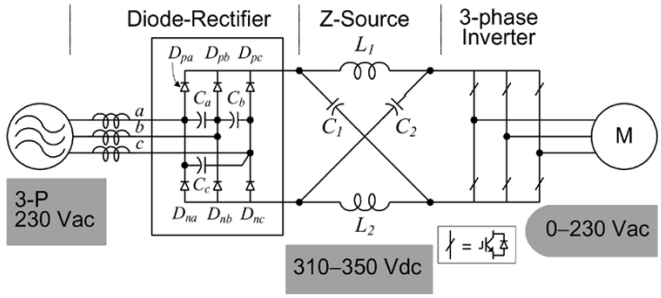

Fig. 4. Main circuit configuration of proposed Z-source inverter ASD system.

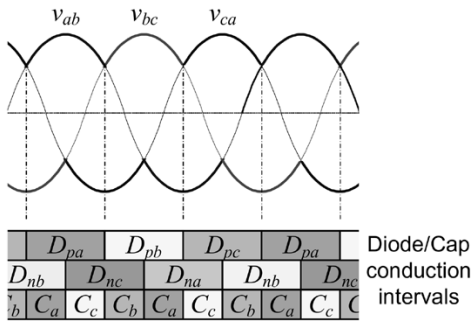

Fig. 5. Six possible conduction intervals per fundamental cycle. Each conduction interval is formed from a combination of one upper diode (D_{pa}, D_{pb}, or D_{pc}), one lower diode (D_{na}, D_{nb}, or D_{nc}), and one capacitor (C_a, C_b, or C_c).

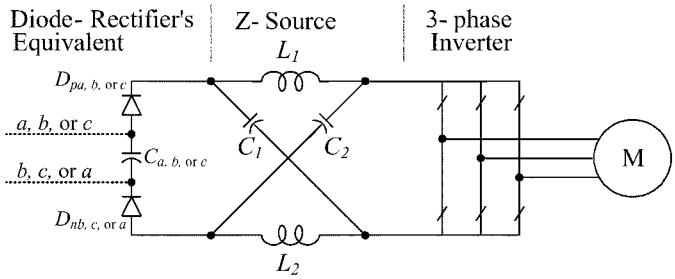

Fig. 6. Equivalent circuit of the diode bridge viewed from the Z-source network.

III. Equivalent Circuit, Operating Principle, and Control

The basic operating principle and control of the Z-source inverter fed by a dc source such as fuel cell stack have been detailed in [7]. In the proposed ASD system in Fig. 4, a diode rectifier bridge with input capacitors (C_a, C_b, and C_c) serves as the dc source feeding the Z-source network. The input capacitors are used to suppress voltage surge that may occur due to the line inductance during diode commutation and shoot-through mode of the inverter, thus requiring a small value of capacitance. At any instant of time, only two phases that have the largest potential difference may conduct, carrying current from the ac line to the dc side. Fig. 5 shows the rectifier's six possible conduction intervals per cycle. The two diodes ($D_{pa,b,}$ or $_c$ and $D_{nb,c,}$ or $_a$) conduct as a pair with the corresponding capacitor ($C_{a,b,}$ or $_c$), respectively. Therefore, as viewed from the Z-source network, the diode bridge can be modeled as a dc source in series with two diodes, as shown in Fig. 6. Note that the order of the suffixes

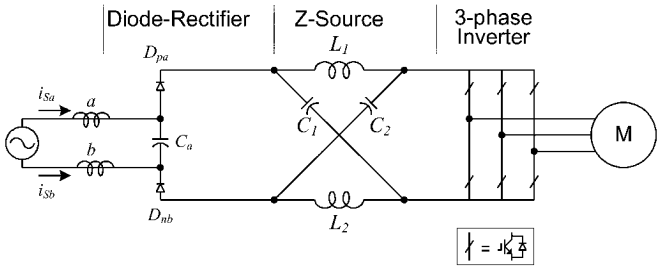

Fig. 7. Reduced circuit during the interval when the potential difference between phases "a" and "b" is the largest.

corresponds with their six combinations, e.g., D_{pa} and D_{nb} conducting as a pair with capacitor C_a, D_{pb} and D_{nc} conducting as a pair with capacitor C_b, and so on. Furthermore, the two diodes conduct in a pair and in series acting like one when viewed from the Z-source network. As a result, the proposed Z-source ASD system is reduced to the basic Z-source inverter that has been presented in [7] and illustrated in Fig. 7 of [7].

Take one interval as an example to further explain the operating principle and operating modes illustrated in Figs. 5 and 6. When the potential difference between phases "a" and "b" is the largest, diodes D_{pa} and D_{nb} conduct as a pair in series with capacitor C_a as shown in Figs. 5 and 6. The other diodes are reversely biased and cut off. Therefore, phase "c" has no line current (or a small resonant/or residual current may exist between the line impedance and capacitors C_b and C_c). Ignoring this small current in phase "c," Fig. 4 can be reduced into Fig. 7. During this interval and from this reduced circuit, there are three operation modes depending on the inverter bridge's switching state.

A. Mode I

The inverter bridge is operating in one of the six traditional active vectors, thus acting as a current source (i_i) viewed from the Z-source circuit. The diodes (D_{pa} and D_{nb}) conduct and carry currents. Fig. 8(a) shows the circuit of this mode. In the traditional ASD system, the diode bridge may not conduct depending on the dc capacitor voltage level. However, the Z-source circuit always forces diodes (D_{pa} and D_{nb}) to conduct and carry the current difference between the inductor current $(I_{Ld.})$ and inverter dc current (i_i), $(2I_{Ld} - i_i)$ as shown in Fig. 8(a). Note that both inductors have an identical current value because of the circuit symmetry. This unique feature widens the line current conducting intervals, thus reducing harmonic current.

B. Mode II

The inverter bridge is operating in one of the two traditional zero vectors and shorting through either the upper or lower three devices, thus acting as a open circuit viewed from the Z-source circuit. The diodes (D_{pa} and D_{nb}) conduct and carry currents. Fig. 8(b) shows the circuit for this mode. Again, under this mode, the two diodes ((D_{pa} and D_{nb}) have to conduct and carry the inductor current, which contributes to the line current's harmonic reduction.

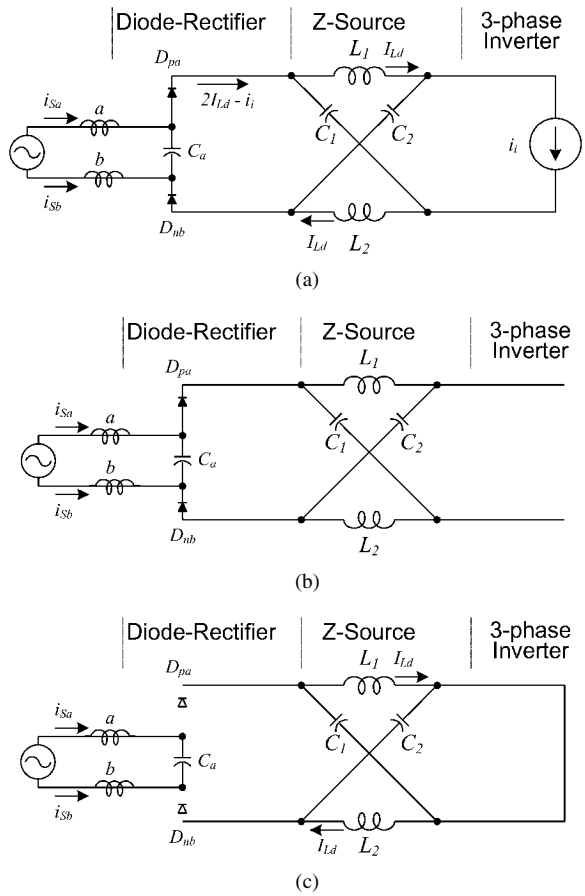

Fig. 8. (a) Mode I circuit when the inverter bridge is producing one of the six traditional active vectors. (b) Mode II circuit when the inverter bridge is producing one of the two traditional zero vectors. (c) Mode III circuit when the inverter bridge is producing one of the shoot-through states.

C. Mode III

The inverter bridge is operating in one of the seven shoot-through states. During this mode, both diodes are off, separating the dc link from the ac line. The line current flows to the capacitor (C_a). Fig. 8(c) shows the resultant circuit. This is the shoot-through mode to be used every switching cycle during the traditional zero vector period generated by the PWM control. Depending on how much a voltage boost is needed, the shoot-through interval (T_0) or its duty cycle (T_0/T) is determined [7]. It can be seen that the shoot-through interval is only a fraction of the switching cycle; therefore it needs a relatively small capacitor (C_a) to suppress voltage.

In summary, there are six diode conduction/rectification intervals per line cycle that are determined by the line side voltage; each interval has three operation modes that are determined by the inverter bridge's switching states. There are a total of 15 switching states: six traditional active states, two traditional zero states, and seven shoot-though states. The shoot-through switching states provide both challenges and opportunities in terms of PWM control. A simple PWM control for the Z-source inverter bridge was proposed in [7] and more sophisticated control methods can be found in [8] and [9]. The following paragraph will describe the shoot-through operation in more detail and provide a summary of the theoretical relationships.

The operating principle and control of the Z-source inverter itself have been detailed in [7]. The traditional three-phase V-source inverter has six active states in which the dc voltage is impressed across the load and two zero states, in which the load terminals are shorted through either the lower or upper three devices, respectively. However, the three-phase Z-source inverter bridge has additional zero states when the load terminals are shorted through both the upper and lower devices of any one phase leg (i.e., both devices are gated on), any two phase legs, or all the three phase legs. These shoot-through zero states are forbidden in the traditional V-source inverter, because it would cause a shoot-through. There are seven different shoot-through states: three shoot-through states via any one phase leg, three shoot-through states from combinations of any two phase legs, and one shoot-through state by all the three phase legs. The shoot-through zero states boost dc capacitor voltage while producing no voltage to the load. It should be emphasized that both the shoot-through zero states and the two traditional zero states short the load terminals and produce zero voltage across the load, thus preserving the same PWM properties and voltage waveforms to the load. The only difference is the shoot-through zero states boost the dc capacitor voltage, whereas the traditional zero states do not. For the proposed ASD system, the three-phase inverter bridge is controlled the same way as the traditional PWM inverter without shoot-through when a desired output voltage is less than 190-V ac, which is the maximum voltage obtainable from 230-V line using the linear region PWM. The diode rectifier produces about 310 V across the dc capacitors (C_1 and C_2). When a higher output voltage is required or when the line voltage is experiencing sags, the shoot-through zero states are employed to boost the dc capacitor voltage. The longer time the shoot-through zero states are used, the higher voltage one gets. By controlling the shoot-through zero state interval, a desired dc voltage can be maintained. All the relationships described in detail in [7] about the dc capacitor voltage, shoot-through time interval (or duty cycle), and output voltage hold true for the proposed ASD system. These relationships are summarized as

$$V_{C1} = V_{C2} = V_C = \frac{1 - \frac{T_0}{T}}{1 - 2\frac{T_0}{T}} V_0 = \frac{B+1}{2} V_0$$

$$\hat{v}_{ac} = MB\frac{V_0}{2}, \quad B = \frac{1}{1 - 2\frac{T_0}{T}}, \quad \text{and}$$

$$V_0 = \frac{3\sqrt{2}}{\pi} V_{\mathrm{LL}} = 1.35\, V_{\mathrm{LL}}$$

where V_{C1} and V_{C2} are voltages across the dc capacitors, C_1 and C_2, respectively, and have an equal value because of the symmetry of the circuit. T_0 is the shoot-through interval over one switching cycle, T. $\hat{v}_{\mathrm{ac}}$ is the peak phase voltage produced by the inverter. B is the boost factor and M is the modulation index of the inverter. V_0 is the inherent dc voltage of the rectifier fed from the line with a line-to-line rms value of V_{LL}, assuming that voltage drop on the line impedance is negligible. In addition to the above equations, it should be noted that the equivalent dc voltage across the inverter bridge, V_{dc} is different from the dc capacitor voltage, V_{C1} or V_{C2} when the boost factor is greater than 1. V_{dc} is expressed as

$$V_{\mathrm{dc}} = BV_0 = \frac{2B}{B+1} V_C.$$

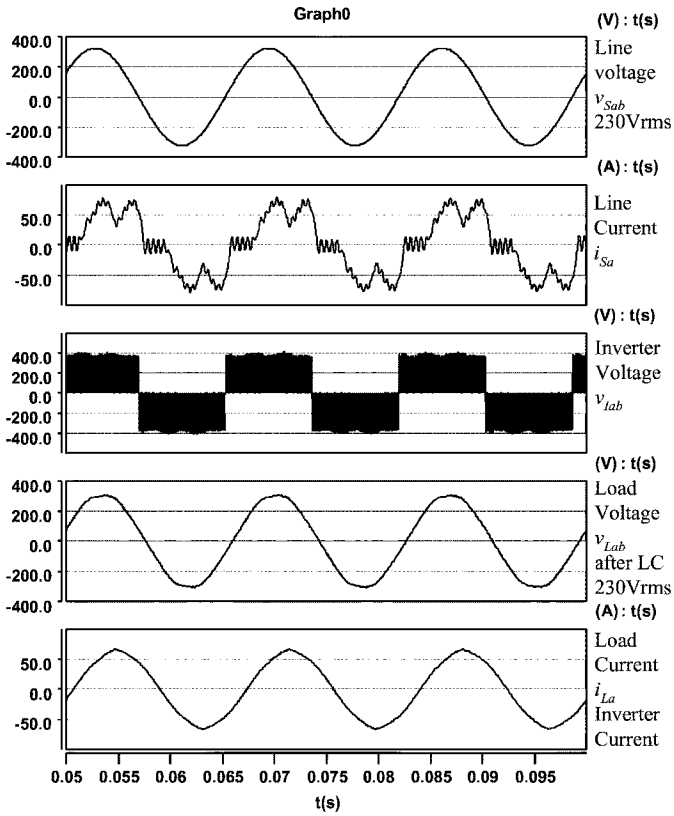

Fig. 9. Simulation waveforms showing line and load voltages and currents under the nominal line voltage, 230 Vac.

IV. Simulation and Experimental Verification of the Z-Source ASD System

To confirm the operating principle of the new ASD system, simulations have been carried out and a 20-kVA prototype has been built. In order to show clearly the output voltage obtained from the inverter, an *LC* filter with 1-kHz cutoff frequency is placed in between the inverter bridge and the motor. The simulation and experimental system are setup with the following parameters.

1) Three-phase line voltage: 230 V, line impedance: 3%.
2) Load: three-phase 230-V 20-KW induction motor.
3) Input capacitors (C_a, C_b, and C_c): 10 μF;
4) Z-source network: $L_1 = L_2 = 160$ μH, $C_1 = C_2 = 1000$ μF.
5) Switching frequency: 10 kHz.

Figs. 9 and 10 show simulation waveforms under the nominal line voltage of 230-V ac. The inverter modulation index was 1.0, producing the same PWM waveform (V_{Iab}) as the traditional inverter. However, the magnitude of the output voltage was boosted to 230 V rms and was confirmed by the sinusoidal waveform (V_{Lab}) after the 1-kHz LC filter. The traditional PWM inverter cannot produce 230 V rms output voltage. Fig. 10 shows

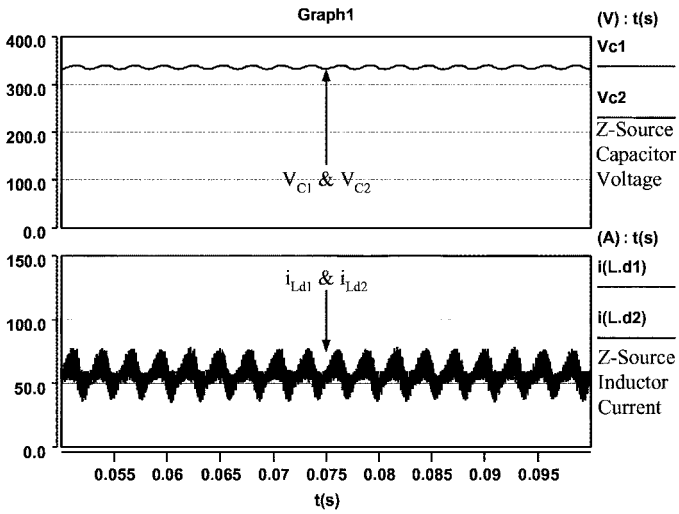

Fig. 10. Simulation waveforms of Z-source capacitor voltage and inductor current under the nominal line voltage.

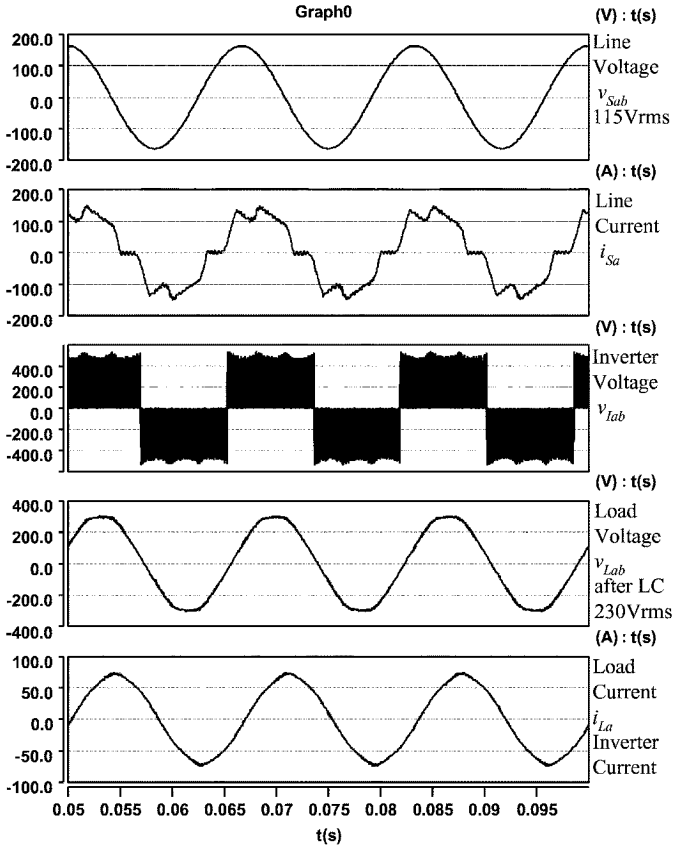

Fig. 11. Simulation waveforms showing line and load voltages and currents under 50% voltage sag.

the inductor current and dc capacitor voltages, which have been boosted to 343 V. Note that the traces of V_{C1} and V_{C2} coincided with each other and so did the two inductor currents L_{d1} and L_{d2}. The equivalent dc voltage across the inverter bridge, V_{dc} was boosted to 376 V (which was confirmed from the line-to-line inverter voltage shown in Fig. 9) and should be limited

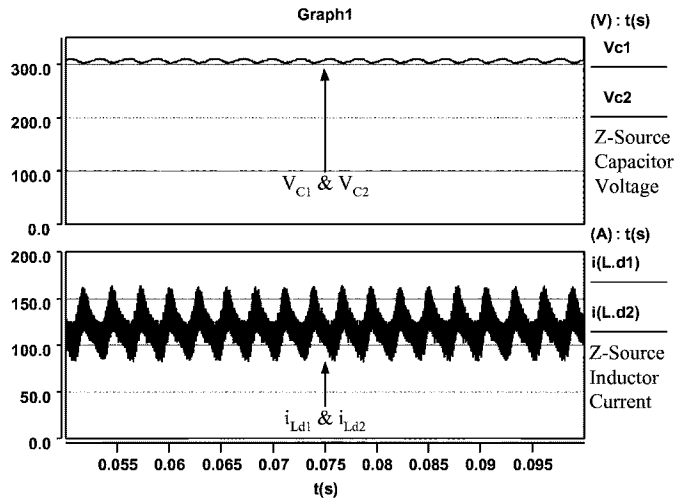

Fig. 12. Simulation waveforms showing Z-source network capacitor voltage and inductor current under 50% voltage sag.

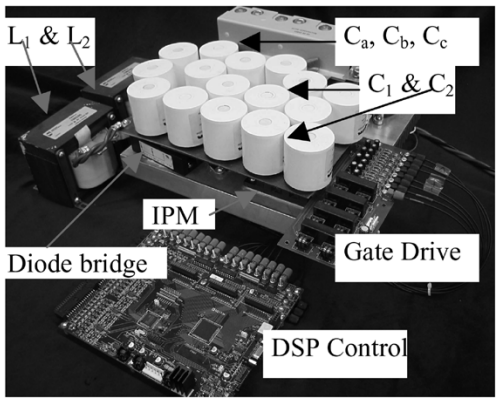

Fig. 13. Prototype of the Z-source ASD system.

below the device voltage rating, which is 450 V for the 600-V IPM. The boost factor B was 1.21. Also, it is noted that the line current contains much less harmonics than the traditional ASD system without dc inductors and appreciably less harmonics than the traditional ASD system even with dc inductor because of both the Z-source inductors and input capacitors. Figs. 11 and 12 show simulation waveforms during 50% voltage sag (the line voltage drops to 115 V ac). The waveforms clearly demonstrate that the dc capacitor voltage can be boosted and maintained to a desired level, which in this case is above 300 V. The boost factor was 2.8 at a modulation index of 0.82. Again, the line current harmonics have been reduced greatly.

A prototype has been built to further verify the operation, theoretical relationships of voltage boost, and simulation results of the presented Z-source ASD system. Fig. 13 shows a photo of the system. It should be noted that the inductors and capacitors were oversized in the prototype for possible regenerative operation during deceleration or inverter trips. The requirement of Z-source network has been discussed in [7], which should not differ much from the traditional drives. For large (50 kW or above) drives, a dc inductor is commonly used to minimize line harmonic current and voltage distortion. The inductor used in the Z-source has the similar effect on the line current harmonic

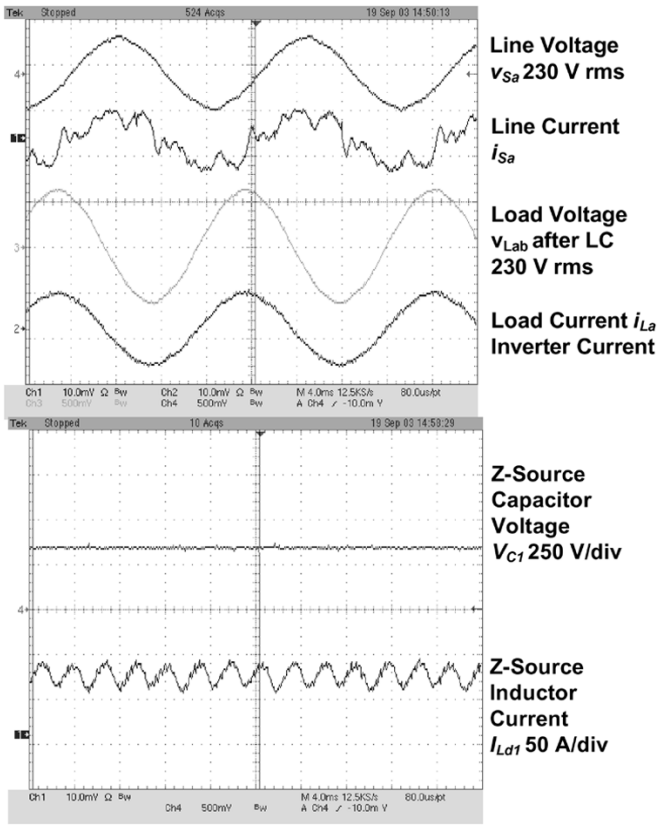

Fig. 14. Experimental waveforms under the nominal line voltageof 230 Vac.

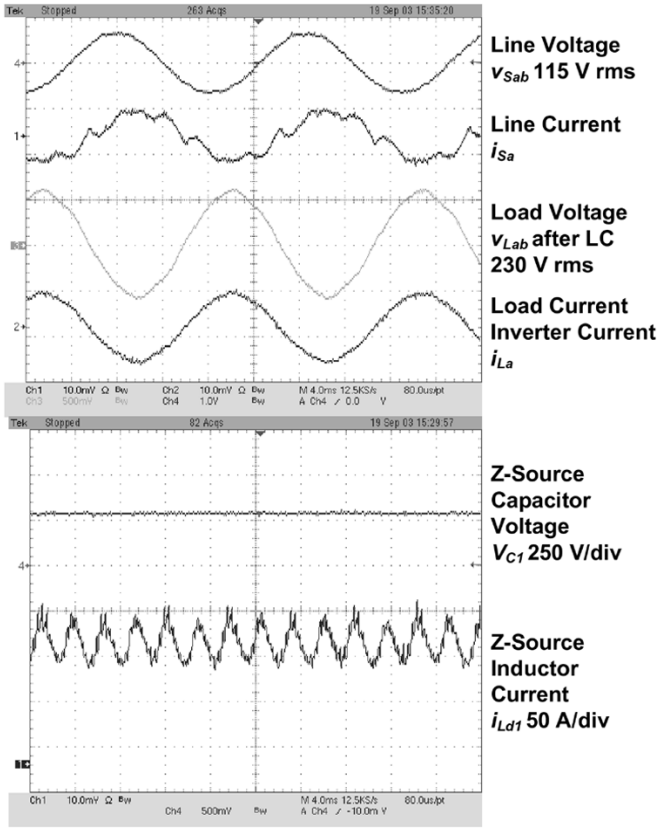

Fig. 15. Experimental waveforms under 50 % voltage sag.

reduction, which was confirmed in the above simulation results. For a motor drive system, the required dc capacitance is relatively small for a tolerable voltage ripple mainly resulted from rectification. The dc capacitance should be sized for possible regenerative operation.

Fig. 14 shows experimental waveforms under the nominal line voltage of 230-V rms with the same conditions as the simulation shown in Figs. 9 and 10. Again, the inverter produced a 230-V rms value, by boosting the dc capacitor voltage to 343 V. The dc voltage across the bridge was boosted to 376 V with a boost factor of 1.21. Also, it can be seen that the line current contains much less harmonics than the traditional ASD without dc inductors, although the wave shape is different from the simulation. This is because the line voltage is distorted in the lab, which was not considered in the simulation.

Fig. 15 shows experimental waveforms during 50% voltage sag (the line voltage dropped to 115-V rms), the same conditions as in the simulation of Figs. 11 and 12. The waveforms clearly demonstrate that the dc capacitor voltage can be boosted and maintained to a desired level, which is above 300 V. It can be confirmed from the results that the boost factor was 2.8 and the modulation index was 0.82.

V. Conclusion

This paper has presented a new ASD system based on the Z-source inverter. The operating principle and analysis have been given. Simulation and experimental results verified the operation and demonstrated the promising features. In summary, the Z-source inverter ASD system has several unique advantages that are very desirable for many ASD applications, it

1) can produce any desired output ac voltage, even greater than the line voltage;
2) provides ride-through during voltage sags without any additional circuits and energy storage;
3) minimizes the motor ratings to deliver a required power;
4) reduces in-rush and harmonic current.

Acknowledgment

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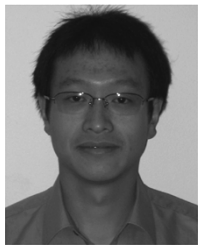
His current research is on FACT's devices, multilevel converters, dc-dc converters, and DSP inverter control.



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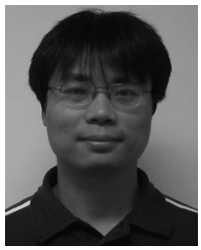

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