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# Zero-Crossing-Based Ultra-Low-Power A/D Converters

*A/D converters that can immediately detect when the input voltage is zero, promise greatly reduced power consumption and elimination of gain and stability concerns.*

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**ABSTRACT** | Since the first demonstration of a comparator-based switched-capacitor circuit, analog-to-digital (A/D) converters based on virtual ground detection have made steady and significant progress. Comparators have been replaced by zero-crossing detectors, leading to the development of zero-crossing based circuits for faster speed and lower power. All facets of performance including the sampling rate, effective number of bits, noise floor, and figure-of-merit have improved substantially. This paper focuses on recent implementations of zero-crossing based A/D converters and discusses the technical issues unique to these A/D converters as well as solutions that have been developed to improve their performance and practicality. A series of prototype designs whose performance ranges from 8 bit, 200 MS/s to 12 bit, 50 MS/s are described. The ultimate low power potentials of these A/D converters are compared with various different types of complementary metal-oxide-semiconductor A/D converters from a fundamental thermal noise standpoint.

**KEYWORDS** | A/D converter; data conversion; mixed signal

## I. INTRODUCTION

The explosive growth of portable electronic systems such as cellular phones, laptop computers, and digital music

players, among many others, has made power consumption one of the most important performance parameters in electronic circuits. The size and weight of batteries is an important consideration in portable electronics. In contrast to the advances in electronic circuits, battery technology has progressed at a much slower pace, making low-power circuit design critical. Therefore, circuit and system design for low power consumption has received increasing attention in recent years. A vast stride has been made in lowering power consumption and improving performance and functionality simultaneously. Such progress has been made predominantly in digital circuits and systems through the combination of low-power design techniques and fabrication technology scaling.

Most real-world signals such as sound and images are analog signals. Microphones and image sensors convert these signals initially to analog signals. Signals used in data storage and wired and wireless communication are also mostly analog even if the data encoding is digital. Sensors that convert pressure, acceleration, temperature, magnetic field, and other mechanical and environmental signals generally first produce analog signals. Analog circuits are used to amplify, process, and filter analog signals and convert them to digital signals, or vice versa, so that the real world and electronic devices can communicate with each other. Therefore, analog circuits are an essential part of most electronic systems. Unfortunately, low-power analog design has enjoyed only limited success, primarily through clever circuit design techniques. This is because the technology development has focused on digital circuits, rendering both active and passive devices inadequate for analog functions. Lower power-supply voltages have made the analog circuit design even more difficult to

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maintain the signal-to-noise ratio (SNR). For this reason, analog circuits are rapidly becoming the bottleneck in power consumption. Many functions that were traditionally implemented in analog circuits—for example, filtering, modulation, and demodulation—are now pushed to the digital domain to alleviate the analog bottleneck. However, this trend increases the performance demand on analog-to-digital converters (ADCs), which are analog circuits themselves.

In order to address ultra-low-power design for the high-performance ADCs that are demanded of modern electronics systems, we have developed a new ADC architecture based on zero-crossing detection. We shall first review the state-of-the-art in ADC technology to provide a rationale for the new architecture. Although ADCs built in compound semiconductor technologies can achieve ultra-high speed, high current levels are required to bias the devices in optimum speed region. In addition, they are not compatible with digital complementary metal-oxide-semiconductor (CMOS) circuits that can provide subsequent signal processing including digital calibration. For these reasons, we will focus on ADCs in CMOS technologies.

Traditionally, operational amplifiers (op-amps) have been widely used in high-performance analog circuits. Op-amp based circuits trade the large open-loop gain for robustness in critical circuit parameters via negative feedback. These circuits typically offer excellent linearity and precisely controlled circuit parameters that depend only on ratio matching of components, primarily, capacitors. Switched capacitor and continuous-time filters, most pipeline and cyclic ADCs, most voltage-output digital-to-analog converters, delta-sigma modulators, instrumentation, and programmable gain amplifiers have been built with op-amps for many decades [1]–[4].

The two most important properties required from op-amps are high open-loop gain and stability under negative feedback. These requirements often conflict with each other and pose difficult challenges for the implementation of op-amps in deep submicrometer technologies. In addition, the op-amp must have high closed-loop bandwidth and settle fast. The nondominant poles must be pushed out to high frequencies to achieve high bandwidth and stability simultaneously. These requirements make op-amp based circuits power inefficient. Moreover, technology scaling makes the realization of op-amps more difficult due to the reduced signal swing and the decrease in intrinsic device gain. Cascoded amplifier stages have been a popular solution to increase amplifier gain, but they further reduce the signal swing. Special high-gain devices have been developed to achieve high intrinsic gain for a power efficient op-amp based pipeline ADC [5]. However, such devices require additional processing steps to standard CMOS technologies.

High-speed ADCs typically have a flash architecture in which the input voltage is compared with each of the  $2^N$  tap

voltages simultaneously. The flash architecture, however, becomes impractical at resolutions over 8 bits due to the large number of comparators required. For example, a 12 bit flash converter would require 4095 comparators. The power consumption and the input capacitance from such a large number of comparators are impractically large. Folding/interpolating converters [6]–[8] significantly reduce the number of comparator preamplifiers compared to flash converters. These converters are well suited for high-speed and low-to-medium resolution applications but are still hardware and power intensive.

Capacitor array based successive approximation ADCs and their variants [9], [10] are power efficient because no op-amps are required. Due to the number of comparator decisions required per conversion, achieving high speed and high resolution simultaneously is challenging. Redundant coding can alleviate this problem at the cost of added complexity [10]. The capacitor array in successive approximation ADCs typically presents a large input capacitance, and the input buffer may consume a large amount of power, often many times greater than the ADC itself. Successive approximation is limited to A/D conversion and cannot be extended to other signal processing applications such as filtering, amplification, or delta-sigma modulation.

Pipeline converters are power efficient and are appropriate for medium to high resolution (10–16 bits) and medium to high bandwidth (1–100 MHz) applications [11]. Time-interleaving can greatly increase the frequency range of pipeline converters up to the GHz range [12]. Pipeline converters also can be configured to partial pipeline or algorithmic topologies for smaller area and lower power at the cost of the sampling rate. Delta-sigma converters are suitable for high-resolution (12 to more than 20 bits), low-to-medium bandwidth (kilohertz to megahertz) applications. Most such ADCs rely on op-amps in their operation.

There are a number of alternative circuit architectures that avoid op-amps. Open-loop amplification is a technique for pipeline ADCs whereby the residue voltage of each stage is generated by an open-loop amplifier. While more power efficient than op-amp based circuits, the open-loop amplification does not enjoy the robustness that op-amps provide. The gain error and nonlinearity of the open-loop amplification are removed through sophisticated digital calibration [13]. Charge-coupled devices (CCDs) provide accurate transfer, addition, and subtraction of charge [14]. The compatibility with scaled CMOS technologies is improved with bootstrapped bucket-brigade devices instead of CCDs [15]. The dynamic amplifiers [16]–[18] are not fundamentally different from op-amp circuits in that there is an explicit analog feedback loop. The difference is that the bias current of the amplifier is reduced as the output settles. However, they do not avoid the classic tradeoff between speed and settling accuracy in op-amp circuits. In fact, the output never fully settles in [16] or [17] because

the bias current gets ever so small as the amplifier settles. Thus, there is a more severe tradeoff between speed and accuracy. Maintaining a small dc bias current in the dynamic amplifier overcomes this issue, which is essentially an implementation of a class AB operational amplifier [18].

As an alternative to op-amp based circuits, comparator based switched-capacitor (CBSC) circuits were developed [19]. This was based on the observation that an accurate output voltage is necessary only at the sampling instant of the next sampling circuit. In conventional sampled-data circuits, an op-amp drives its inverting input to virtual ground. In a CBSC circuit, the op-amp is replaced by a comparator. The comparator detects the instant the inverting input crosses virtual ground. The comparator output is used to determine the sampling instant. Despite the different transient response, the same final output is sampled as the op-amp based circuit. The comparator only detects the virtual ground crossing rather than forcing virtual ground; thus it is more power efficient than an op-amp. The CBSC circuits offer compatibility with most switched-capacitor circuits, including pipeline ADCs, delta-sigma modulators, switched-capacitor filters, and programmable gain amplifiers without compromising the robustness op-amps provide—for example, key circuit parameters and linearity being determined by capacitor ratios.

In this paper, we focus on zero-crossing based (ZCB) circuits that are extensions of CBSC circuits but are potentially more power efficient and operate faster [20]–[22]. Voltage comparators are designed to compare two arbitrary voltage waveforms. Since the comparator in a CBSC circuit effectively determines the zero-crossing instant where the input voltage is a constant ramp, the circuit can be simplified by replacing the comparator with a zero-crossing detector.

## II. ZERO-CROSSING BASED CIRCUITS

### A. Single-Ended ZCB Circuit Implementation: Lowest Power and High Speed

Since only the zero-crossing detection function is needed from the threshold detection comparator in a CBSC circuit, the comparator can be replaced by a zero-crossing detector (ZCD). A dynamic inverter shown in Fig. 1 can be employed as a ZCD [20]. Initially, the output voltage  $V_P$  of the ZCD is charged up to  $V_{DD}$ . When the voltage ramp input voltage  $V_X$  approaches the threshold

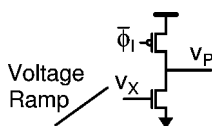


Fig. 1. Dynamic inverter as a zero-crossing detector.

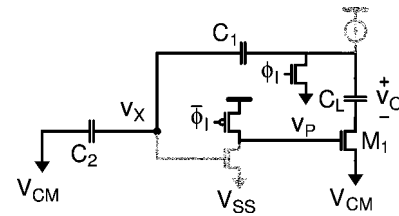


Fig. 2. One complete stage of the dynamic ZCD-based pipeline ADC.

voltage of the NMOS transistors,  $V_P$  drops rapidly, performing effective zero-crossing detection.

In the dynamic ZCD, power is consumed only during the critical time when the input crosses virtual ground and the output makes the transition. Thus, the dynamic ZCD-based circuits are extremely power efficient without compromising speed. The ZCB circuit offers unique opportunities for using dynamic circuits for highly power-efficient analog functions. Originally, a dual-phase charge transfer was devised in order to improve the power efficiency and accuracy of the CBSC circuits. However, the fact that the dynamic ZCD has no static power consumption obviates the need for the dual phase, enabling faster operation. A single-phase charge transfer is very fast and provides adequate accuracy for applications requiring accuracy of 8 bits or less.

Fig. 2 shows the complete schematic diagram of one stage of a pipeline ADC based on the dynamic ZCD. The input voltage is sampled on  $C_1$  and  $C_2$  during the sampling phase. Shortly before the transfer phase, the ZCD output  $V_P$  is precharged to  $V_{DD}$ , and the output voltage  $V_O$  is discharged to ground by pulsing  $\phi_1$  high briefly. The current source is then applied in a manner similar to the CBSC operation to produce a ramp waveform at the output. At the instant the input node voltage  $V_X$  crosses the threshold of the ZCD, its output voltage  $V_P$  drops rapidly. This output is used to turn off the sampling switch  $M_1$  of the next stage, thereby determining the sampling instant. The dynamic ZCD is very power efficient because it consumes no dc power. The ZCD is also extremely fast, with a typical switching delay of about 100 ps or less, depending on the technology and the input ramp rate.

It must be pointed out that the dynamic ZCD is unsuitable as a general-purpose voltage comparator since the switching threshold depends on the input waveform. The threshold will vary on a sample-to-sample basis if an arbitrary input waveform is applied. However, the constant-rate ramp waveform in a zero-crossing based circuit ensures a constant switching threshold.

The ZCD consumes only  $CV^2f$  power, just like digital gates. Although the current sources are used to generate the ramp waveform, they only dissipate dynamic power for the capacitor network.

One drawback of the dynamic ZCD is that the threshold is a function of the ramp rate, process, and

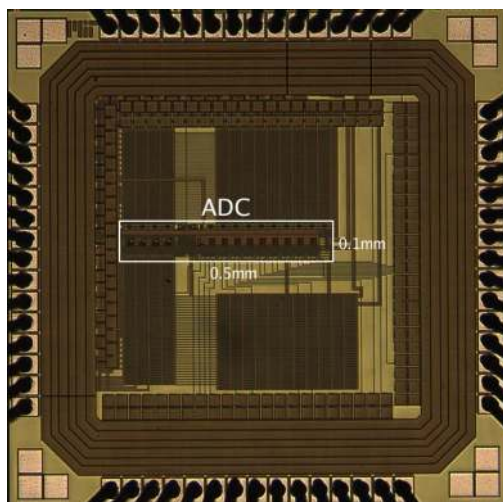


Fig. 3. Die photograph single-ended ZCB pipeline ADC.

temperature. For this initial design, an autozeroing circuit to null these dependencies was not implemented. For practical circuits, autozeroing techniques, similar to offset cancellation in op-amp circuits, must be developed.

An 8 bit prototype pipeline ADC was implemented in a 0.18  $\mu\text{m}$  CMOS technology in an active die area of 0.05  $\text{mm}^2$  (Fig. 3). The measured differential nonlinearity (DNL) is  $\pm 0.5/\pm 0.7$  LSB and the integral nonlinearity (INL) is  $\pm 0.75/\pm 1.0$  LSB at 100 and 200 MS/s, respectively, at 8 bits. The signal-to-noise-plus-distortion ratio (SNDR) and the spurious-free dynamic range (SFDR) are measured to be 41.5/38.5 and 60/55 dB, respectively. The measured effective number of bits (ENOBs) at the Nyquist input frequency is 6.9 and 6.4 bits, respectively. The power consumption is 4.5/8.5 mW from a 1.8 V supply, 2/3 of which is attributed to digital circuits. The corresponding figure of merit (FOM) is 0.38 pJ/step at 100 MS/s and 0.51 pJ/step at 200 MS/s. The limitation in the ENOBs is believed to be caused by noise coupling from the digital inputs/outputs (I/Os).

Fig. 4 shows the signal-to-noise ratio (SNR) as a function of the I/O supply voltage. The degradation of SNR with increasing I/O supply voltage is a strong indication of the noise coupling through ground and substrate. Strategic placement of on-chip decoupling capacitors on power supplies and voltage references may improve the performance significantly. The summary of the performance at 100 and 200 MS/s is shown in Table 1.

### B. Dual Phase Differential ZCB Circuit: Improved Accuracy and Power Supply Rejection

For accuracy of 10 bits and higher, a differential signal path is strongly preferred for better power supply and substrate noise rejection. A differential ZCD can be constructed from a differential preamplifier driving a dynamic threshold detector much like the dynamic ZCD

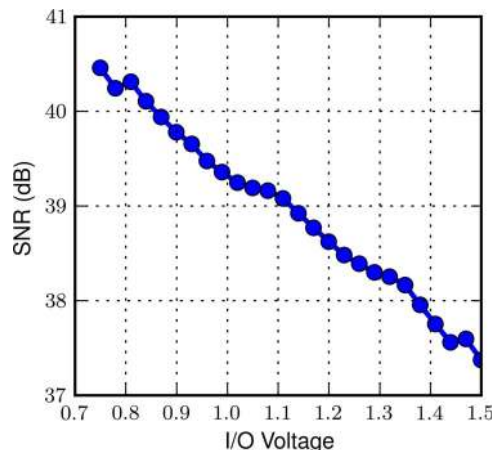


Fig. 4. Measured SNR versus I/O supply voltage.

described in the previous section. The drawback of such an implementation is the reduced power efficiency due to the constant bias current in the preamplifier. A dynamic biasing or duty cycling of the preamplifier can be employed to improve the power efficiency, as described in the next section. In this design, a dual-phase operation similar to that used in the first CBSC circuit is implemented for improved power efficiency. The dual-phase operation also improves linearity.

Table 1 Single-Ended ZCB Pipeline ADC Summary of Performance

<b>Technology</b>	0.18 $\mu\text{m}$ CMOS
<b>Supply Voltage</b>	1.8 V
<b>Resolution</b>	8 bits
<b>Sampling Rate</b>	100/200MS/s
<b>Full-Scale Input</b>	1V (single-ended)
<b>Die Area</b>	0.05 $\text{mm}^2$
<b>Power Consumption</b>	4.2/8.5mW
<b>DNL</b>	$\pm 0.5/\pm 0.7$ LSB
<b>INL</b>	$\pm 0.75/\pm 1$ LSB
<b>SFDR</b>	60/55dB
<b>SNDR</b>	41.5/38.5dB
<b>ENOB</b>	6.9/6.4b
<b>FOM</b>	0.38/0.51pJ/step

The first fully differential ZCB pipeline ADC consists of nine pipelined 1.5 bit stages for 10 bit resolution [20]. For simplicity of the design, Stages 2–9 are made identical. Stage 1 is made twice as large and has twice the current level for lower noise. The schematics of the fully differential ZCB pipeline stages are shown in Fig. 5. Current sources  $I_1$  and  $I_2$  are for the coarse and the fine phases, respectively.

The timing diagram is shown in Fig. 6. The input voltage is sampled and held on  $C_1, C_2, C_3,$  and  $C_4$  on the falling edge of  $Q_1$  prior to the beginning of charge-transfer phase (the rising edge of  $Q_2$ ). A short preset signal  $P$  presets the true output  $OUTT$  to GND and the complementary output  $OUTC$  to  $V_{DD}$  through  $SW_1$  and  $SW_2$ . This ensures that the differential input to the ZCD is always negative at the start of the coarse phase. After the preset, the coarse charge-transfer phase begins. The coarse current sources labeled  $I_1$  charge  $OUTT$  and discharge  $OUTC$  at a fast rate until the ZCD inputs  $V_x$  and  $V_y$  cross each other. At this point, the ZCD makes its first decision. Due to the finite delay of the ZCD, current sources  $I_1$  are turned off shortly after  $V_x$  crosses  $V_y$ . The fast ramp rate

and the finite delay in the ZCD causes overshoot during the coarse phase. In the previous CBSC circuit, the overshoot was corrected by a variable comparator threshold [21]. Since it is not straightforward to change the switching threshold of the fully differential ZCD, a switched-capacitor overshoot correction circuit has been developed. The overshoot correction capacitors  $C_{O1-2}$  are charged to a predetermined voltage during the coarse phase, and the charge on  $C_{O1-2}$  is subtracted from  $C_1, C_2, C_3,$  and  $C_4$  at the end of the coarse phase. This reduces the coarse phase overshoot and maximizes the time for the fine phase for lower noise bandwidth and higher power efficiency without affecting the accuracy of the fine charge transfer.

During the coarse phase, a switched-capacitor common-mode feedback (CMFB) similar to that in fully differential op-amps is engaged to maintain a constant output common-mode. The CMFB is engaged only during the coarse phase because the output voltage changes are small in the fine phase, causing negligible common-mode variation. After the current sources  $I_1$  turn off at the end of the coarse phase, fine current sources  $I_2$  turn on to begin the fine charge-transfer phase. The current  $I_2$  is approximately an

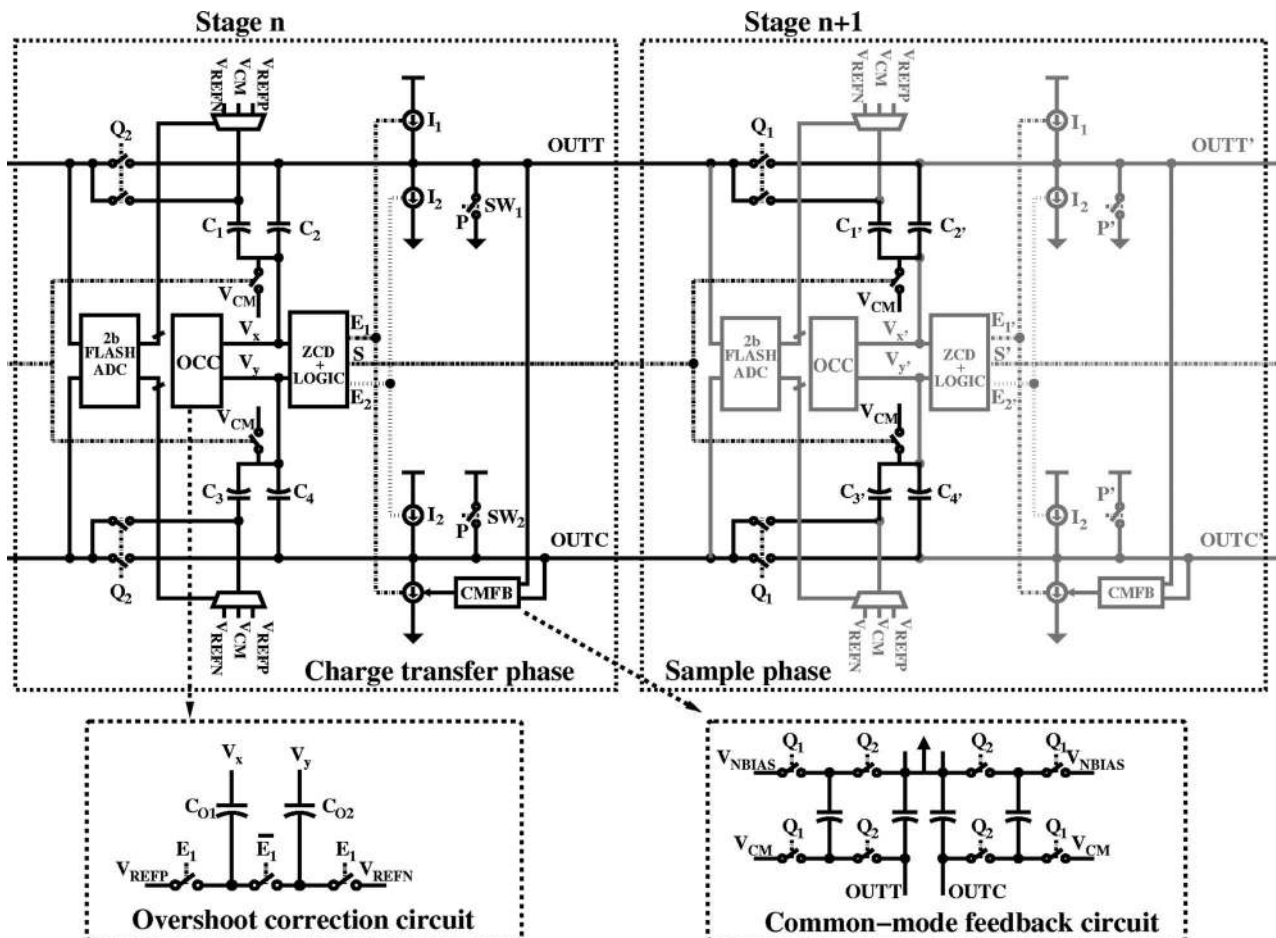
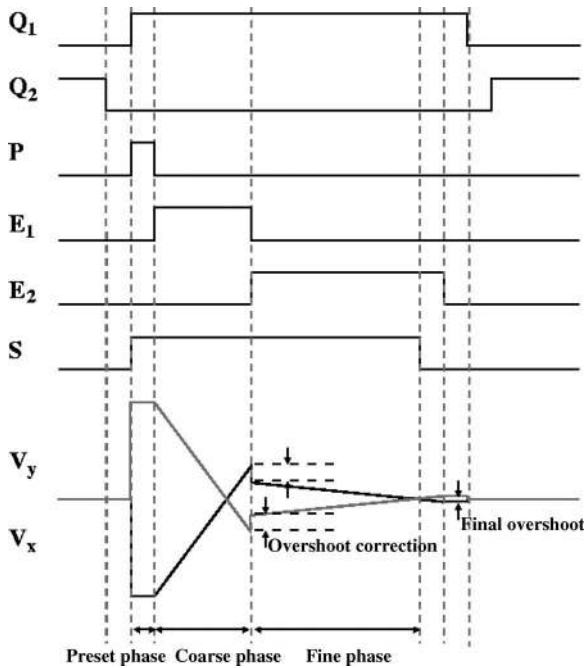


Fig. 5. Two adjacent stages of fully differential ZCB pipeline ADC.

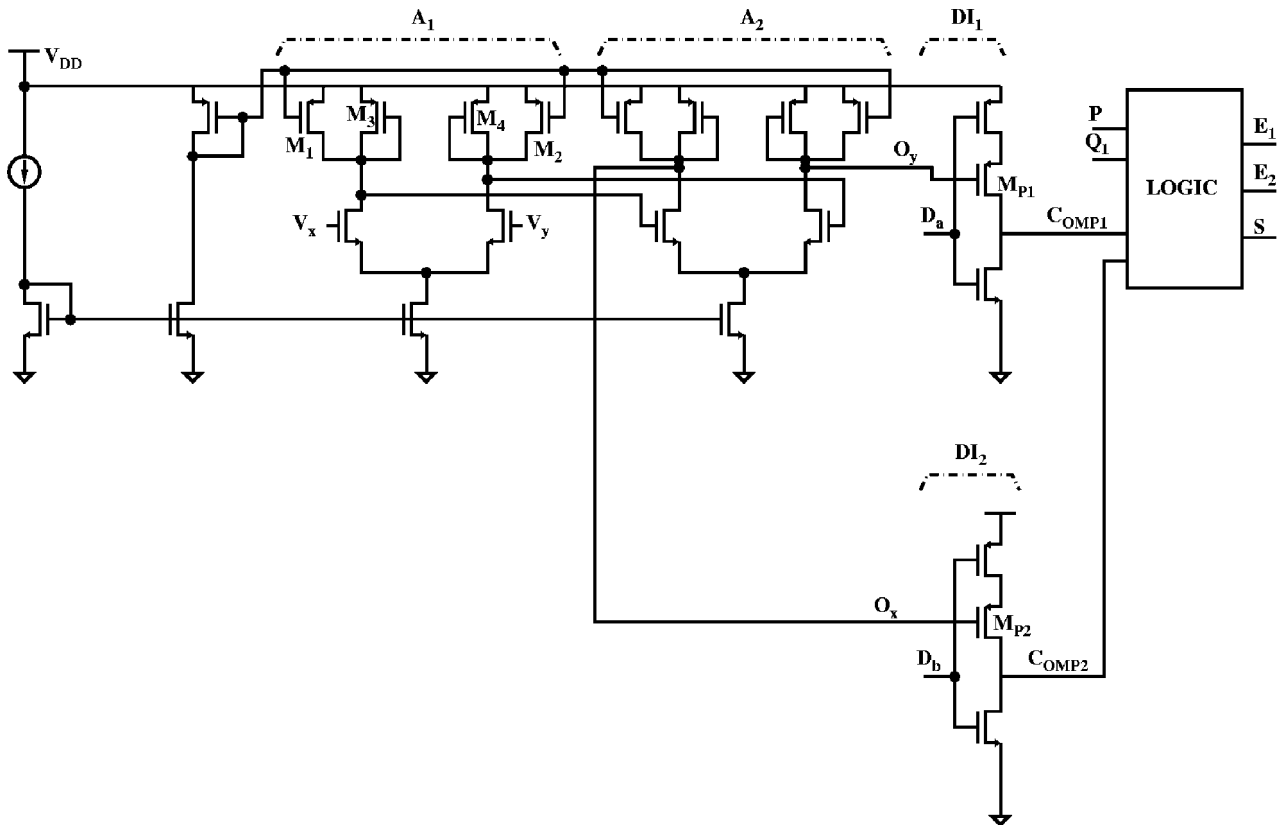


**Fig. 6.** Timing diagram of dual-phase fully differential ZCB pipeline ADC.

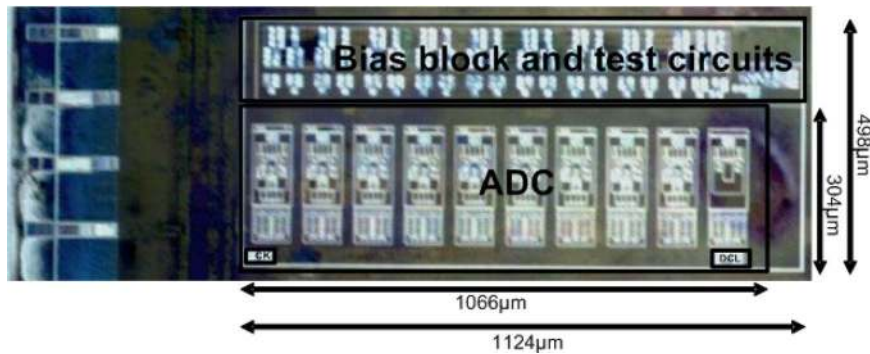
order of magnitude smaller than  $I_1$ , resulting in a slower ramp that generates much smaller overshoot [21]. When the inputs  $V_x$  and  $V_y$  cross again during the fine phase, the sampling signal  $S$  falls to open the sampling switches. The accurate output voltage is sampled on the next stage capacitors  $C_1, C_2, C_3,$  and  $C_4$  at that instant.

A single differential preamplifier is used for both the fine and the coarse phases for lower power consumption and offset matching between the two phases. The preamplifier has two stages of differential amplifiers  $A_1$  and  $A_2$ , as shown in Fig. 7. The differential amplifier stages provide voltage gain and common-mode and power-supply rejection. The first stage  $A_1$  is band-limited for lower noise. Since the PMOS-input dynamic inverter can detect only a negative-going change of the input signal, two dynamic inverters  $DI_1$  and  $DI_2$  are used as threshold detectors during the coarse and fine phases, respectively.

A prototype ADC fabricated in a 65 nm 1.2 V CMOS process is implemented in a core die area of  $0.33 \text{ mm}^2$ , as shown in Fig. 8. The measured DNL and INL are  $+0.16/-0.22$  and  $+0.45/-1.21$  LSB, respectively. The measured SNDR with a 12.9 MHz input tone is 54.3 dB (8.73 ENOB), and the SFDR 70.4 dB. Table 2 shows the summary of



**Fig. 7.** Schematic diagram of dual-phase differential ZCD.



**Fig. 8.** Die photograph of dual-phase differential ZCB pipeline ADC.

performance. The core ADC power consumption is 1.78 mW, resulting in a 161 fJ/step FOM.

### C. Single-Phase Differential ZCB Circuit: High Speed, Accuracy, and Power-Supply Rejection

A single-phase charge-transfer operation offers higher speed than the dual-phase operation at the cost of linearity and power efficiency. Dynamic biasing or duty cycling the differential preamplifier can recover the power efficiency, as explained in the next section. In this section, a single-phase fully differential ZCB pipeline ADC with preamplifier duty cycling is described [22]. Further reduction in power consumption is achieved by removing the CMFB circuit. A power-efficient offset cancellation based on chopping is also introduced.

A simplified schematic and timing diagrams of two adjacent fully differential ZCB pipeline stages are shown in Figs. 9 and 10. During the sampling phase, the input voltage is sampled onto sampling capacitors  $C_{1\pm}$  and  $C_{2\pm}$ .

The transfer phase begins when the precharge signal  $\varphi_{2I}$  turns on devices  $M_3$ ,  $M_{4\pm}$ , and  $M_{5\pm}$  to initialize the load capacitors  $C_{3\pm}$  and  $C_{4\pm}$  to  $V_{DD}$  and ground, respectively. This ensures the differential output voltage starts below the minimum full scale range. After the precharge phase, current sources  $I_{2\pm}$ ,  $I_{3\pm}$ , and  $I_{4\pm}$ , which have been split to avoid series switches for improved linearity [20], begin to charge the capacitors. The resulting voltage ramp continues until the ZCD detects the virtual ground condition, i.e.,  $v_{x+} = v_{x-}$ . At this point, the ZCD output  $\varphi_{2e}$  turns off the differential sampling switch  $M_3$  to sample the desired residue voltage.

To improve the power-supply noise rejection, symmetric dummy current sources (not shown in Fig. 9) that are permanently turned off are added on both the positive and negative channels to provide first-order parasitic capacitance matching between the power supplies and the output nodes. This ensures that high-frequency power-supply noise coupling is common mode and does not get sampled on the differential output nodes  $v_{o\pm}$ .

In traditional fully differential op-amp based implementations, CMFB is essential to keep both channels of the differential signal within range. CMFB is necessary because a fully differential op-amp typically has high native common-mode gain. The dual-phase fully differential ZCB ADC described in the previous section employs a similar CMFB during the coarse phase. In high-speed circuits, the conventional CMFB circuits pose a challenge due to the fast common-mode settling requirement. Unlike op-amp based fully differential circuits, the native common-mode gain of a ZCB circuit is very low because the output common mode is reset automatically to  $V_{DD}/2$  during each preset phase. The output common-mode variation is small and results from ramp-rate differences between the positive and negative channels. Therefore, the CMFB can be completely removed, improving the speed and power consumption.

The ZCD used in this design is shown in Fig. 11. The ZCD consists of a differential preamplifier and a dynamic threshold detector. The preamplifier is duty-cycled to save power. The output of the detector is fed back to  $M_6$  to turn

**Table 2** Dual-Phase Differential ZCB Pipeline ADC Performance Summary

Technology	65nm CMOS 1-Poly 6-Metal
Supply voltage	1.2V
Resolution	10b
Sampling Rate	26MS/s
Full-scale Input	1.0Vpp
Die Area	0.33mm <sup>2</sup>
Power consumption	1.78mW
DNL	+0.16 / -0.22LSB
INL	+0.45 / -1.21LSB
ENOB	8.73b
FOM	0.161pJ/step



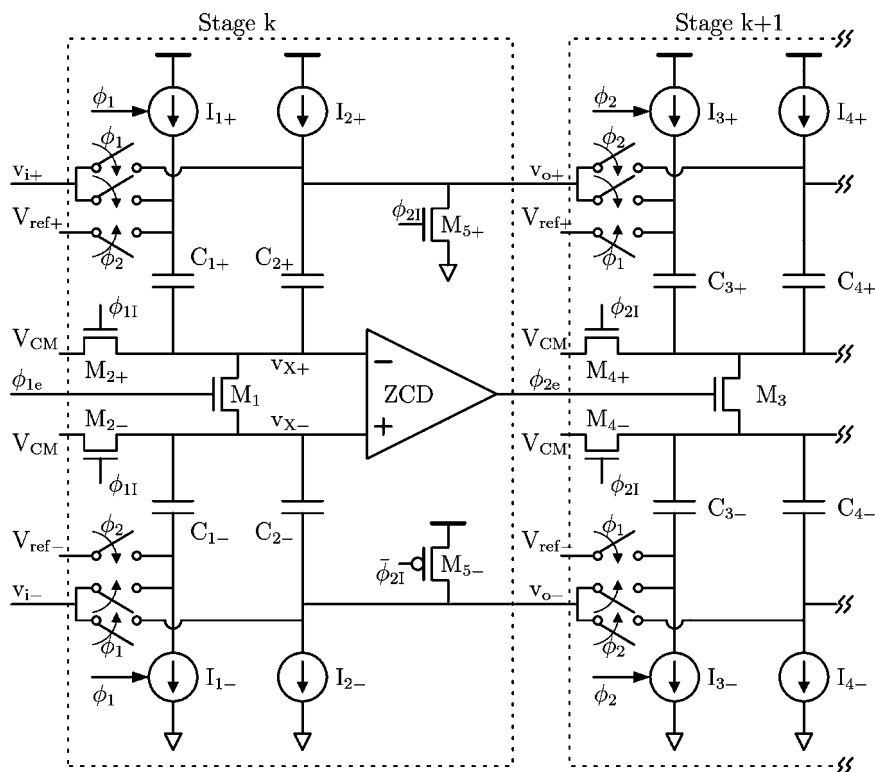


Fig. 9. Schematic of two stages of single-phase fully differential ZCB pipeline ADC.

off the bias current in the preamplifier as soon as the ZCD switches.

Offset in a ZCB circuit design comes from conventional sources such as device mismatch as well as the voltage ramp overshoot due to the finite delay of the ZCD. In this work, both sources of error are removed by a chopping technique. This offset cancellation removes both systematic and random offsets while adding a negligible amount of power consumption.

Implemented in  $0.3 \text{ mm}^2$  area in a 90 nm CMOS process with a power-supply voltage of 1.2 V, this design consumes 4.5 mW at 50 MS/s. The DNL is within  $\pm 0.5$  LSB and the INL is within  $\pm 3$  LSB on a 12 bit scale. The SNDR and SFDR measure 62 and 68 dB, respectively. The measured ENOB with a near-Nyquist rate input tone is 10.0 and 10.6 bits at 50 and 25 MS/s, respectively, and the resulting FOM is 88 and 98 fJ/step. The small-signal SNR is 72.3 dB, indicating that the ENOB is limited not by thermal noise but by distortion caused by INL. The dominant source of INL comes from offsets in the bit decision comparators in the sub-ADC of each stage. These offsets are larger than Monte Carlo simulation predicted and cause the cascoded current sources to leave saturation when the residue nears the positive reference.

The fully differential design greatly improves the signal integrity as shown in Fig. 12. The noise level hardly changes for the I/O voltage levels between 1.2 and 2.6 V, in

contrast to the severe degradation of SNR in the single-ended implementation shown in Fig. 4. Disabling the I/O and taking the data through an on-chip SRAM does not change the SNR either. Fig. 13 shows the die photograph, and Table 3 summarizes key performance parameters.

### III. ULTIMATE POTENTIAL FOR ANALOG POWER FOR HIGH-PERFORMANCE ADCs

Table 4 shows the evolution of comparator and zero-crossing based circuit design and performance since the development of the first prototype CBSC pipeline ADC. Every new design roughly halved the FOM while increasing the ENOB or the sampling rate or both.

The latest design discussed in Section II-C is compared with the state of the art in Table 5. Since the traditional FOM gets worse as the ENOB or sampling rate becomes higher, it must be compared in the same ENOB and sampling-rate ranges. Table 5 lists published ADCs with sampling rate 50 MS/s and higher and ENOB of ten or higher at the Nyquist input frequency. Only ADCs with FOM less than 1 pJ/step are listed.<sup>1</sup>

<sup>1</sup>Delta-sigma ADCs are excluded from this comparison because they are suitable for a different application space. They are not suitable for high-bandwidth applications because time-interleaving to sample a higher bandwidth signal is impractical or difficult. Moreover, the more popular continuous-time delta-sigma ADCs are incapable of sub-Nyquist sampling.

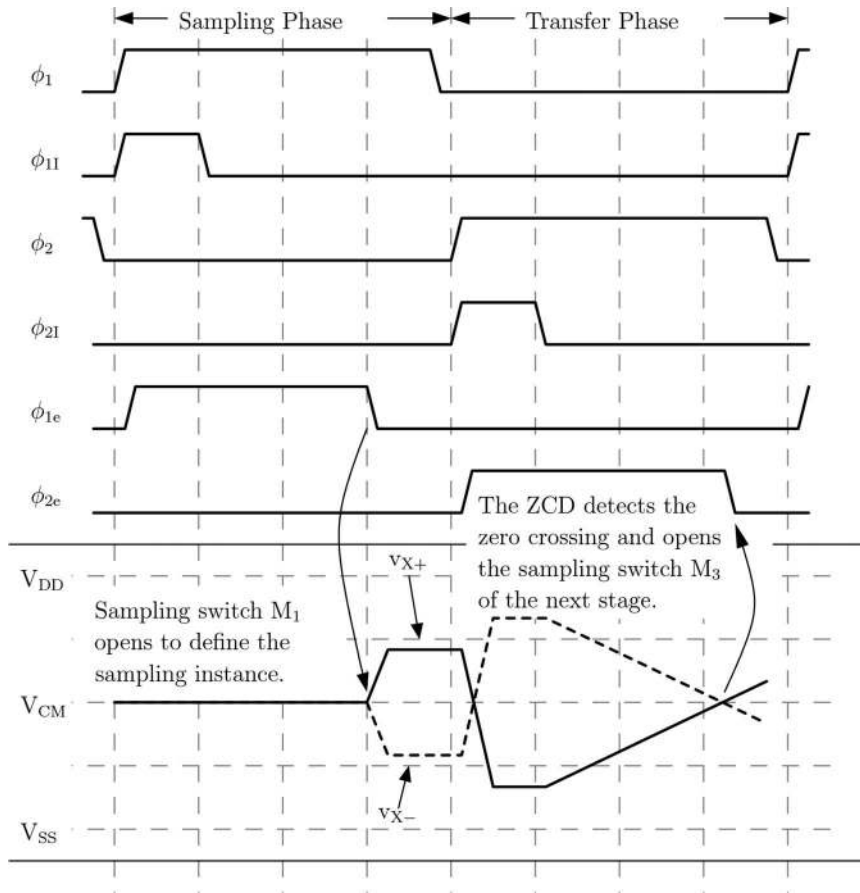


Fig. 10. Timing diagram for single-phase fully differential ZCB pipeline ADC.

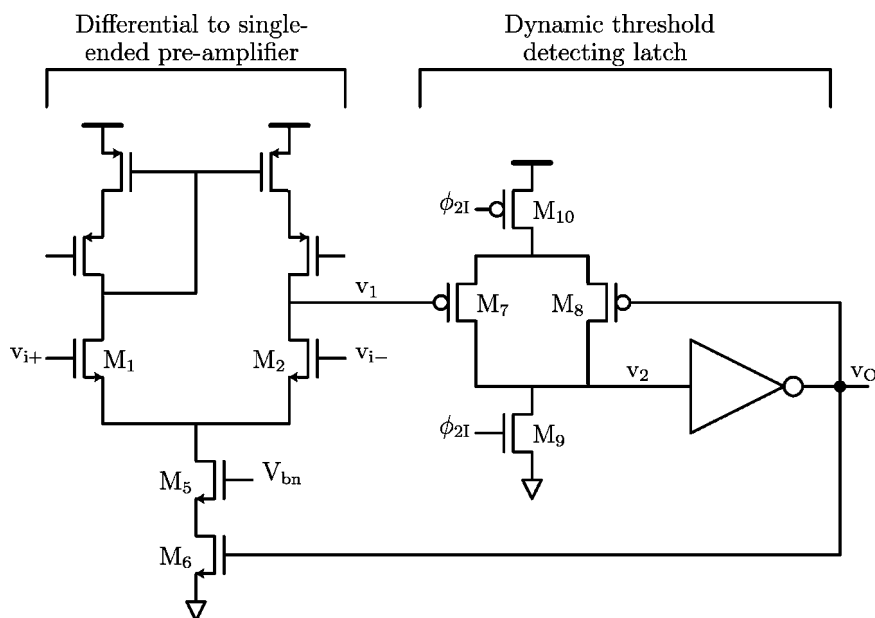


Fig. 11. Differential zero-crossing detector.

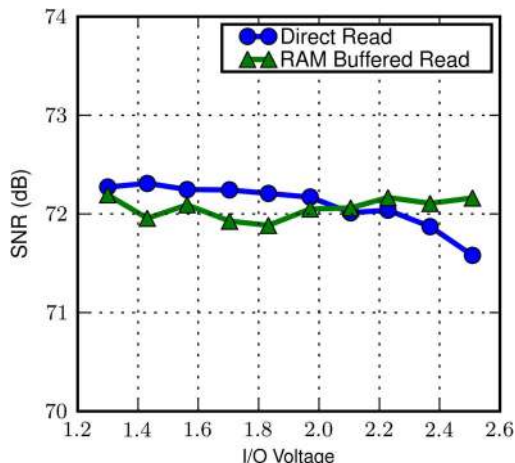


Fig. 12. I/O voltage versus noise of fully differential ZCB pipeline ADC.

Steady improvements in performance as well as the FOM have been made in ZCB circuits as knowledge is gained in the design strategy of zero-crossing based circuits. The latest design already surpasses the state-of-the-art FOM in the same performance range. Although maintaining a similar rate of progress will not be possible indefinitely, there is much room for improvements as more design experience is gained and innovative techniques are learned for ZCB circuits.

The experimental data demonstrate the viability and low power capability of ZCB circuits. In this section, we speculate on the ultimate potential of this class of circuits by examining the theoretical and practical limits.

It would be of interest to investigate what level of power consumption may be feasible when the design techniques mature. This section attempts to compare the ultimate low power potential of ZCB ADCs with traditional designs such as op-amp based pipeline, flash, and successive approximation ADCs. Delta-sigma ADCs

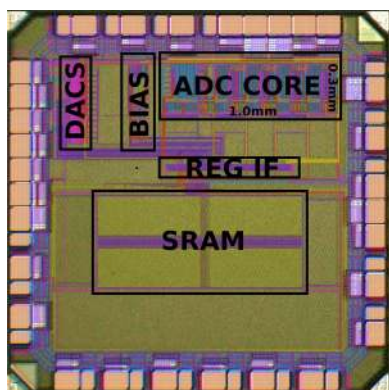


Fig. 13. Die/layout photograph of single phase fully differential ZCB pipeline ADC (layout diagram overlaid on die photo to show details).

Table 3 Single-Phase Differential ZCB Pipeline ADC Summary of Performance

<b>Technology</b>	<b>90nm CMOS</b>	
<b>Supply Voltage</b>	<b>1.2V</b>	
<b>Resolution</b>	<b>12 bits</b>	
<b>Full-Scale Input</b>	<b>2V (differential)</b>	
<b>Area</b>	<b>0.3 mm<sup>2</sup></b>	
<b>Sampling Rate</b>	<b>25MS/s</b>	<b>50MS/s</b>
<b>Power Consumption</b>	<b>3.8mW</b>	<b>4.5mW</b>
<b>DNL</b>	<b>±0.5 LSB</b>	<b>+0.68/-0.4LSB</b>
<b>INL</b>	<b>±2.0 LSB</b>	<b>±2.7 LSB</b>
<b>SNR</b>	<b>72dB</b>	<b>72dB</b>
<b>SFDR</b>	<b>73dB</b>	<b>68dB</b>
<b>SNDR</b>	<b>66dB</b>	<b>62dB</b>
<b>ENOB</b>	<b>10.6b</b>	<b>10.0b</b>
<b>FOM</b>	<b>98 fJ/step</b>	<b>88 fJ/step</b>

are excluded from this comparison for reasons stated previously.

The FOM is a useful measure in comparing the energy efficiency of ADCs. The traditional FOM is given by [24]

$$FOM = \frac{P}{2f_{sig} \cdot 2^{ENOB}} \tag{1}$$

where  $f_s$  is the signal bandwidth and ENOB the effective number of bits ( $ENOB = (SNDR(dB) - 1.8)/6$ ). SNDR is the maximum SNDR measured with a sinusoidal input. The FOM has a unit of energy per conversion step,  $1/2^N$ , and is typically expressed in picojoules/step.

The standard FOM in (1) is largely based on empirical data and includes noise and distortion regardless of their sources. In ADCs with resolution of 10 bits or higher, thermal and shot noise become the fundamental limit of resolution. Previously, we suggested that the thermal-noise limited FOM would be more appropriate for investigating the ultimate low power potential in ADCs with resolution 10 bits or higher [25]. The thermal-noise based FOM2 is

$$FOM2 = \frac{P}{2f_{sig} \cdot SNTR^2} \tag{2}$$

Table 4 Evolution of Performance in CBSC and ZCB ADCs

Design	Resolution (Bits)	ENOB (Bits)	Sampling Rate (MS/s)	Signal path	Node	FOM (fJ/step)	Year
CBSC	10	8.7	7.9	Single-Ended	0.18 $\mu$	800	2006 [19]
Single-ended ZCB	8	6.9/6.7	100/200	Single-ended	0.18 $\mu$	380	2007 [20]
Differential ZCB	10	8.7	26	Differential	65nm	161	2008 [21]
Differential ZCB	12	10.0	50	Differential	90nm	88	2009 [22]

where SNTR is the maximum signal-to-thermal noise ratio. It can be shown that the charge transfer phase dominates the power consumption in most switched-capacitor ADCs. The FOM2 of traditional single-ended switched-capacitor circuits was derived previously [25]. In fully differential circuits, the signal swing doubles, reducing the FOM2 by a factor of four from that of a single-ended circuit

$$\text{FOM2} = \frac{P}{2f_{\text{sig}} \cdot \text{SNTR}^2} = F \cdot \frac{\gamma k T V_{DD} V_{pv}}{(V_{DD} - 2\Delta)^2} \quad (3)$$

where the factor  $F$  for a fully differential op-amp based circuit is given by

$$F = 16.5(N + 1)(1 + b)(1 + d)(1 + g). \quad (4)$$

In (4),  $N$  is the accuracy in number of bits the op-amp output must settle to, and  $\gamma$  is a noise coefficient that depends on the device region of operation. The linear dependence of FOM2 on  $N + 1$  is the result of exponential settling of the op-amp output. The parameters  $b$  and  $d$

represent noise from noninput devices and power consumption in other parts of the op-amp than the input stage, respectively. The parameter “ $g$ ” accounts for the increase in settling time due to slewing and ringing, and the pivot voltage  $V_{pv}$  is defined as the ratio between transconductance and bias current. In weak inversion,  $V_{pv} = nkT/q \approx 40$  mV, and in strong inversion  $V_{pv}$  increases to  $(V_{GS} - V_T)/2$ . Since the FOM2 (and power consumption) is proportional to  $V_{pv}$ , minimizing  $V_{pv}$  is desirable. The minimum  $V_{pv}$  can be determined by the minimum  $f_T$  requirement, as explained in the Appendix.

The FOM2 for all types of the ADCs has exactly the same form as in (3) with different expressions for the factor  $F$ . In a flash ADC

$$F = 64(1 + b)2^N \quad (5)$$

where  $b$  represents noise from devices other than input devices of the comparator preamplifier. The parameter  $d$  that accounted for the noninput-stage power consumption in the op-amp circuit is absent here because a regenerative latch that typically follows the preamplifier consumes a

Table 5 Comparison of Low-Power ADCs

Resolution (Bits)	ENOB (Bits)	Sampling Rate (MS/s)	Type	Node	FOM (fJ/step)	Year
14	11.7	100	Pipeline	0.18 $\mu$	679	2008 [26]
13	10.6	250	Bucket Brigade Pipeline	0.18 $\mu$	349	2008 [15]
12	10.3	50	Pipeline	0.18 $\mu$	285	2008 [27]
12	10.0	50	ZCB Pipeline	90nm	88	2009 [22]

Table 6 FOM Comparison Table

Converter Type	Value of $F$	$f_T$ Requirement
Pipeline (Op-Amp Based)	$16.5(N+1)(1+b)(1+d)(1+g)$	$2.2(N-M+3)f_s$
Flash	$F = 64(1+b)2^N$	$1.6f_s$
Interpolating	$F = 64(1+b)\frac{2^N}{M}$	$1.6f_s$
Successive Approximation	$16(1+b)(N+M)$	$\frac{1.6(N+M)f_s}{1-(N+M)f_sT_I}$
Differential CBSC Pipeline (Dual Phase)	$\frac{48}{\alpha}(1+b)$	$\frac{6.4}{\alpha}f_s$
Differential ZCB Pipeline (Dual Phase)	$\frac{48}{\alpha}(1+b)$	$\frac{6.4}{\alpha}f_s$
Differential ZCB Pipeline (Single Phase)	$\frac{48D}{\alpha}(1+b)$	$\frac{6.4}{\alpha}f_s$
Dynamic ZCB Pipeline	12	$\frac{6.4}{\alpha}f_s$

negligible amount of power compared with the preamplifier. Since most flash ADCs employ a single-ended signal path, the factor  $F$  is computed for the single-ended architecture. Interpolating (nonfolding) flash ADCs require fewer preamplifiers for the comparators and have a correspondingly better FOM

$$F = 64(1+b)\frac{2^N}{M} \tag{6}$$

where  $M$  is the number of levels produced by interpolation. The FOM can be better than this figure in practice due to some spatial averaging effects of preamplifiers. The exact improvement factor depends on the design of the interpolator.

Similar derivation for a fully differential capacitor array successive approximation ADCs yields

$$F = 16(1+b)(N+M) \tag{7}$$

where  $M$  is the number of subclock cycles during which the input voltage is sampled on the capacitor array. A smaller value of  $M$  improves the FOM but places more burden on the input buffer because it has to settle faster.

Noise in the comparator and the ZCD in CBSC and ZCB circuits causes jitter in the sampling edge. The jitter acting on the ramp slope produces noise in the sampled voltage. It can be shown that the input referred noise is independent of the ramp rate and is identical to noise computed directly from the input referred thermal (or shot) noise of the comparator or the ZCD [28]. The factor  $F$  for the CBSC circuit was derived previously where an integrating-type preamplifier was assumed [25]. The analysis can be easily generalized to a differential ZCB

circuit with a wide-band preamplifier employed in the ZCB prototypes, giving

$$F = \frac{48}{\alpha}(1+b) \tag{8}$$

where  $1/\alpha$  is the product between the clock period and the noise bandwidth of the ZCD. For a well-designed dual-phase circuit, the value of  $\alpha$  is approximately 0.5. In a single-phase circuit, the linearity and speed requirements typically limit the maximum  $\alpha$  to approximately 0.2. Again, the parameter  $d$  that accounted for the noninput stage power consumption is absent because a dynamic threshold detector that follows the preamplifier consumes negligible power compared with the preamplifier.

If the preamplifier is duty-cycled

$$F = \frac{48D}{\alpha}(1+b) \tag{9}$$

where  $D$  is the duty cycle of the preamplifier. For example, in the single-phase ZCB pipeline ADC described in Section II-C, the preamplifier is turned off immediately after the ZCD trips. The theoretical value of the average duty cycle  $D$  is close to 0.5. The actual value depends on several design parameters such as the power supply voltages and the reference voltages. In a typical design,  $D$  is approximately 0.7. In a single-ended dynamic ZCD-based circuit, it can be shown that  $F = 12$ .

Table 6 summarizes the factor  $F$  for various ADC architectures and the minimum  $f_T$  requirement calculated from the formula in the Appendix. The power consumption that may be feasible for various different ADC architectures can be calculated from FOM2. In Table 7, ADC

Table 7 Power-Consumption Comparison for 12 Bit, 250 MS/s ADCs

Converter Type	$F$	$f_T$	$V_{pv}$	Power Consumption (mW)
Pipeline (Op-Amp Based)	1716	13.2 GHz	60 mV	7.66 mW
Flash	$3.93 \times 10^5$	400 MHz	40 mV	502 mW
Interpolating	$2.45 \times 10^4$	400 MHz	40 mV	31.4 mW
Successive Approximation	1020	45 GHz	240 mV	1.1 mW
Differential CBSC Pipeline (Dual Phase, $\alpha=0.25$ )	288	6.4 GHz	40 mV	735 $\mu$ W
Differential ZCB Pipeline (Dual Phase, $\alpha=0.5$ )	144	3.2 GHz	40 mV	367 $\mu$ W
Differential ZCB Pipeline (Single Phase, $\alpha=0.2$ , $D=0.7$ )	252	8 GHz	40 mV	643 $\mu$ W

architectures and their power potential at a 12 bit thermal noise floor and a 250 MS/s sampling rate are listed. Table 8 is for 16 bit thermal noise floor and 100 MS/s sampling rate. The values of  $V_{pv}$  and  $\gamma$  are derived from the minimum  $f_T$  and the  $f_T$  versus  $V_{pv}$  plot for 90 nm MOS transistors, shown in the Appendix. For op-amps, a two-stage design with a PMOS cascaded input stage is assumed with  $b = 3$ ,  $d = 4$ , and  $g = 1$ . For comparators and ZCDs, it is assumed that an NMOS input differential pair dominates the power consumption, with  $b = 0.5$ . For pipeline converters, the second and subsequent stages are assumed to account for 50% of the total power. Dynamic ZCD-based circuits are

excluded from these high-resolution converters due to their limited supply rejection from the single-ended signal path. Obviously, the choice of some of the parameter values is somewhat arbitrary. Nevertheless, the intention is to choose values for expertly designed circuits.

Tables 7 and 8 show that the zero-crossing based converters have a potential for more than an order of magnitude lower power consumption than op-amp based counterparts. As expected, flash converters consume a large amount of power and are impractical in these resolution ranges due to their complexity. Successive approximation converters are power efficient because they do not

Table 8 Power-Consumption Comparison for 16 Bit, 100 MS/s ADCs

Converter Type	$f_T$	$V_{pv}$	Power Consumption
Pipeline (Op-Amp Based)	5.3 GHz	50 mV	785 mW
Flash	160 MHz	40 mV	51.4 W
Interpolating	160 MHz	40 mV	3.21 W
Successive Approximation	5.77 GHz	40 mV	113 mW
Differential CBSC Pipeline (Dual Phase, $\alpha=0.25$ )	2.56 GHz	40 mV	85.3 mW
Differential ZCB Pipeline (Dual Phase, $\alpha=0.5$ )	1.28 GHz	40 mV	42.6 mW
Differential ZCB Pipeline (Single Phase, $\alpha=0.2$ , $D=0.7$ )	3.2 GHz	40 mV	74.6 mW

require op-amps. As mentioned previously, however, one practical issue with successive approximation converters is the large array capacitance. Often, the input buffer consumes greater power than the ADC itself to drive the large capacitor array.

The power-consumption figures in Tables 7 and 8 represent what may be ultimately possible for the ADC core excluding the supporting circuitry such as the voltage references, input buffers, and digital circuits. The power consumption of state-of-the-art ADCs, regardless of their architecture, are still more than an order of magnitude higher than these figures. Many issues that are not considered in this section's analysis can drive the power-consumption figure much higher. For example, in op-amp based circuits, the open-loop gain requirement may necessitate long channel devices or gain enhancement circuits, which will increase power consumption significantly. Longer devices increase parasitic capacitance and lower nondominant pole frequencies. The additional devices to achieve higher gain introduce additional parasitic poles. To obtain a reasonable phase margin, power needs to be spent to push out these parasitic poles, and devices may need to be biased in the high  $V_{pv}$  region. For zero-crossing based circuits, the ZCD power may have to be increased beyond what thermal noise dictates in order to drive large sampling switches rapidly. Due to the inherently low power consumption in these circuits, power consumption in digital circuits and flash ADC comparators, which is typically much smaller than the ADC core power consumption in op-amp based ADCs, may not be negligible. Ramp linearization circuits for higher accuracy applications can add power consumption, although the extra power is likely to be modest at most. Closed-loop offset cancellation approximately quadruples power consumption for the same noise floor and sampling rate in both op-amp based and ZCB circuits. For this reason, more power-efficient offset cancellation technique such as chopper offset estimation is preferred [22], [23]. Power consumption in the input and reference buffers must also be considered. The ZCB circuits require smaller capacitors compared to op-amp based ADCs for the same noise floor because zero-crossing detectors contribute considerably less noise than op-amps. Therefore, the capacitance loading on the input and reference buffers is lower than op-amp based circuits, thus significantly lowering their power consumption. Theoretically, the power consumption in these ancillary circuits amounts to only a fraction of the ADC core power consumption [24]. In order to approach the ultimate power consumption figures in the tables, continued research is of great importance to identify the sources of extra power consumption and to find power-efficient solutions to overcome these issues.

#### IV. CONCLUSION

In order to avoid difficulties with op-amps in deep submicrometer CMOS technologies, alternative circuit topolo-

gies are developed that replace virtual ground forcing by an op-amp with virtual ground detection by zero-crossing detectors. Because the same virtual ground condition is realized at the sampling instant, the key circuit characteristics are largely unchanged. For example, the robustness of the circuit operation that op-amps provide is maintained. The key circuit parameters are still determined by ratios of capacitors, which can be controlled precisely. However, the classic open-loop gain and stability concerns in op-amps are removed entirely, allowing for a simpler, low-power implementation of the same functions. A series of designs that address the key issues in ZCB circuits are presented. These include a dynamic zero-crossing detector for ultimate low power consumption, a fully differential signal path for improved power supply rejection, dual-phase operation for better linearity and power efficiency, and single-phase operation with preamplifier duty-cycling for high speed and power efficiency.

The comparison with the present state of the art indicated that the power efficiency measured by the traditional FOM of the latest prototype is superior to the best reported results in the similar performance category. While very power efficient, the ZCB circuits are still in the early stages of development. There are many issues to be discovered and resolved before they can potentially replace the mainstream op-amp based circuits. Nevertheless, the anticipated issues appear to be easier to overcome than those for op-amp based circuits in deep submicrometer technologies. The main reason is that open-loop gain, stability, settling time, and noise bandwidth are intimately interrelated in op-amp based circuits but are decoupled in ZCB circuits.

The ultimate low power potential of various types of ADCs including the ZCB and op-amp based pipeline, flash, interpolating, and successive approximation ADCs are compared from the fundamental thermal (or shot) noise constraints. The analyses show that ZCB circuits are potentially an order of magnitude more power efficient at the same resolution and sampling rate compared with most architectures. The successive approximation type ADCs are also shown to be power efficient, within a factor of two to three of ZCB pipeline ADCs. However, the total system power consumption is likely to be much higher due to the input buffer that must drive the large input capacitance presented by the capacitor array. Alternative successive approximation ADCs that do not present a large input capacitance can be a viable option for certain performance ranges. Although the single-phase fully differential ZCB prototype achieved the lowest power reported in the similar performance range by at least a factor of three, the power consumption is more than an order of magnitude higher than the analysis predicts. As indicated in Section II-C, the primary limiting factor in ENOB, and thus power efficiency, is the offsets in the flash comparators. Offset compensation in flash comparators can significantly improve the ENOB and the FOM. The thermal noise floor of  $-72.3$  dB indicates that an additional factor of four

better FOM would have been possible if it were not for the flash comparator offsets. An order of magnitude better FOM than the state-of-the art appears possible with the present design.

Continued research to optimize the power efficiency in ZCB circuits may improve the power efficiency by another factor of two to three. The foreseeable techniques include more power-efficient ZCD designs utilizing positive feedback, the use of current copiers for current sources to remove power consumption in biasing circuits, and ramp linearization circuits to improve accuracy.

Many challenges still remain to be resolved before ZCB circuits are adopted in mainstream electronic systems. Circuit simulations and the interpretations of their results are more difficult in ZCB circuits compared with op-amp based circuits because the circuit is always in transient without fully settling. More systematic and fast simulation methodology needs to be developed for an efficient design process. As described in Section III, linearity of the ramp provides the ultimate speed–accuracy–power tradeoff. Therefore, power-efficient ramp linearization techniques need to be developed to further improve the performance and power consumption. Low power offset compensation in flash comparators is another issue to be resolved to improve the accuracy and robustness. For manufacturability, the values of current sources and their matching must be managed carefully. Aforementioned current copiers can address these issues while removing power consumption in biasing circuits. The reference buffer typically requires op-amps, but its power consumption is much lower than that of op-amps in the ADC core. Nevertheless, the power efficiency of the reference buffer can be significantly improved by incorporating ZCB circuits in the reference instead of op-amps. As performance of the ZCB circuits is pushed to higher accuracy and sampling rates, more issues are likely to surface. Innovative solutions must be developed to cope with these issues while maintaining their ultra-low-power capability. ■

## APPENDIX

### $V_{PV}$ REQUIREMENT FOR INPUT DEVICES

The pivot voltage  $V_{pv}$  has a strong effect on the FOM, as indicated in (3). The pivot voltage  $V_{pv} = (V_{GS} - V_T)/2$  in strong inversion and is  $V_{pv} \approx V_{GS} - V_T$  in the high field region affected by velocity saturation. In weak inversion,  $V_{pv} = nkT/q$ , only about 40 mV at room temperature. The difference between the pivot voltages in high field versus weak inversion can be large. Therefore, it is most power efficient to bias the input devices on the edge of weak inversion for optimum FOM. Biasing them deeper in weak inversion does not improve FOM. On the contrary, it may hurt the FOM. Biasing the input devices in deep weak inversion would require wider devices that have higher parasitic capacitance. The higher parasitic capacitance  $C_p$  in Fig. 14 adversely affects the speed and noise perfor-

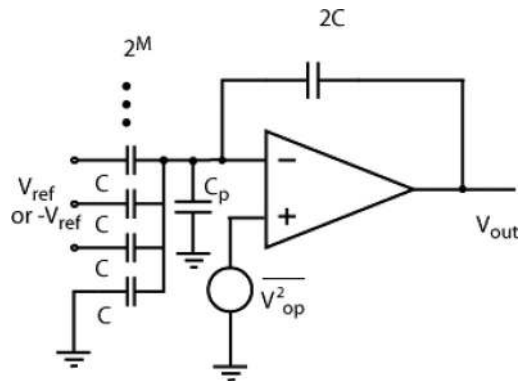


Fig. 14. Op-amp based switched-capacitor circuit.

mance of the circuit. The actual biasing point and the value of the  $V_{pv}$  depends on the bandwidth requirement of the circuit as discussed below.

The signal gain of the  $M$ -bit pipeline ADC stage shown in Fig. 14 is given by

$$A_{\text{sig}} = \frac{2^M C}{2C} = 2^{M-1}. \quad (\text{A.1})$$

The sampling rate of pipeline and cyclic converters is related to the settling time of op-amps, which can be approximately calculated from the  $-3$  dB bandwidth. Assuming that  $1/4$  LSB settling (input referred) at  $N$ -bit resolution is desired, the output of the op-amp must settle to  $1/4$  LSB at  $N - M + 1$  bits within the half-clock period  $T/2$ . This is because the first stage adds  $M - 1$  bits of resolution and the second stage must resolve  $N - M + 1$  bits if the typical redundancy is introduced between the first and the second stages. Thus

$$e^{-\frac{T_c}{2\tau}} = \frac{1}{2^{N-M+3}} \text{ where } \tau = \frac{1}{2\pi f_{-3}} = A_{\text{sig}} \frac{C}{g_{mi}}. \quad (\text{A.2})$$

Solving for the clock period  $T_c$

$$T_c = 2\tau(N - M + 3) \ln 2 = 1.38(N - M + 3) 2^{M-1} \frac{C}{g_{mi}}.$$

In practice, longer time must be allowed to account for slewing. Also ringing due to insufficient phase margin may require longer settling time. Allowing a factor of two for slewing and ringing

$$T_c = 1.38(N - M + 3) 2^M \frac{C}{g_{mi}}. \quad (\text{A.3})$$



In a pipeline ADC, a new input can be sampled every clock cycle; thus  $T_c = 1/f_s$

$$f_s = \frac{1}{1.38(N - M + 3)2^M} \cdot \frac{g_{mi}}{C} \quad (A.4)$$

where  $f_s$  is the sampling frequency.

From (A.1), (A.2), and (A.4), the closed-loop bandwidth is derived

$$f_{-3 \text{ dB}} = \frac{1}{2\pi\tau} = \frac{1.38(N - M + 3)}{\pi T_c} f_s. \quad (A.5)$$

The  $f_T$  of the devices must be much higher than the closed-loop bandwidth. Allowing an order of magnitude margin

$$f_T > 10f_{-3 \text{ dB}} = \frac{13.8(N - M + 3)}{\pi T} f_s. \quad (A.6)$$

Equation (A.6) gives minimum  $f_T$  of the devices. In practice, however, it is likely that higher  $f_T$  is required due to the design of the op-amp. In order to achieve reasonable phase margin, parasitic pole frequencies must also be much higher than the closed-loop bandwidth in (A.5). In a cascode input stage of an op-amp, for example, the drain parasitic capacitance of input transistors loads common-gate amplifier, lowering the parasitic pole frequency. In order to reduce this capacitive loading, it may be necessary to make the input devices narrower. Since the same transconductance must be maintained to keep the same closed-loop bandwidth, the input devices must be biased at higher  $V_{pv}$ , and thus higher  $f_T$ , than would be required to meet (A.6).

From the  $V_{pv}$  versus  $f_T$  curve such as those shown in Figs. 15 and 16, the minimum  $V_{pv}$  can be found. For example, for  $N = 12$ ,  $M = 3$ , and  $f_s = 250$  MS/s, the minimum  $f_T$  for the input devices is 13.2 GHz. Pipeline converters with resolution 10 bit or higher typically use a two-stage op-amp configuration in which the first stage is cascoded. In such a two-stage op-amp, the input devices are often PMOS transistors. At the minimum gate length of 90 nm, the corresponding  $V_{pv}$  for PMOS input devices is about 70 mV. However, if 180 nm length is chosen to improve matching, gain, and flicker noise,  $V_{pv}$  quickly increases to 240 mV, and the FOM and corresponding power consumption increase by more than a factor of three.

For circuits not requiring op-amps, there is no concern for stability or closed-loop bandwidth. However, in order

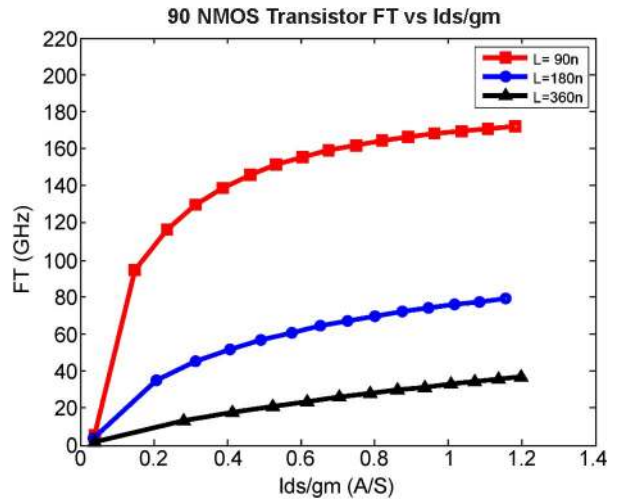


Fig. 15.  $f_T$  versus  $V_{pv}$  curve for NMOS transistors in 90 nm CMOS technology.

to avoid the device carrier transit time degrading the delay of comparators or ZCDs excessively

$$\frac{1}{2\pi f_T} \ll T_d \quad (A.7)$$

where  $T_d$  is the comparator or ZCD delay. Allowing a factor of ten as a rule of a thumb

$$f_T > \frac{10}{2\pi T_d}. \quad (A.8)$$

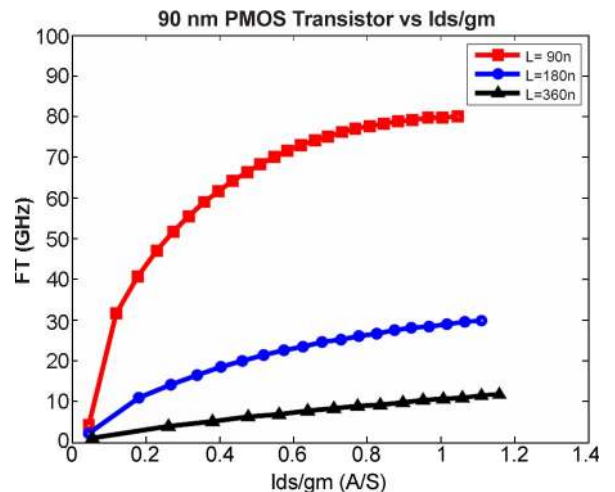


Fig. 16.  $f_T$  versus  $V_{pv}$  curve for PMOS transistors in 90 nm CMOS technology.

For flash and interpolating converters

$$f_T > \frac{10}{2\pi T_d} \approx 1.6f_s. \quad (\text{A.9})$$

In practice, however, much higher  $f_T$  will be desired to reduce the input capacitance of the flash ADC due to the large number of comparators loading the input.

In a successive approximation ADC, the maximum delay allowed for the comparator is

$$T_d = \frac{1}{f_s(N+M)} - T_l \quad (\text{A.10})$$

where  $T_l$  is the delay due to the successive approximation logic and capacitor array settling.

The minimum  $f_T$  requirement for a successive approximation ADC is then

$$f_T > \frac{1.6(N+M)f_s}{1-(N+M)f_s T_l}. \quad (\text{A.11})$$

For CBSC and ZCB circuits, it can be shown that

$$f_T > 10 \cdot \frac{2f_s}{\pi\alpha} = \frac{6.4}{\alpha} f_s. \quad (\text{A.12})$$

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