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Zero-Crossing Detector Based Reconfigurable Analog System

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Abstract— **A reconfigurable analog system is presented that implements pipelined ADCs, switched-capacitor filters, and programmable gain amplifiers. Each block employs a zero-crossing based circuit for easy reconfigurability and power efficiency. Configured as a 10-bit ADC, the chip consumes 1.92mW at 50MSPS with ENOB of 8.02b and FOM of 150fJ/conversion-step. A third order Butterworth filter is also demonstrated. The chip is implemented in 65nm technology.**

I. INTRODUCTION

While digital FPGAs provide a fast and cost-efficient method to prototype digital circuits, the development of similar system for analog circuits is still limited because it is difficult to realized a programmable analog system that can be configured to wide variety of analog circuits. Field programmable analog arrays (FPAA) have been proposed [1]. It uses continuous-time blocks whose gain is programmable by changing transconductance of amplifiers. Programmable connectivity between analog circuits is a major challenge in reconfigurable analog systems. It uses permanent connection between adjacent blocks and sets the gain of adjacent blocks to zero to effectively disconnect it. Another implementation uses programmable transconductance and programmable capacitor to control the gain of stages [2]. A programmable ADC that can be configured as sigma-delta or pipelined employs programmable capacitors, programmable connectivity, and adjustable biasing [3]. This paper demonstrates a highly-reconfigurable analog system that can be used to implement a pipelined ADC and switched-capacitor filters. Zero-crossing based circuits are utilized for superior power efficiency and reconfigurability.

II. SYSTEM DESCRIPTION

Fig. 1 shows the block diagram of the system. It consists of configurable analog blocks, programmable switches, and configuration block. Configurable analog blocks have both amplification and integration functionality. Unlike digital FPGAs, the required connectivity of analog blocks is limited
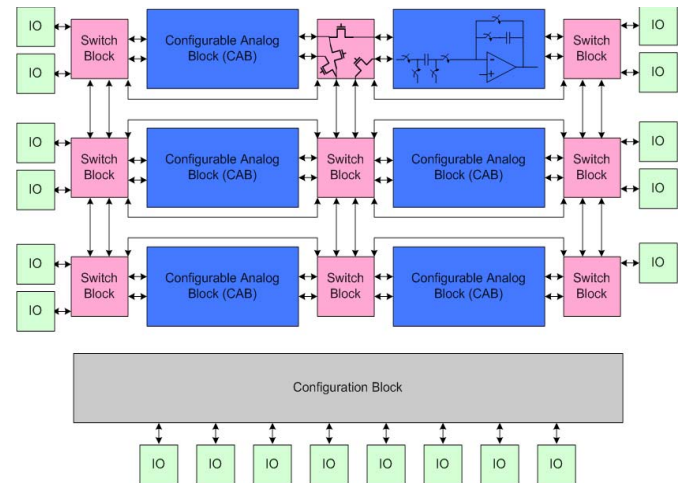

Figure 1. System Block Diagram

(both in terms of number of connections and the distance between source and destination blocks). As a result, the switches can be placed only between adjacent blocks.

Fig. 2 shows how an opamp-based switched-capacitor circuit can either amplify or integrate the input signal. If the input signal is sampled on both capacitors during phase 1, the circuit performs amplification during phase 2. If the input signal is only sampled on the lower capacitor without resetting the integration capacitor, the circuit performs integration. Fig. 3 shows the building block of a pipelined ADC. It has a bit decision comparator (BDC) and reference voltages in addition to the basic circuit of Fig. 2. Similarly, Fig. 4 shows the building block of a low-pass filter. It consists of two inputs that are being added and integrated. With differential implementation of these blocks, inverting a signal can be easily performed by switching the polarity of the differential signal.

Implementing the system with opamp raises two concerns. One is that in a highly-programmable system, the output of each block may be connected to only one other block or

several other blocks. This implies that the output load of the opamp is not known *a priori*. In addition, the feedback factor varies due to the programmability. As a result, the frequency compensation must be designed for the worst-case load and feedback conditions. This greatly compromises speed and power consumption. Another concern with opamp-based circuits is the power consumption while the operating frequency changes. Opamps consume static power and are often optimized for a particular speed.

To address both of these concerns with opamp-based circuits, zero-crossing based circuits (ZCBCs) have been used in our proposed system. ZCBC was first introduced to improve power consumption of ADCs [4,5]. Since there is no explicit feedback in ZCBC, there is no stability concern even with widely varying load and feedback conditions. In addition, no power is consumed once zero-crossing is detected (except currents in the biasing network). Therefore, power consumption is linearly proportional to the operating frequency.

III. RECONFIGURABLE BUILDING BLOCK

Fig. 5 shows the basic building block. It consists of 7 programmable capacitors, a zero-crossing detector, BDCs, and switches. In the pipeline ADC configuration, each stage has
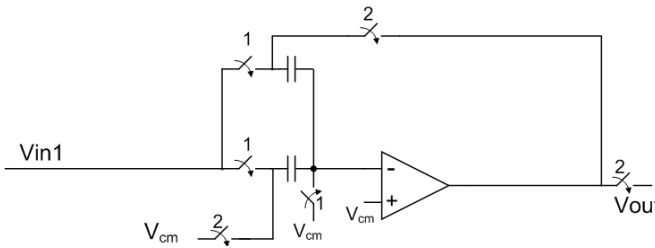

Figure 2.   Amplification and Integration using the same switched-capacitor circuit
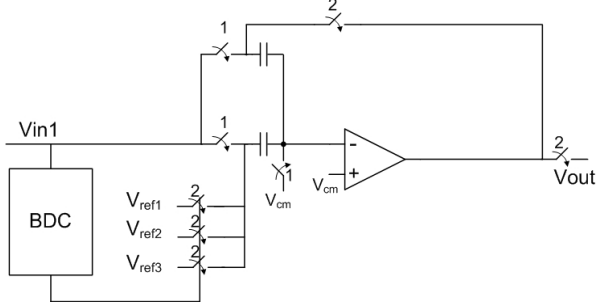

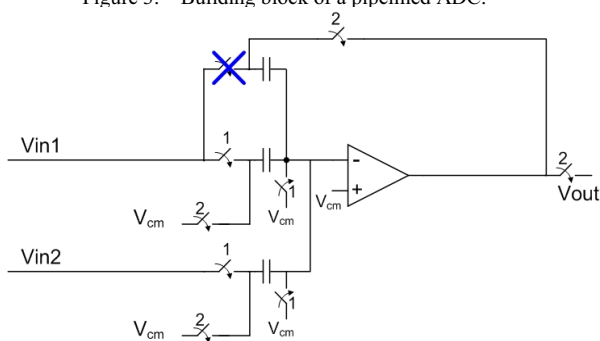Figure 3.   Building block of a pipelined ADC.

Figure 4.   Building block of an active ladder filter

2.6 bit quantization (which includes 0.6 bit over-range protection). For example, cascading 5 stages provides 10-bit resolution. Each stage has digitally-configurable feedback capacitors which provide programmable integration-coefficient for filter functionality. While these capacitors are not active in an ADC configuration, their parasitic capacitors will increase the power consumption. Putting configurable switches on both side of the feedback capacitors isolate their parasitic capacitors from the rest of the stage. Switches are bootstrapped to reduce their size and parasitic capacitance. To avoid any disturbance on the virtual-ground node, the node is buffered by a source follower before feeding into the bootstrap block. While most circuits are shown as single-ended in this paper, the actual implementation is differential. Traditionally, differential signals have the same swing on the positive and negative direction. In order to utilize the maximum signal range, asymmetric output swing is employed. Reference voltages are chosen so that they add a constant offset to the output signal to compensate for signal range asymmetry.

There are two main architectures to implement switched-capacitor filters: biquad and ladder architecture. Since this chip is intended for any arbitrary filter implementation, the exact functionality of each stage is not known before fabrication. Since biquad-based filters are sensitive to capacitor matching, ladder filter architecture is used in this chip. Fig. 6 and Fig. 7 show passive and active implementation of a ladder filter [6]. This implementation is compatible with ZCB circuits.

The binary-weighted feedback capacitors are programmed by configuration switches as shown in Fig. 5. The implementation of the terminating resistor at the input and output stages is implemented by adding an additional local feedback, which samples the output of the stage and subtracts it from the input in the next clock cycle. This implementation requires additional set of sampling capacitors when
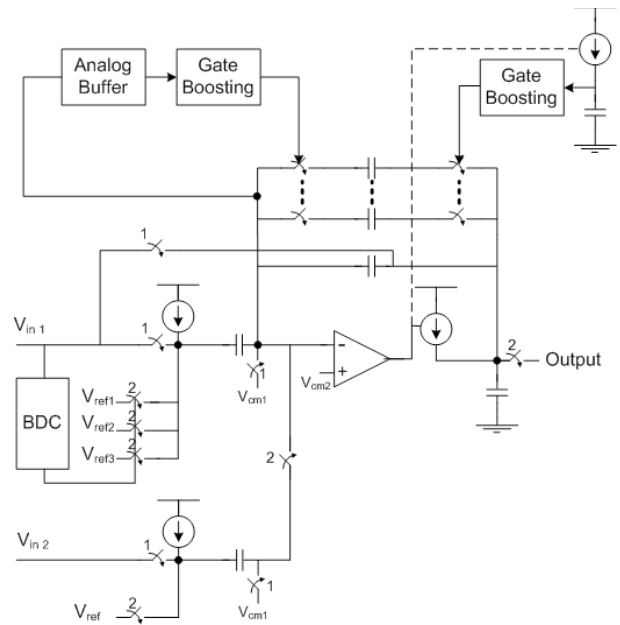

Figure 5.   Basic building block of reconfigurable stage
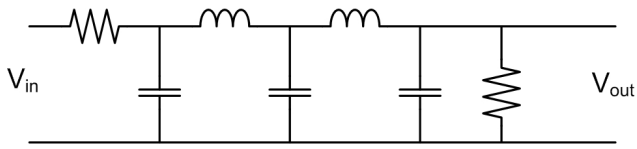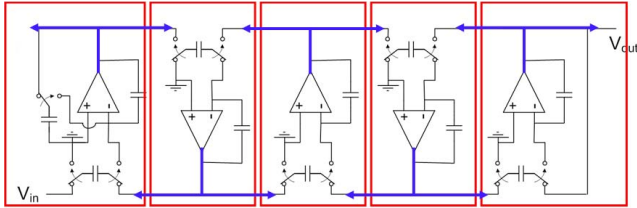
Figure 6.   Passive ladder filter

Figure 7.   Active ladder filter

implemented by opamp. In ZCB implementation, the local capacitor must sample the output at the same time it is connected to the input for integration. This timing conflict requires a second set of capacitors so that one set samples the output while the other set is connected to the input for integration. A highly-programmable system requires such a block in every configurable stage.   However, the implementation of the block is expensive in terms of required area, additional parasitics, and more complex control signals. The new solution is shown in Fig. 8. Fig. 8a shows the original implementation, where the output voltage is sampled across a unit-size capacitor and then subtracted from the input in the next cycle. The same output voltage is also sampled on the feedback capacitor. Fig. 8b shows the new circuit which performs the same functionality by splitting the feedback capacitor into two capacitors, one of which has a unit size. Instead of subtracting the output of the stage from the input in the next cycle, the unit-size capacitor in the feedback is discharged.   Since there are already binary-weighted capacitors in the feedback with the corresponding switches, this technique does not require any additional capacitors or switches to implement terminating resistors.   The only additional component is the switch to discharge the unit-size capacitor (which is very small). Using this technique, all stages can implement the terminating resistors without any penalty.
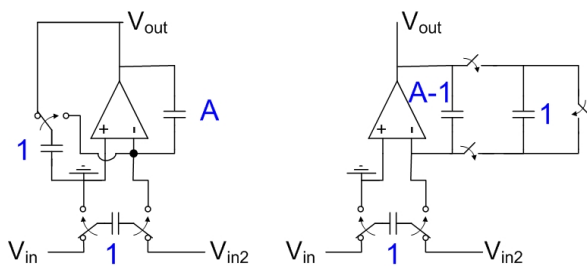

Figure 8.   Implementation of terminating resistors

IV.   EXPERIMENTAL RESULTS

Fig. 9 shows the die photo of the chip fabricated in 65nm technology. The core is 340um x 900um and consists of 8 identical stages (except for the sampling circuit of the first stage which has minor differences).   To demonstrate the configurability, the chip is configured as an ADC and a filter for two different sets of measurements.

In ADC configuration, stages 1 to 5 are used to implement a 10-bit ADC that operated at up to 50MSPS. Fig. 10 shows the dynamic performance of the ADC at 50 MSPS with a 24.7MHz sinusoid input. The ADC consumes 1.92mW with ENOB of 8.02 and FOM of 150fJ/conversion-step. INL is +1.7/-1.8b as shown in Fig. 11.   Scaling the sampling frequency scales down the power consumption linearly as shown in Fig.12. The FOM degrades, however, due to currents in the bias network, which do not scale with frequency. The 3-dB input bandwidth of the ADC is 56MHz. The reference
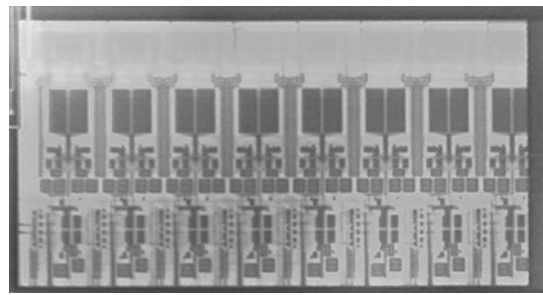

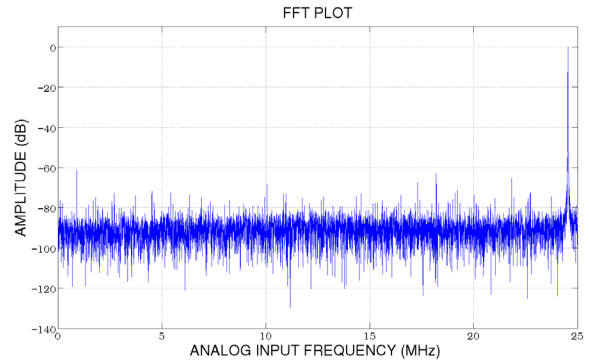Figure 9.   Die photo of the core that consists of eight stages.

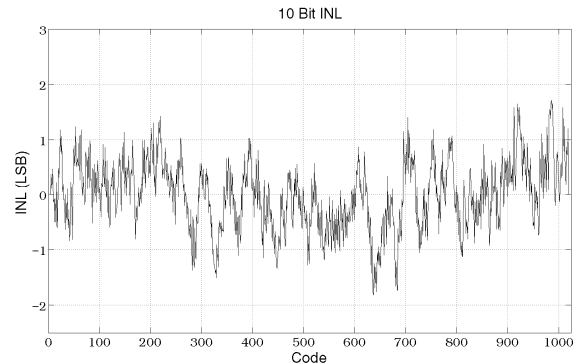Figure 10.   FFT plot of ADC output at near Nyquist rate.

Figure 11.   INL of ADC with 10 bit quantization levels

voltage is provided externally and the power drawn from the external reference voltage is negligible.

To test the filter functionality, the chip is programmed as a 3rd order Butterworth filter with cutoff frequency at 1MHz for sampling rate of 50MSPS. In this configuration, stages 1 to 3 are configured as filter and stages 4 to 8 are configured as an ADC to read out the analog output of the filter. Fig. 13 shows the frequency response of the filter. Fig. 14 compares this work with state of the art standalone ADCs and table 1 summarizes measurement results.
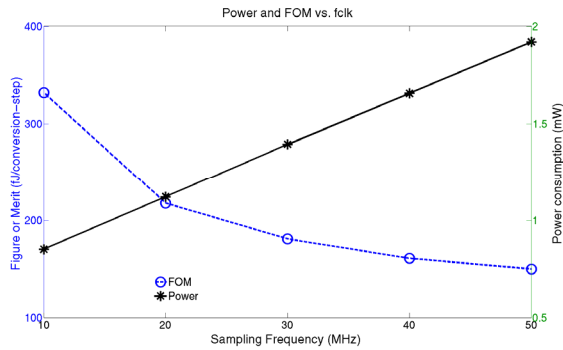

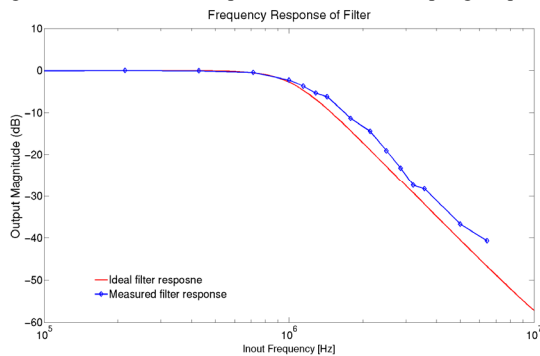Figure 12.   Power consumption and FOM vs. sampling frequency

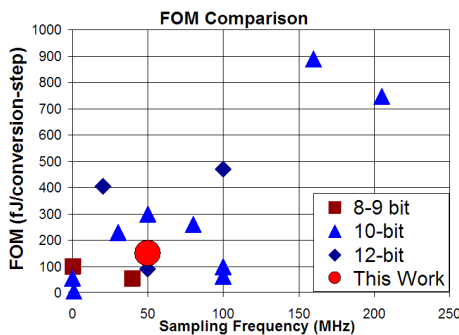Figure 13.   Ideal and measured filter transfer function

Figure 14.   Comparison of state of the art non-reconfigurable ADCs (ISSCC 2007-2010) with this work.

TABLE I.   ADC AND FILTER MEASUREMENT SUMMARY

Process	65nm Digital CMOS
Active Area	340um x 900um
Supply	1V
Functionalities	• Pipelined ADC • Low-pass filter
Pipe Line ADC:	
Quabtization Levels	10 bits
ENOB	8.02 bits
INL	+1.7/-1.8
SFDR	62dB
Power	1.92 mW (Total)
FOM	150 fJ/conversion-step
Input Signal Bandwidth	56MHz
Sampling Rate	50 MSPS
Low Pass Filter	
Type	Third order Butterworth Low-Pass Filter (switched-capacitor)
Cutoff Frequency	1MHz
Sampling Frequency	50MSPS

V.   CONCLUSION

A highly-configurable analog system is presented which can be programmed as a pipelined ADC, switched-capacitor filter, or a programmable gain amplifier. The ZCBC architecture has been used to address the stability problems and scale power consumption with sampling frequency. New technique is introduced to implement the terminating resistors in ladder filter.

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