Zero-Voltage and Zero-Current-Switching PWM Combined Three-Level DC/DC Converter

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***Abstract*—This paper proposes a zero-voltage and zero-current-switching (ZVZCS) PWM combined three-level (TL) dc/dc converter, which is a combination of a ZVZCS PWM TL converter with a ZVZCS PWM full-bridge converter. The proposed converter has the following advantages: all power switches suffer only half of the input voltage; the voltage across the output filter is very close to the output voltage, which can reduce the output filter inductance significantly; and the voltage stress of the rectifier diodes is reduced too, so that the converter is very suitable for high input voltage and wide input voltage range applications. The converter also can achieve zero-voltage-switching for the leading switches and ZCS for the lagging switches in a wide load range to achieve higher efficiency. The design considerations and procedures are presented in this paper. The operation principle and characteristics of the proposed converter are analyzed and verified on a 400–800-V input and 54-V/20-A output prototype.**

***Index Terms*—Combined three-level (TL) dc/dc converter, phase shift, zero-current-switching (ZCS), zero-voltage-switching (ZVS).**

I. Introduction

HALF-BRIDGE (HB) three-level (TL) dc/dc converters are very suited for high input voltage applications because the switches sustain only half of the input voltage. Various soft-switching HB TL dc/dc converters have been proposed in recent years, which can be classified into two types: zero-voltage-switching (ZVS) PWM TL converter [1]–[5] and zero-voltage and zero-current-switching (ZVZCS) PWM TL converter [6], [7].

The HB TL converters are essentially two-level converters because the voltage across the output filter is a two-level waveform. In some applications such as railway power supply systems or ship electric power distribution systems, the input voltage is not only very high but also variable in a wide range. The output filter inductance of the HB TL converters should be large enough to reduce the output current ripple, resulting in low power density and slow transient response. Meanwhile, the converter should be designed to output the required voltage at low line, but the duty cycle will be very small at high line, resulting in a low efficiency.

To reduce the filter requirement, various converters have been proposed in [8]–[12]. The secondary rectified voltage is a TL waveform having a low high-frequency content across the filter inductance. However, the switches sustain the whole input voltage, which is not suitable for high input voltage applications.

Liu and Ruan proposed a ZVS PWM combined TL dc/dc converter [13], which is composed of HB TL and full-bridge sections. The switches sustain only half of the input voltage; therefore, it is suitable for high input voltage applications. The converter has two operation modes: TL and two-level modes. In each mode, the rectified voltage is always close to the output voltage; therefore, the high-frequency content is reduced, and a small filter inductance can be obtained. As a result, the converter can be adopted to wide input voltage range applications. Meanwhile, all the switches can achieve ZVS in the same manner as phase-shifted full-bridge converter.

One drawback of the ZVS PWM combined TL dc/dc converter is that the two lagging switches experience ZVS difficulty because only the energy stored in the leakage inductances of the transformers is used to achieve ZVS. In order to achieve a complete ZVS of switches down to light load, we can increase the leakage inductances of the transformers or add an external resonant inductance in series with the primary sides of the transformers. However, the increased leakage inductance and/or the resonant inductance will cause a duty cycle loss at the secondary rectified voltage and will result in severe parasitic oscillation on the secondary side of the transformers, which will reduce the overall conversion efficiency indirectly.

The other disadvantage of the ZVS PWM combined TL converter is that, in the two-level mode when the primary currents decrease across zero and increase in the negative direction, the body diode reverse recovery of the leading switches will occur due to their slow switching speed, and it will result in a reverse recovery loss, which degrades severely the conversion efficiency of the converter in the two-level mode.

In order to solve the problems, the lagging switches can be realized ZCS, and they can adopt an insulated gate bipolar transistor (IGBT) instead of MOSFET. In the meanwhile, the ZVS mechanism of the leading switches remains; thus, the combined TL dc/dc converter will be turned into a combination of a ZVZCS PWM TL converter [6] and a ZVZCS PWM full-bridge converter [14], as shown in Fig. 1. The proposed dc/dc converter can achieve ZVS for the leading switches relying on the output filter inductance in a wide load range and realize ZCS for the lagging switches over a wide load and line range too; thus, the

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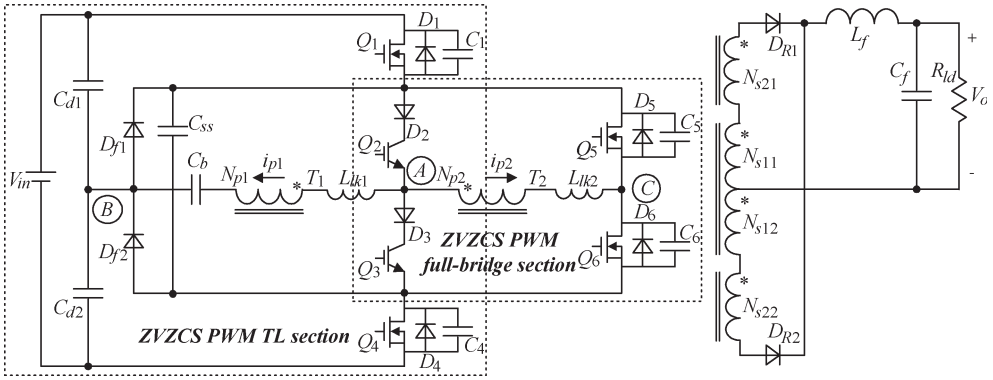

Fig. 1. ZVZCS PWM combined TL dc/dc converter.

efficiency over the line range can be increased. This converter maintains all advantages of the ZVS PWM combined TL dc/dc converter, including the reduced filter inductance requirement and the lower voltage stress on the rectifier diodes. Furthermore, the body diode reverse recovery of MOSFETs is also eliminated due to ZCS in the two-level mode. The operation analysis, characteristics, and design considerations of the proposed converter are illustrated in this paper. The performance of the converter was experimentally verified by a 54-V/20-A prototype operating at 100 kHz and with a 400–800-V input.

II. Operation Principle

As shown in Fig. 1, the proposed converter is a combination of two sections: ZVZCS PWM TL and ZVZCS PWM full-bridge sections. The ZVZCS PWM TL section is comprised of the switches Q_1–Q_4, the series diodes D_2 and D_3, the freewheeling diodes D_{f1} and D_{f2}, the flying capacitor $C_{\rm ss}$, and the transformer T_1. The ZVZCS PWM full-bridge section is comprised of the switches Q_2, Q_3, Q_5, and Q_6; the diodes D_2 and D_3; and the transformer T_2. C_{d1} and C_{d2} form a capacitive divider that splits the input voltage in half (i.e., $V_{Cd1} = V_{Cd2} = V_{\rm in}/2$). L_{lk1} and L_{lk2} are the primary intrinsic leakage inductances of T_1 and T_2, respectively. C_b is the blocking capacitor that makes the primary currents decay to zero to achieve ZCS for Q_2 and Q_3. C_b can be in series with T_1 or T_2. In Fig. 1, C_b is in series with T_1. D_2 and D_3 are in series with Q_2 and Q_3, respectively, to make them conduct only in the positive direction. The output of each section is added at the secondary side and rectified and filtered to obtain the output voltage.

Fig. 2 shows the key waveforms of the proposed converter. When the input voltage is low, the shift phase between $Q_1\&Q_4$ and $Q_2\&Q_3$ is set at a minimum value of δ to make the primary currents reset and ensure ZCS for Q_2 and Q_3. Q_2, Q_3, Q_5, and Q_6 are phase-shift controlled to regulate the output voltage, and Q_5 and Q_6 are switched leading to Q_3 and Q_2, respectively. Therefore, Q_5 and Q_6 are called leading switches, and Q_2 and Q_3 are called lagging switches. As shown in Fig. 2(a), the rectified voltage $v_{\rm rect}$ has three levels: 1 level ($(k_1+k_2)V_{\rm in}/2$), the middle level ($k_1V_{\rm in}/2$), and 0 level, where k_1 and k_2 are the secondary to primary turn ratios of T_1 and T_2, respectively. In this situation, the proposed converter operates in the TL mode.

When the input voltage increases, or during start up, overload, or short circuit, the shift phase of the full-bridge section approaches to 180°; therefore, this section operates with zero pulsewidth and does not contribute to the output. The shift phase of the TL section begins to be regulated to maintain the output voltage, Q_1 and Q_4 are leading switches, and Q_2 and Q_3 are lagging switches. In this situation, the rectified voltage has two levels: the middle and 0 levels, as shown in Fig. 2(b), and the converter operates in the two-level mode.

Whether in TL or two-level modes, $v_{\rm rect}$ is always close to its average value (the output voltage); therefore, it has a lower high-frequency content, and the output filter inductance can be reduced significantly.

The operation principles of the two modes are analyzed in this section. For convenience to analysis, it is assumed that all the switches and diodes are ideal, the flying capacitor $C_{\rm ss}$ is large enough to be treated as a voltage source with a value of $V_{\rm in}/2$, and the output filter inductance L_f is large enough to be considered as a constant current source of I_o, where I_o is the output current.

A. TL Mode

Referring to the time diagram as shown in Fig. 2(a), the proposed converter has 14 operation stages during a switching period in the TL mode. The corresponding equivalent circuits for all operation stages are shown in Fig. 3.

1) Stage 1 $[t_0, t_1]$ [refer to Fig. 3(a)]: From t_0, Q_1, Q_2, and Q_6 conduct; $v_{AB} = v_{AC} = V_{\rm in}/2$; D_{R1} conducts; and D_{R2} is off. The primary current i_{p1} charges C_b, and the initial values of i_{p1} and i_{p2} at t_0 are $I_{p01} = k_1 I_o$ and $I_{p02} = k_2 I_o$, respectively.
2) Stage 2 $[t_1, t_2]$ [refer to Fig. 3(b)]: At t_1, Q_6 is turned off, and i_{p2} charges C_6 and discharges C_5. As C_5 and C_6 limit the rising rate of the voltage across Q_6, Q_6 is zero-voltage turn off. During this stage, the current source I_o is reflected to the primary sides of the transformers and in series with the leakage inductances; therefore, i_{p1} and i_{p2} are keep at I_{p01} and I_{p02}. i_{p1} continues to charge C_b. The voltage of C_6 (v_{C6}) rises linearly, and the voltage of C_5 (v_{C5}) decays linearly. At t_2, v_{C6} rises to $V_{\rm in}/2$, and v_{C5} drops to zero, so that D_5 conducts naturally.

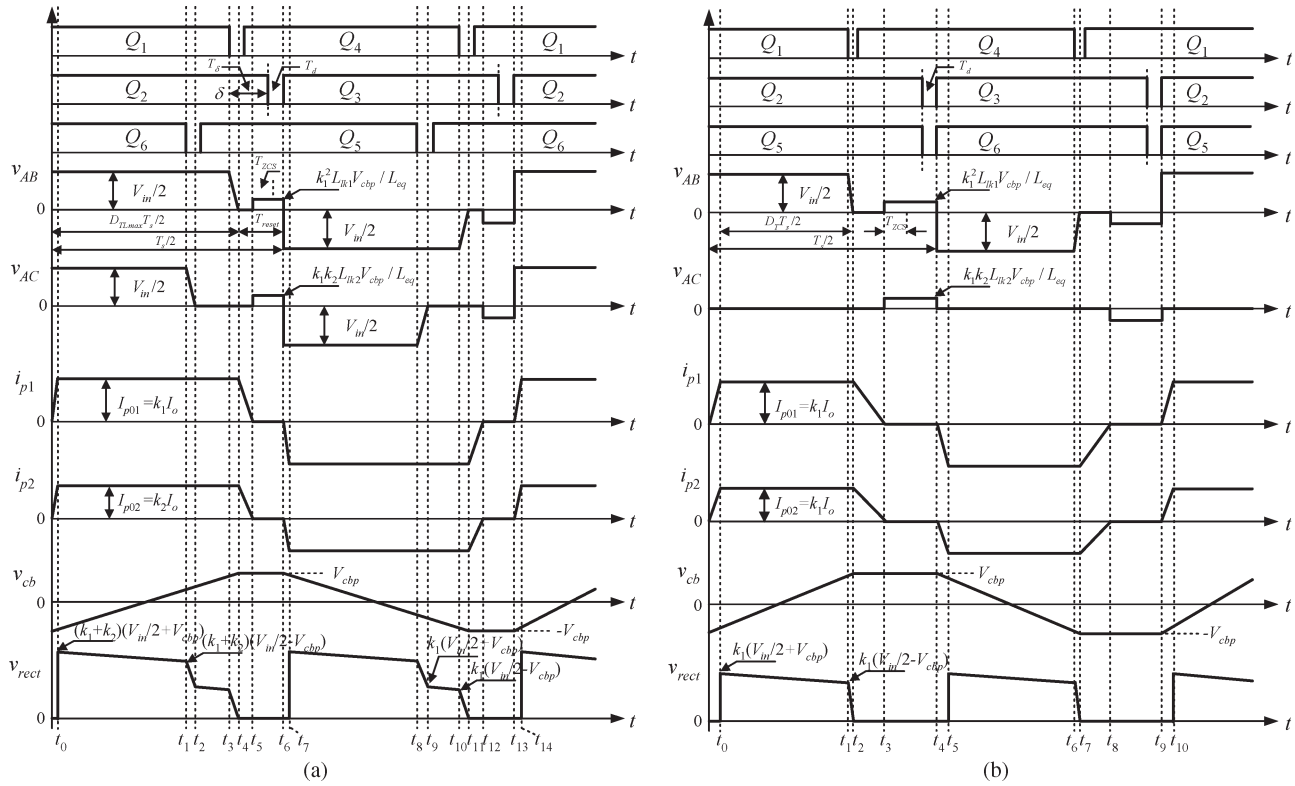

Fig. 2. Key waveforms of the ZVZCS PWM combined TL dc/dc converter. (a) TL mode. (b) Two-level mode.

3) Stage 3 $[t_2, t_3]$ [refer to Fig. 3(c)]: D_5 conducts and clamps the voltage across Q_5 at zero; as a result, Q_5 can be zero-voltage turn on. $v_{AB} = V_{\rm in}/2$, $v_{AC} = 0$, and i_{p1} continues to charge C_b.
4) Stage 4 $[t_3, t_4]$ [refer to Fig. 3(d)]: Q_1 is turned off at t_3, and i_{p1} charges C_1 and discharges C_4 via $C_{\rm ss}$. As C_1 and C_4 limit the rising rate of the voltage across Q_1, Q_1 is zero-voltage turn off. At t_4, v_{C1} rises to $V_{\rm in}/2$, v_{C4} decays to zero, D_{f1} conducts naturally, and $v_{AB} = 0$.
5) Stage 5 $[t_4, t_5]$ [refer to Fig. 3(e)]: As D_{f1} is conducting, the voltage of C_4 is clamped to zero; therefore, Q_4 is turned on at zero-voltage condition. The voltage across C_b (v_{cb}) is applied to the leakage inductances and primary windings, which forces i_{p1} and i_{p2} to reduce simultaneously. i_{p1} and i_{p2} cannot provide the output current; therefore, both the rectifier diodes conduct, shorting the series-connected secondary windings. The further equivalent circuit corresponding to this stage is shown in Fig. 4, where we have the following expressions:

$$v_{P1}+L_{lk1}\cdot\frac{di_{p1}}{dt}+V_{cbp}=v_{P1}+L_{lk1}\cdot\frac{k_1\cdot di_{\rm sec}}{dt}+V_{cbp}=0 \quad (1)$$

$$v_{P2}+L_{lk2}\cdot\frac{di_{p2}}{dt}=v_{P2}+L_{lk2}\cdot\frac{k_2\cdot di_{\rm sec}}{dt}=0 \quad (2)$$

$$v_{S1}+v_{S2}=k_1\cdot v_{P1}+k_2\cdot v_{P2}=0 \quad (3)$$

where v_{P1}, v_{P2}, v_{S1}, and v_{S2} are the primary and secondary voltages of T_1 and T_2, respectively; $i_{\rm sec}$ is the secondary current; and V_{cbp} is the peak value of v_{cb}.

From (1)–(3), the following expressions can be obtained:

$$v_{P1} = -\frac{k_2^2\cdot L_{lk2}\cdot V_{cbp}}{L_{\rm eq}} \quad (4)$$

$$v_{P2} = \frac{k_1\cdot k_2\cdot L_{lk2}\cdot V_{cbp}}{L_{\rm eq}} \quad (5)$$

$$\frac{di_{\rm sec}}{dt} = -\frac{k_1\cdot V_{cbp}}{L_{\rm eq}} \quad (6)$$

where $L_{\rm eq} = k_1^2 L_{lk1} + k_2^2 L_{lk2}$.

At t_5, $i_{\rm sec}$ transits from I_o to zero, and i_{p1} and i_{p2} decay to zero. According to (6), t_{45} can be given by the following:

$$t_{45} = \frac{L_{\rm eq}\cdot I_o}{k_1\cdot V_{cbp}}. \quad (7)$$

6) Stage 6 $[t_5, t_6]$ [refer to Fig. 3(f)]: D_2 blocks the reverse paths of i_{p1} and i_{p2}; therefore, i_{p1} and i_{p2} are kept at zero. As there is no current flowing through Q_2, Q_2 can be zero-current turn off during $[t_5, t_6]$. Both the rectifier diodes conduct and share the output current.
7) Stage 7 $[t_6, t_7]$ [refer to Fig. 3(g)]: Q_3 is turned-on at zero-current condition because the leakage inductances limit the rising rate of the primary currents. The primary currents begin to rise linearly in the negative direction and are not sufficient to power the load; therefore, both the rectifier diodes continue conducting. At t_7, i_{p1} and i_{p2} reach the reflected load current.
8) Stage 8 $[t_7, t_8]$ [refer to Fig. 3(h)]: From t_7, the primary powers the load, and i_{p1} discharges C_b. D_{R1} turns off,

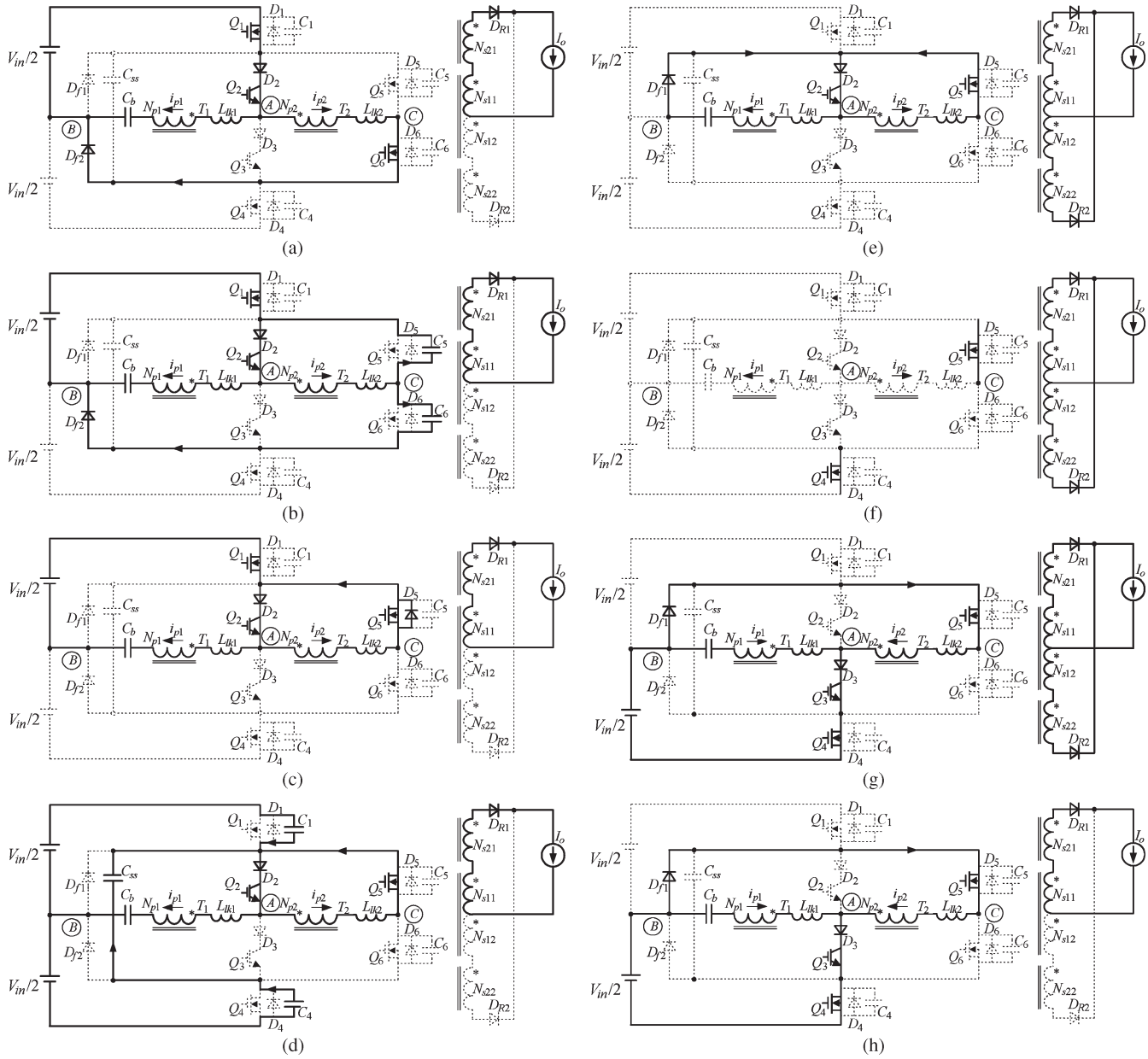

Fig. 3. Equivalent circuits in the TL mode. (a) $[t_0, t_1]$. (b) $[t_1, t_2]$. (c) $[t_2, t_3]$. (d) $[t_3, t_4]$. (e) $[t_4, t_5]$. (f) $[t_5, t_6]$. (g) $[t_6, t_7]$. (h) $[t_7, t_8]$.

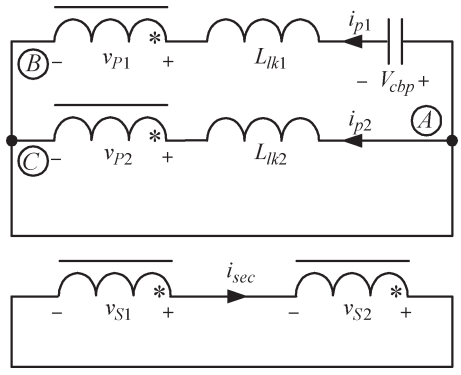

Fig. 4. Further equivalent circuit during $[t_4, t_5]$ in the TL mode.

D_{R2} carries the entire load current, and the converter operates in the second half period, which is similar to the first half period as described previously.

B. Two-Level Mode

As shown in Fig. 2(b), the proposed converter has ten operation stages during a switching period in the two-level mode; among which, $[t_0, t_3]$ is the same as $[t_2, t_5]$ in the TL mode. In the following, only the operation during $[t_3, t_6]$ is analyzed. Fig. 5 shows the equivalent circuits of $[t_3, t_6]$.

1) Stage 4 $[t_3, t_4]$ [refer to Fig. 5(a)]: At t_3, i_{p1} and i_{p2} drop to zero, and D_2 prevents i_{p1} and i_{p2} from flowing in the reverse direction; therefore, i_{p1} and i_{p2} are kept at zero. Both the rectifier diodes conduct and share the load current. During this interval, Q_2 and Q_5 can be turned off with zero-current, and no body diode reverse recovery occurs.
2) Stage 5 $[t_4, t_5]$ [refer to Fig. 5(b)]: Turn on Q_3 and Q_6 at t_4, $v_{AB} = -V_{\rm in}/2$, and $v_{AC} = 0$. The rectifier diodes continue conducting and shorting the series secondary

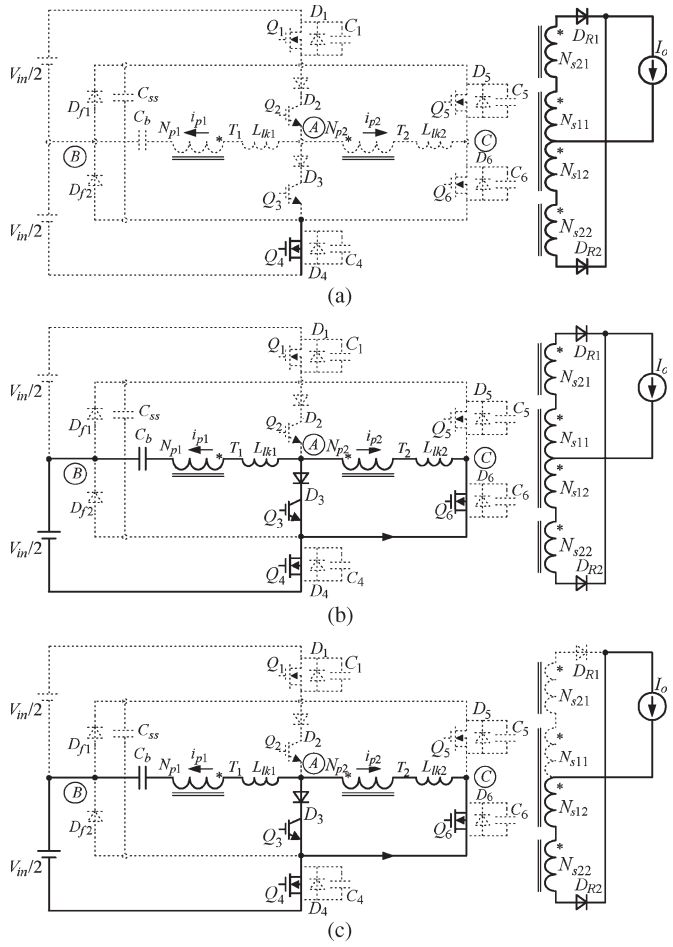

Fig. 5. Equivalent circuits in the two-level mode. (a) $[t_3, t_4]$. (b) $[t_4, t_5]$. (c) $[t_5, t_6]$.

windings of transformers. i_{p1} and i_{p2} increase in the negative direction and arrive at the reflected load current at t_5.

3) Stage 6 $[t_5, t_6]$ [refer to Fig. 5(c)]: From t_5, the primary currents power the load, D_{R1} turns off and D_{R2} carries all the output current, the proposed converter operates in the second half period, which is similar to the first half period.

III. Theoretical Analysis of the Proposed Converter

A. Power Switches

According to the operation principle of the combined TL dc/dc converter, we can know that Q_1, Q_4, Q_5, and Q_6 sustain only half of the input voltage.

During $[t_5, t_6]$ in TL mode, $i_{p1} = i_{p2} = 0$, $v_B = V_{\rm in}/2$, $v_A = V_{cbp} + v_{P1} + V_{\rm in}/2$, and $v_C = -v_{P2} + V_{cbp} + v_{P1} + V_{\rm in}/2$. Therefore

$$v_{AB} = v_A - v_B = V_{cbp} + v_{P1} = \frac{k_1^2 \cdot L_{lk1} \cdot V_{cbp}}{L_{\rm eq}}. \quad (8)$$

$$v_{AC} = v_A - v_C = v_{P2} = \frac{k_1 \cdot k_2 \cdot L_{lk2} \cdot V_{cbp}}{L_{\rm eq}}. \quad (9)$$

The voltages across Q_2 and Q_3 are

$$V_{Q3} = \frac{V_{\rm in}}{2} + v_{AB} = \frac{V_{\rm in}}{2} + \frac{k_1^2 \cdot L_{lk1} \cdot V_{cbp}}{L_{\rm eq}}. \quad (10)$$

$$V_{Q2} = -v_{AC} = -\frac{k_1 \cdot k_2 \cdot L_{lk2} \cdot V_{cbp}}{L_{\rm eq}}. \quad (11)$$

From the earlier expressions, it can be understood that the voltage stress of Q_2 and Q_3 will be slightly higher than $V_{\rm in}/2$, and Q_2 and Q_3 will sustain the negative voltage, which needs diodes in series with them to avoid reverse breakdown.

B. Conditions to Achieve Soft Switching

1) ZVS for Q_1 and Q_4: As analyzed previously, during the switching transition of Q_1 and Q_4 in the TL and two-level modes, the output filter inductance is always reflected to the primary side and in series with the leakage inductances, and the energy stored in these inductances is large enough to ensure Q_1 and Q_4 to achieve ZVS even at light load.

2) ZCS for Q_2 and Q_3: To achieve ZCS for Q_2 and Q_3, the primary currents should decay to zero before Q_2 or Q_3 turns off.

In the TL mode, referring to Fig. 2(a), the time t_{45} is relative to V_{cbp} under different loads according to (7). As the leakage inductances are small, t_{67} is very short to be neglected. If C_b is assumed to be large enough so that v_{Cb} is kept constant during $[t_4, t_5]$, therefore, v_{Cb} varies from $-V_{cbp}$ to V_{cbp} during $T_s/2 - T_{\rm reset}$

$$V_{cbp} = \frac{k_1 I_o}{2C_b}\left(\frac{T_s}{2} - T_{\rm reset}\right) \quad (12)$$

where $T_{\rm reset}$ is the preset resetting time for primary currents, which includes t_{45} and $T_{\rm ZCS}$. $T_{\rm ZCS}$ is the time for most of minority carriers to be combined for IGBTs used as Q_2 and Q_3, and T_s is the switching period.

Substituting (12) into (7) yields

$$t_{45} = \frac{2L_{\rm eq} \cdot C_b}{k_1^2 \cdot (T_s/2 - T_{\rm reset})}. \quad (13)$$

Equation (13) indicates that t_{45} is independent of load current. If (14) is satisfied, the primary currents will be ensured to be reset, and ZCS will be achieved for Q_2 and Q_3 in the full-load and the line range

$$t_{45} + T_{\rm ZCS} \le T_{\rm reset}. \quad (14)$$

As shown in Fig. 2(a), t_{34} is so short that it can be neglected; therefore, $T_{\rm reset}$ is the sum of T_δ and T_d, where T_δ is the time corresponding to the minimal shift phase δ between the drive signals of $Q_1\&Q_4$ and $Q_2\&Q_3$ and T_d is the delay time between the drive signals of the complementary switches. In practical design, $T_{\rm reset}$ is set at a fixed value of around $0.05T_s$.

Similarly, in the two-level mode, referring to Fig. 2(b), time t_{23}, during which the primary currents decay to zero, can be derived as

$$t_{23} = \frac{2L_{\rm eq} \cdot C_b}{k_1^2 \cdot t_{02}} = \frac{2L_{\rm eq} \cdot C_b}{k_1^2 \cdot D_T \cdot T_s/2} = \frac{4L_{\rm eq} \cdot C_b}{k_1^2 \cdot D_T \cdot T_s} \quad (15)$$

where $D_T = V_o/(k_1 \cdot V_{\rm in}/2)$.

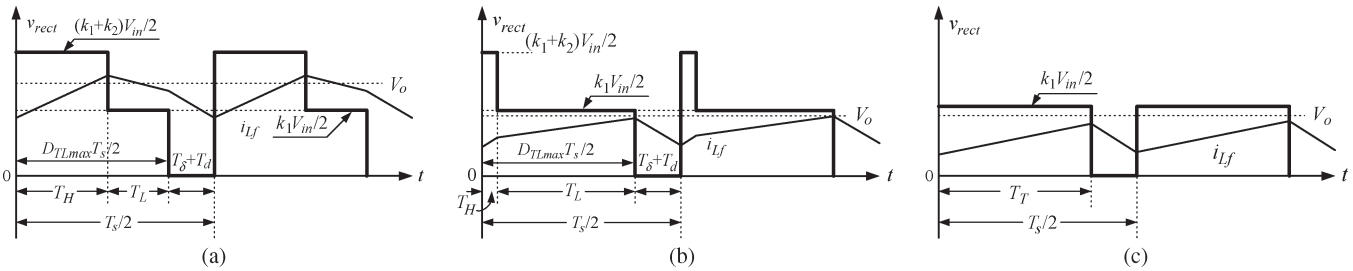

Fig. 6. Rectified voltage waveforms. (a) TL mode, $V_o \geq k_1 V_{\rm in}/2$. (b) TL mode, $V_o < k_1 V_{\rm in}/2$. (c) Two-level mode.

From (15), it can be seen that t_{23} is independent with load current and increases along with the input voltage due to the reduced D_T, as shown in Fig. 2(b). The realization of ZCS for Q_2 and Q_3 in overall load range in the two-level mode depends on the following constraint:

$$D_{\rm sum} = D_{23} + D_{\rm ZCS} + D_T \leq 1 \tag{16}$$

where $D_{23} = t_{23}/((1/2)T_s)$ and $D_{\rm ZCS} = T_{\rm ZCS}/((1/2)T_s)$.

3) ZVS for Q_5 and Q_6: In the TL mode, during the switching transition of Q_5 and Q_6, L_f is reflected to the primary sides of the transformers, and the energy stored in L_f is large enough to realize ZVS for Q_5 and Q_6 in a wide load range.

In the two-level mode, prior to turning off of Q_5 and Q_6, the drain currents have already decayed to zero, as shown in Fig. 2(b); therefore, Q_5 and Q_6 are zero-current turn off. However, there is no current to charge or discharge the intrinsic capacitors of Q_5 and Q_6 prior to their turn on; therefore, they are capacitive turn on.

C. Blocking Capacitor

The value of the blocking capacitor C_b should be designed based on three considerations.

1) ZCS condition for Q_2 and Q_3. Substituting (13) into (14) yields

$$\frac{2L_{\rm eq}\cdot C_b}{k_1^2\cdot(T_s/2 - T_{\rm reset})} + T_{\rm ZCS} \leq T_{\rm reset}. \tag{17}$$

To ensure that Q_2 and Q_3 realize ZCS over the whole load range, C_b must be satisfied with the following expression:

$$C_b \leq k_1^2\cdot(T_s/2 - T_{\rm reset})\cdot(T_{\rm reset} - T_{\rm ZCS})/2L_{\rm eq}. \tag{18}$$

2) Maximum duty cycle of the TL section ($D_{\rm TLmax}$). In the proposed converter, $T_{\rm reset}$ should be preset to realize ZCS for Q_2 and Q_3, as shown in Fig. 2(a). $D_{\rm TLmax}$ is given by the following:

$$D_{\rm TLmax} = 1 - \frac{T_{\rm reset}}{T_s/2}. \tag{19}$$

In order to increase $D_{\rm TLmax}$, C_b should be reduced according to (13) and (19).

3) Voltage stress of Q_2 and Q_3 and series diodes. Referring to (10)–(12), C_b should be selected as large as possible to reduce the voltage stress of Q_2 and Q_3 and series diodes. In the prototype, there will be a tradeoff in determining the value of C_b.

D. VA Ratings of the Transformers

As previously explained, in the two-level mode, T_2 does not contribute to the output, and only T_1 transfers the whole power. Therefore, T_1 should be designed to be able to deliver the whole power at maximum input voltage and full load; then, the VA rating of T_1 is approximately identical to that of the conventional dc/dc converters with single transformer at the same specifications. In the TL mode, as the input voltage decreases, the contribution from T_1 to the output drops, and T_2 delivers the balance of the output power; therefore, T_2 will be chosen to supply the partial output power right down to the minimum input voltage and full load. As a result, the total VA rating of the two transformers in the proposed converter is a little higher than that of the conventional dc/dc converters with single transformer.

IV. Design Consideration for Turn Ratios of Transformers

The turn ratios should be designed to obtain the required output voltage at low line. Fig. 6 shows the ideal secondary rectified voltage waveforms of the proposed converter.

From Fig. 6(a), k_1 and k_2 should satisfy the following expression:

$$(k_1\cdot D_{\rm TLmax} + k_2\cdot D_{\rm Hmax})\cdot\frac{V_{\rm inmin}}{2} = V_o \tag{20}$$

where $D_{\rm TLmax} = 1 - T_{\rm reset}/((1/2)T_s) = 1 - (T_\delta + T_d)/((1/2)T_s)$, $D_{\rm Hmax}$ is the value at full load and the lowest input voltage, and $D_H = T_H/((1/2)T_s)$.

The proposed converter has two freedoms (k_1 and k_2) which provides possibilities of optimizing the performance of the converter. Under the precondition of (20), the specific value of k_1 and k_2 will be designed according to two principles: 1) minimize the output filter inductance and 2) minimize the voltage stress on rectifier diodes.

According to Fig. 6, the output filter inductance L_f of the combined TL dc/dc converter is shown by (21a)–(21c) the bottom of the next page, where Δi_{Lf} is the current ripple of L_f.

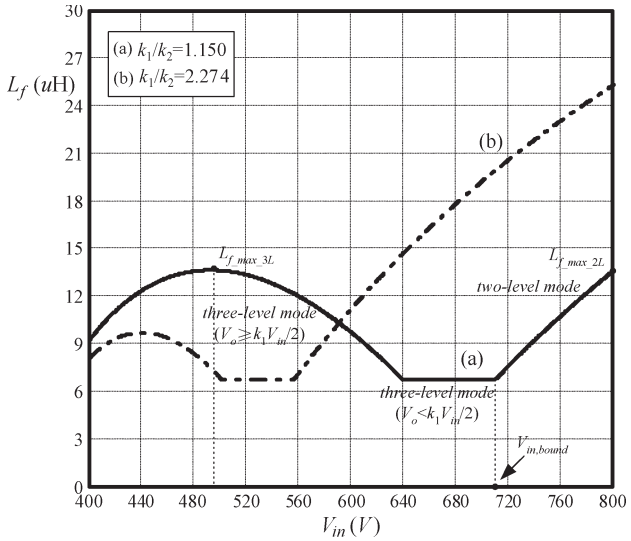

Fig. 7. Curves of the output filter inductance versus the input voltage.

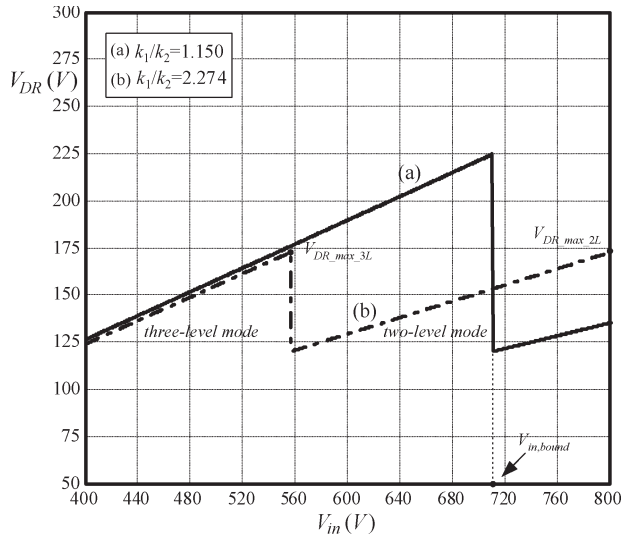

Fig. 8. Curves of the voltage stress on the rectifier diodes versus the input voltage.

With a full-wave output rectifier, the voltage stress on the rectifier diodes is

$$V_{\mathrm{DR}} = \begin{cases} (k_1 + k_2) \cdot V_{\mathrm{in}} & \text{(TL mode)} \quad (22a) \\ k_1 \cdot V_{\mathrm{in}} & \text{(two-level mode).} \quad (22b) \end{cases}$$

According to (20)–(22), it can be known that L_f and V_{DR} are the functions of k_1, k_2, and V_{in}. Figs. 7 and 8 show L_f and V_{DR} versus input voltage for different choices of turn ratios, respectively, where the specifications are the following: $V_{\mathrm{inmin}} = 400$ V, $V_{\mathrm{inmax}} = 800$ V, $V_o = 54$ V, $I_o = 20$ A, $T_s = 10$ us, $\Delta i_{Lf} = 4$ A, and $D_{\mathrm{TLmax}} = 0.9$. In the following, the design procedures of k_1 and k_2 will be discussed.

1) Minimize L_f: According to the computational procedure of minimizing L_f in [13], the maximal L_f in two modes (TL mode, $V_o \geq k_1 V_{\mathrm{in}}/2$, and two-level mode) $L_{f\_\max\_3L}$ and $L_{f\_\max\_2L}$ should be equal; then, the turn ratios must satisfy

$$\left[\sqrt{\frac{2V_o + k_1 \cdot V_{\mathrm{inmin}} \cdot (D_{\mathrm{Hmax}} - D_{\mathrm{TLmax}})}{V_{\mathrm{inmin}} \cdot D_{\mathrm{Hmax}}}} - \sqrt{k_1 \cdot D_{\mathrm{TLmax}}}\right]^2 = \frac{(2V_o - k_1 \cdot V_{\mathrm{inmin}} \cdot D_{\mathrm{TLmax}}) \cdot (k_1 \cdot V_{\mathrm{inmax}} - 2V_o)}{k_1 \cdot V_{\mathrm{inmin}} \cdot V_{\mathrm{inmax}} \cdot D_{\mathrm{Hmax}}}. \quad (23)$$

Once k_1 is calculated, k_2 can be calculated according to (20); therefore, a minimal L_f can be obtained, as shown in Fig. 7 [curve (a)]. However, the V_{DR} in such case is shown in Fig. 8 [curve (a)], where the maximal V_{DR} in the TL mode is higher than that in the two-level mode.

2) Minimize V_{DR}: Similar to the calculation method of minimizing V_{DR} in [13], the turn ratios should satisfy

$$k_1^2 - k_1 \cdot \frac{2V_o \cdot (D_{\mathrm{Hmax}} - D_{\mathrm{TLmax}})}{V_{\mathrm{inmax}} \cdot D_{\mathrm{Hmax}} \cdot D_{\mathrm{TLmax}}} - \frac{4V_o^2}{V_{\mathrm{inmax}} \cdot V_{\mathrm{inmin}} \cdot D_{\mathrm{Hmax}} \cdot D_{\mathrm{TLmax}}} = 0. \quad (24)$$

Once k_1 is calculated, k_2 can be solved according to (20), and then, a minimal V_{DR} can be achieved, as shown in Fig. 8 [curve (b)]. Curve (b) in Fig. 7 shows the value of L_f when the turn ratios are designed to minimize V_{DR}, where the maximal L_f in the two-level mode is larger than that in the TL mode.

From Figs. 7 and 8, it can be known that L_f and V_{DR} cannot obtain minimal values simultaneously whatever the turn ratios may be and that the turn ratios should be determined depending on the specific requirement. In addition, it should be noted that the imprecise turn ratios will have an effect on the boundary input voltage between two modes and subsequently affect the output current ripple and V_{DR}, but the influence is so slight that it can be neglected in a practical design.

V. Design Procedure and Example

This section illustrates a simplified design procedure and example with the input data given in Section IV.

In order to achieve ZCS for Q_2 and Q_3 and increase D_{TLmax} as large as possible, the preset resetting time is designed as $0.05T_s$ (i.e., $T_{\mathrm{reset}} = 0.05 \times T_s = 500$ ns), so that $D_{\mathrm{TLmax}} = 1 - T_{\mathrm{reset}}/(T_s/2) = 0.9$. The delay time between

$$L_f = \begin{cases} \frac{(k_1+k_2)\cdot\frac{V_{\mathrm{in}}}{2} - V_o}{\Delta i_{Lf}} \cdot \left(\frac{2V_o}{k_2 V_{\mathrm{in}}} - \frac{k_1}{k_2} \cdot D_{\mathrm{TLmax}}\right) \cdot \frac{T_s}{2} & \left(\text{TL mode, } V_o \geq \frac{k_1 V_{\mathrm{in}}}{2}\right) \quad (21a) \\ \frac{V_o}{\Delta i_{Lf}} \cdot (1 - D_{\mathrm{TLmax}}) \cdot \frac{T_s}{2} & \left(\text{TL mode, } V_o < \frac{k_1 V_{\mathrm{in}}}{2}\right) \quad (21b) \\ \frac{V_o \cdot \left(1 - \frac{2V_o}{k_1 V_{\mathrm{in}}}\right)}{\Delta i_{Lf}} \cdot \frac{T_s}{2} & \text{(two-level mode)} \quad (21c) \end{cases}$$

the complementary switches is $t_d = 300$ ns; therefore, the time corresponding to the minimum shift phase δ is $T_\delta = 500 - 300$ ns $= 200$ ns.

D_{Hmax} should be chosen as large as possible to minimize the turn ratios and subsequently reduce the conduction losses in the primary side. D_{Hmax} is, however, limited by the maximum duty cycle of the ZVZCS PWM TL section (D_{TLmax}), and it cannot surpass the value of D_{TLmax}. Let $D_{\mathrm{Hmax}} = 0.8$ at the lowest input voltage; then, the relationship between k_1 and k_2 is obtained from (20)

$$k_2 = 0.338 - 1.125k_1. \tag{25}$$

The specific values of k_1 and k_2 are designed to minimize L_f to achieve higher power density and better dynamic performance. From (23) and (25), we can obtain $k_1 = 0.169$ and $k_2 = 0.147$. According to (21), $L_f = 13.62$ μH.

Substituting k_1 and k_2 into (22), the maximum V_{DR} in the two modes is 224.4 and 135.2 V, respectively; therefore, the voltage stress of the rectifier diodes is 224.4 V.

The leakage inductances L_{lk1} and L_{lk2} of the two transformers measured at 100 kHz are 2.6 and 3 μH, respectively; therefore, $L_{\mathrm{eq}} = 0.139$ μH. Referring to the datasheet of the chosen IGBT (IXGH40N60C2D1) for Q_2 and Q_3, the current tail time is $T_{\mathrm{tail}} = T_{\mathrm{ZCS}} = 130$ ns. According to (18), $C_b \leq 0.171$ μF. In actual prototype, C_b is selected as 0.1 μF and is inserted into the ZVZCS PWM TL section.

In the two-level mode, the peak value of v_{cb} (V_{cbp}) is given by

$$V_{cbp} = \frac{k_1 I_o}{2C_b} \cdot t_{57} = \frac{k_1 I_o}{2C_b} \cdot D_T \cdot \frac{T_s}{2} = \frac{I_o V_o T_s}{2C_b V_{\mathrm{in}}}. \tag{26}$$

Therefore, at full load and maximum input voltage, V_{cbp} is 67.5 V. Then, the voltage stresses of IGBTs and series diodes are $V_{\mathrm{IGBT}} = 436$ V and $V_{D(\mathrm{series})} = 40.8$ V, respectively, according to (10) and (11).

With the parameters calculated earlier, it is indicated that IGBTs can realize ZCS over a wide load range in TL mode according to (14), (17), and (18). Meanwhile, it is necessary to verify that whether ZCS for IGBTs can be achieved in the two-level mode, and the boundary condition is given by (16). According to the calculation method in [13], the boundary input voltage between the TL and two-level modes is $V_{\mathrm{in,bound}} = 710.1$ V.

D_{23}, D_T, and D_{sum} as the functions of the input voltage in the two-level mode are shown in Fig. 9. As shown, within the input voltage limit of the two-level mode, D_{sum} is always less than one, which means that the ZCS for IGBTs can be realized over a wide load range in the two-level mode.

The chosen MOSFET (SPW20N60S5) to meet the voltage and current requirements has an intrinsic capacitor $C_{\mathrm{oss}} = 1170$ pF at $V_{\mathrm{ds}} = 25$ V.

The value of the effective intrinsic capacitance C_o is C_{oss} multiplied by a factor of 4/3 [13], i.e.,

$$C_o = \frac{4}{3} \times 1170 \times 10^{-12} \times \sqrt{\frac{25}{V_{\mathrm{in}}/2}}. \tag{27}$$

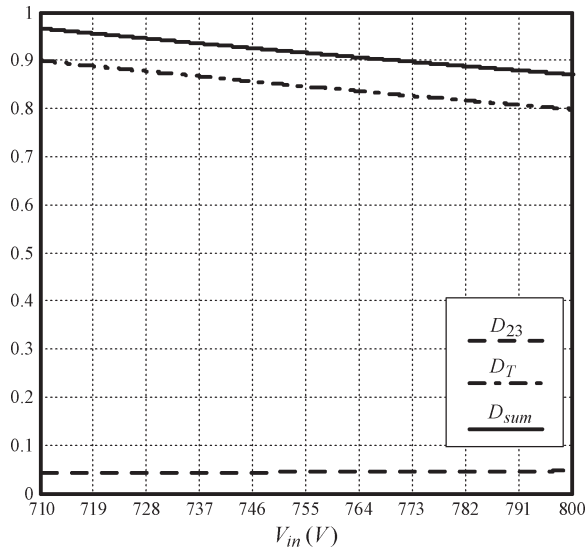

Fig. 9. D_{23}, D_T, and D_{sum} as functions of the input voltage in the two-level mode.

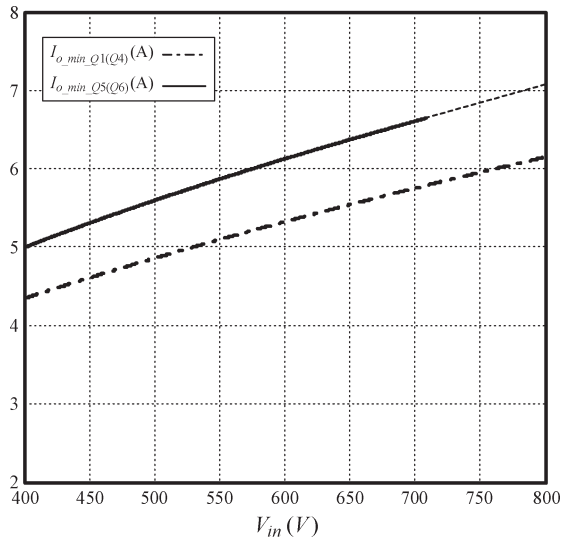

Fig. 10. Minimum load current to achieve ZVS for the switches versus the input voltage.

In order to ensure ZVS for Q_1 and Q_4, the intrinsic capacitor of the incoming switch should be fully discharged by i_{p1} during the delay time. The ZVS condition will be lost if the load current is below $I_{o\_\min\_Q1(Q4)}$, which is expressed by

$$I_{o\_\min\_Q_1(Q_4)} = \frac{V_{\mathrm{in}} \cdot C_o}{t_d \cdot k_1}. \tag{28}$$

$I_{o\_\min\_Q1(Q4)}$ as the function of the input voltage is shown in Fig. 10, from which we can see that Q_1 and Q_4 can realize ZVS when the output current is 4.35 A (21.7% of the full load) and 6.15 A (30.8% of the full load) at the lowest and highest input voltages, respectively.

As analyzed earlier, when the converter transits into the two-level mode, the ZVS condition for Q_5 and Q_6 is lost. While in the TL mode, the intrinsic capacitor of the incoming switch should be fully discharged by i_{p2} during the delay time to

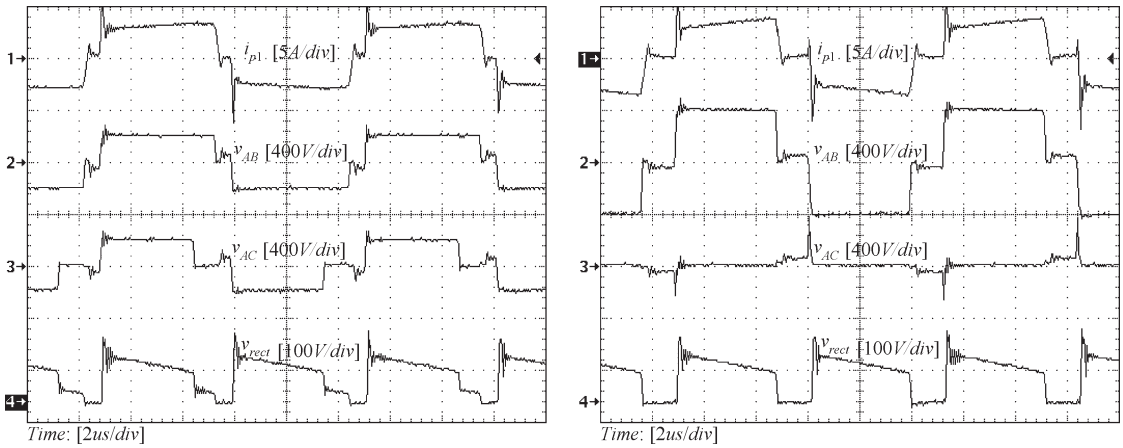

Fig. 11. Experimental waveforms at full load. (a) TL mode. (b) Two-level mode.

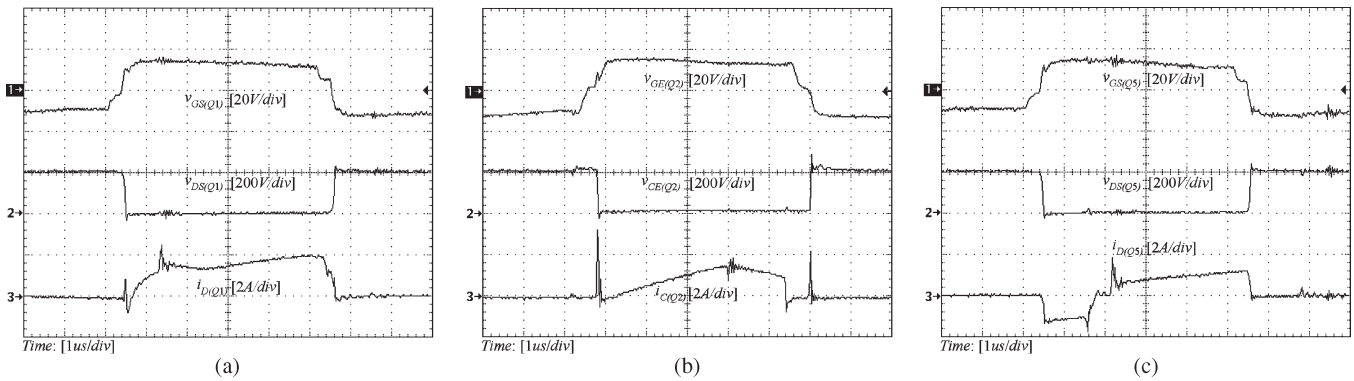

Fig. 12. $v_{GS}(v_{GE})$, $v_{DS}(v_{CE})$, and $i_D(i_C)$ of (a) $Q_1(I_o = 5.5$ A), (b) $Q_2(I_o = 2.5$ A), and (c) $Q_5(I_o = 5.5$ A) at $V_{\rm in} = 400$ V.

provide ZVS for Q_5 and Q_6. Therefore, the minimum load current needed is given by

$$I_{o\_\min\_Q_5(Q_6)} = \frac{V_{\rm in} \cdot C_o}{t_d \cdot k_2}. \tag{29}$$

$I_{o\_\min\_Q5(Q6)}$ as a function of the input voltage is also shown in Fig. 10; it is illustrated that Q_5 and Q_6 can achieve ZVS when the output current is 5 A (25% of the full load) at the lowest input voltage, and the dotted line indicates that the ZVS condition for Q_5 and Q_6 in the two-level mode is lost.

VI. Experimental Results

The performance of the proposed dc/dc converter is verified by a 1080-W (54-V/20-A) prototype circuit operating at 100 kHz from a 400–800-V input. The parameters of the prototype are as follows: MOSFET, SPW20N60S5 (21 A/650 V); IGBT, IXGH40N60C2D1 (75 A/600 V); series diode, DSS16-01A (16 A/100 V); freewheeling diode, DSEI30-06A (30 A/600 V); rectifier diode, DSEP30-03A (30 A/300 V); turn ratios of transformers, $k_1 = 0.169$ and $k_2 = 0.147$; output filter inductance, $L_f = 13.6$ μH; blocking capacitor, $C_b = 0.1$ μF; and switching frequency, $f_s = 100$ kHz.

Fig. 11 shows the experimental waveforms of i_{p1}, v_{AB}, v_{AC}, and $v_{\rm rect}$ at full load in the TL and two-level modes. From Fig. 11(a), it can be seen that, in the TL mode, $v_{\rm rect}$ is a TL waveform due to the voltages of the two transformers added at the secondary side. Fig. 11(b) shows that, in the two-level mode, the pulsewidth of the full-bridge section decreases to zero; therefore, $v_{\rm rect}$ is a two-level voltage waveform.

Fig. 12 shows the gate drive signal $v_{GS}(v_{GE})$, the voltage across the drain (collector) and source (emitter) $v_{DS}(v_{CE})$, and the drain (collector) current $i_D(i_C)$ of Q_1, Q_2, and Q_5, respectively, at light load and $V_{\rm in} = 400$ V. It can be seen that the ZVS turn on for MOSFETs is achieved while the antiparallel diode is conducting before the MOSFET is turned on. The IGBTs are turned off with complete ZCS since the current through it is zero before turning off. There is no IGBT tail current due to ZCS.

Fig. 13 shows the experimental waveforms at light load and $V_{\rm in} = 800$ V, where the converter operates in the two-level mode. As shown in Fig. 13(a) and (b), Q_1 and Q_2 can still realize ZVS and ZCS. However, as shown in Fig. 13(c), before Q_5 turns off, i_{p2} has already decreased to zero; therefore, Q_5 can realize zero-current turn off, and there is a current spike resulted by charging its own output capacitance when Q_6 is turned on. The experimental results are in substantial agreement with the theoretical analysis in Section V.

Fig. 14(a) shows the overall efficiency of ZVZCS PWM combined TL converter under different load currents with an input voltage of 400 and 800 V; the ZVS PWM combined TL converter is also included for comparison. Fig. 14(b) shows the

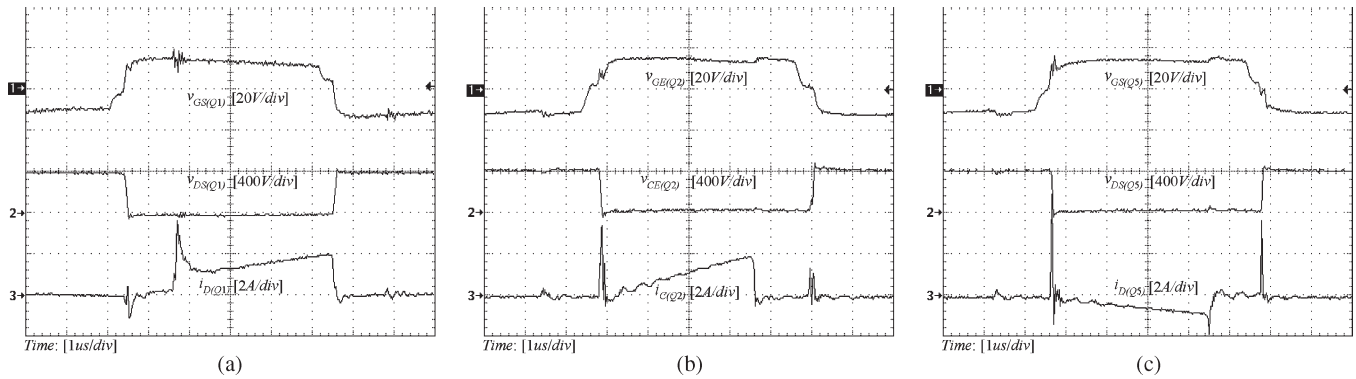

Fig. 13. $v_{GS}(v_{GE})$, $v_{DS}(v_{CE})$, and $i_D(i_C)$ of (a) $Q_1(I_o = 7\text{ A})$, (b) $Q_2(I_o = 2.5\text{ A})$, and (c) $Q_5(I_o = 2.5\text{ A})$ at $V_{\text{in}} = 800\text{ V}$.

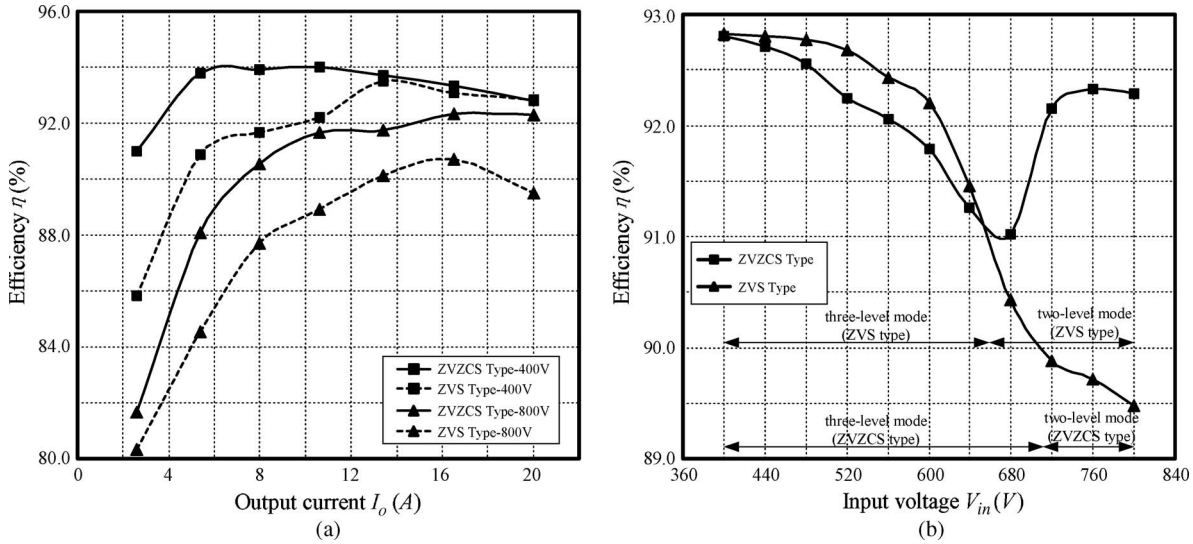

Fig. 14. Conversion efficiency. (a) Efficiency at different output currents under the lowest and highest input voltages. (b) Efficiency at full load under different input voltages.

overall efficiency at full load under different input voltages. As shown in Fig. 14(a), the efficiency of the ZVZCS type is relatively higher under full load range variations, owing to ZVS and ZCS realization for the switches and the elimination of the body diode reverse recovery loss. As the load current increases in the TL mode, the additional conduction losses of series diodes increases, which reduce the efficiency difference between ZVZCS and ZVS types until the two efficiency curves intersect at full load. In Fig. 14(b), the efficiency of the ZVZCS type is lower than the ZVS type in the TL mode due to the conduction loss of the series diodes and is higher in the two-level mode because there is no body diode reverse recovery loss.

VII. Conclusion

This paper has proposed a ZVZCS PWM combined TL dc/dc converter, which has the following advantages.

1) All power switches sustain only half of the input voltage.
2) ZVS for the leading switches in a wide load range.
3) ZCS for the lagging switches in a wide load and line range.
4) The output filter inductance and the voltage stress on rectifier diodes are reduced.

Furthermore, with the reduced output filter inductance, the converter has potentially high power density and rapid dynamic response. It is quite suitable in high power and high input voltage with wide range applications.

In addition, it should be pointed out that, as the total VA rating of the transformers in the proposed converter is higher than that of the dc/dc converter with single transformer, some optimization schemes such as magnetic integration technique for the transformers should be investigated and employed in the future to achieve a higher power density.

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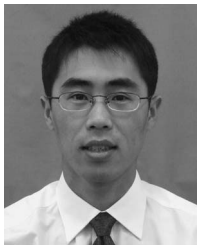

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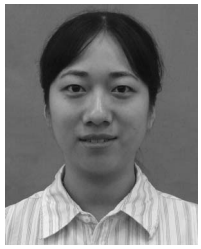

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